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Ge-Source Based L-shaped Tunnel Field Effect Transistor for Low Power Switching Application

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Abstract- **In this work, the performance of the heterojunction L-Tunnel Field Effect Transistor (LTFET) has been analyzed with different engineering techniques such as bandgap engineering, pocket engineering, work-function engineering, and gate dielectric engineering, respectively. The electrical characteristics of the device has been investigated by using Synopsys Sentaurus TCAD tool and compared with some recent other TFETs. The proposed Ge-source L-TFET device with n-type pocket shows ON-state current of $2.12*10^{-5}$ Aμm^{-1}, OFF-state current of $1.09*10^{-13}$ Aμm^{-1}, current ratio of ~10^{8} and sub-threshold slope (SS) of 21 mV/decade and the threshold voltage of 0.26 V and compared to the conventional Si/Ge source L-shaped TFETs without pocket simulation result. The pocket engineering techniques suppress the leakage without degrading the ON current, threshold voltage and SS of the proposed device. The simplified fabrication steps of the proposed device have also been discussed. The proposed L-TFET is free from ambipolarity issues and can be used to develop low-power switching devices.**

Keywords— **Tunnel Field Effect Transistor; Heterojucntion; Band-to-Band Tunneling; Ambipolarity; Subthreshold Swing.**

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1. Introduction

In the rapid advancement of Internet of Things (IoT) and wearable technology, low power operation is a huge concern for digital applications [1-3]. Though, metal oxide semiconductor (MOS) devices can be utilized in microprocessor and static RAM (SRAM) but the subthreshold swing (SS) cannot be lowered than 60 mV/dec [4-5]. The downscaling of MOSFETs dimensions in sub-nanometer region increases the proximity between source and drain increases that further reduces the controlling capability of the gate over the channel. Also, scaling down the MOSFET leads to high SS, short channel effects and leakage current [6-7]. On the current technology nodes, rapid switching and scaling are the substantial factors as per the device requirements. The reduction in fundamental limit of the SS can improve the switching mechanism. As a breakthrough, Tunnel Field-effect transistors (TFETs) has appeared as a promising candidate due to its steep slope (SS<60 mV/dec) and can be used for low power applications. TFETs are a gated reverse biased p-i-n diode that works on the principle of band-to-band-tunnelling (BTBT) and exhibits low leakage current and reduced short channel effects [8][9]. Still, TFET withstands some limitations like low on-current, large ambipolar current and poor RF performance that demand additional improvements [10-11]. These technical issues can be entangled by using different design approaches like using high-k material as dielectric [12], III-V semiconductors [13], use heavily doped pocket [14], and making different shaped TFET [15-17].

Several researchers have reported different strategies to overcome the shortcomings of TFET [18-21]. The ON-state current can be increased by increasing the gate-source overlap that enhances the tunneling area, using doped pocket [22], and hetero gate dielectric [23]. Another solution is to increase the effective channel length by structural changing like recessed channel and mesa structure [24]. The ambipolarity can be reduced by considering asymmetric source-drain doping, large band gap materials for drain, gate-drain overlap, and heterogenous gate dielectric etc [25-26]. However, these strategies can result in some serious problems in TFETs like increases in drain resistance, lowers on-current or makes the process more complex [27]. Keeping these points in mind, in this paper, L-Tunnel Field Effect Transistor (LTFET) of 20 nm gate length has been investigated with different engineering techniques such as bandgap engineering, pocket engineering, work-function engineering, and gate dielectric engineering, respectively, by using Sentaurus TCAD tool. The effect of different design parameters on the device performance is observed and discussed in different sections. This paper is organized as follows: The propose L-TFET structure and its simulation methodology has been described in section 2. The impact of pocket engineering on homojunction and heterojunction L-TFET and the calibration of the proposed device have been discussed in section 3. The optimization of the proposed device and fabrication process flow are described in Section 4 and Section 5. Section 6 deals with results and discussions and different parameters are analyzed by the drain voltage variation in section 7. Section 8 discusses the comparative analysis of proposed device with already existing structures. Finally, this paper is concluded in section 9.

2. Proposed TFET Structure and Simulation Methodology

The working of TFET is based on principle of quantum tunneling which states that if a particle does not have sufficient energy to cross a potential barrier but still it tunnels through the barrier. In TFET, the movement of carrier depends upon the BTBT phenomena. The tunneling probability depends upon the height, width, shape of the potential barrier, and tunneling mass of charge carriers. Kane's approach and Wentzel-Kramers-Brillouin's approach (WKB) approaches can be used to calculate the rate of BTB tunneling [28]. The rate of tunneling is given in Eq. (1) [29]:

$$T = \exp^{\frac{-\sqrt[4]{2m_r}\,E_g^{1.5}}{3q\hbar}} \exp^{\frac{-E_\perp}{E}} \tag{1}$$

Where q= electron charge, F=average junction field, $E_\perp$ = transverse component of total carrier energy, E= the impact of the transverse-energy-state carriers on the tunneling magnitude.

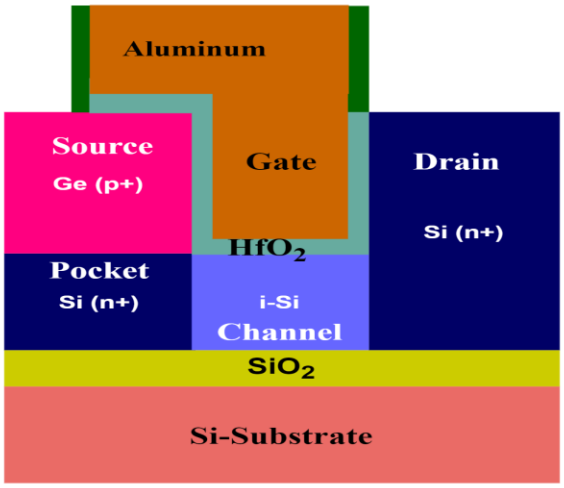

Fig. 1: Schematic view of proposed L-TFET

Figure 1 shows the cross-sectional view of proposed n-type LTFET in which Ge as source material and Si is as drain material. In the source region, the low band gap material Ge offers higher tunneling in the ON state while on the drain side the high band gap material Si weakness the tunneling. The optimized doping concentration of $1\times 10^{18} cm^{-3}$ for source, $1\times 10^{18}\ cm^{-3}$ for drain, $1\times 10^{16}\ cm^{-3}$ for channel, and has been considered. The gate metal function is taken 4.3 eV with 4 nm physical thickness and 0.57 nm as Equivalent Oxide Thickness (EOT) of HfO_2. The length of source and drain regions are 40 nm each while width of source is 40 nm and drain are 55 nm, respectively, has been fixed for all simulations. The width of pocket and channel regions are 15 nm while length of pocket is 40 nm and length of channel is 32 nm. The optimized thickness of SiO2 and Si-substrate are 5 nm and 30 nm, respectively.

3. Proposed Device Justification

In this section, the proposed device has been justified through comparative study of homo and hetero junction TFET with and without pocket and also calibrated with published experimental results.

A. Homo- and Hetero junction TFET with and without pocket

In this section of study, the device parameters and dimensions mentioned in section 2 has been considered. Fig. 3 depicts the analysis performed for LTFET with pocket and without pocket structure by considering Si and Ge as source material. It has been observed that LTFET device using Ge as source material exhibits very good performance as it has high on-state current and low leakage current, whereas, in Si based LTFET though the OFF current is low but ON current is also poor. On comparing the results of with pocket and without pocket structures, the Ge-LTFET with pocket device shows very good results because of high I_{ON}/I_{OFF} ratio. Further analysis has been carried out using Ge with pocket structure. The influence of use of pocket is more noticeable in OFF current than in ON current. It is also clear from plot that Ge-LTFET device shows very good performance as there is no ambipolarity observed in the results. The results of all important parameters I_{ON}, I_{OFF}, I_{ON}/I_{OFF} ratio, SS, g_m, V_{th} for both Si and Ge based LTFETs with and without pocket structures has been discussed in Table I.

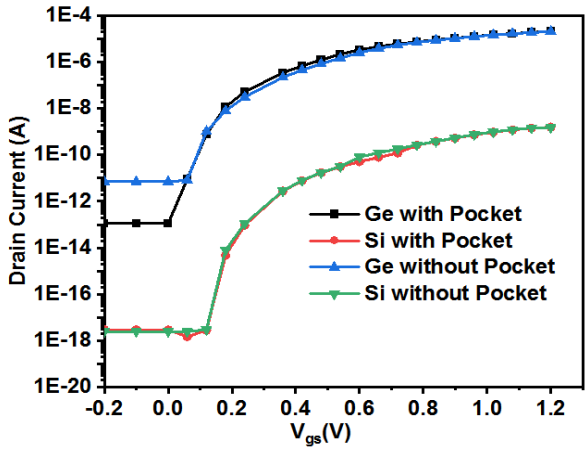

Fig. 2: I_d-V_{gs} curve for Si/Ge source with and without pocket TFET

Table 1: Obtained results for Si and Ge TFETs

Parameters	Si (without pocket)	Si (with pocket)	Ge (without pocket)	Ge (with pocket)
I_{ON}(A)	$1.52*10^{-9}$	$1.59*10^{-9}$	$2.11*10^{-5}$	$2.12*10^{-5}$
I_{OFF}(A)	$2.41*10^{-18}$	$2.88*10^{-18}$	$6.99*10^{-12}$	$1.09*10^{-13}$
I_{ON}/I_{OFF}	$0.63*10^{-9}$	$0.55*10^{-9}$	$0.30*10^{-7}$	$1.94*10^{-8}$
g_m (S/m)	$4.32*10^{-9}$	$4.21*10^{-9}$	$3.59*10^{-5}$	$3.54*10^{-5}$
V_{th} (V)	0.62	0.60	0.30	0.26
SS (mV/decade)	33	31	27	21

B. Calibration of the device:

Here, the simulated proposed LTFET structure is calibrated against the experimental data of reference [30] at drain voltage 0.5V as shown in Fig.3. It is observed that there is a good matching of both data, which certify the validity of the selected models.

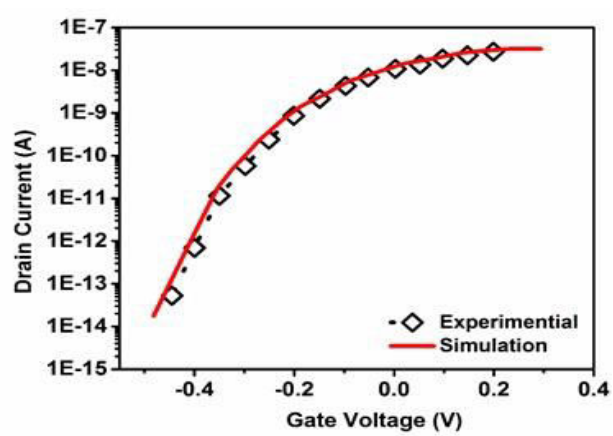

Fig. 3: Calibration of TCAD simulation set up of proposed device with experimental data of reported paper [30].

4. Optimization of Proposed Device

In this section, the optimization of the proposed LTFET has been done in terms source doping concentration, pocket doping concentration variation, gate oxide material variation, and work function variation, respectively. Also, the BTBT model has also been optimized by using different band to band models.

A. Different Band to Band Models

The Band-to-Band Tunneling (BTBT) is the quantum mechanical phenomena and can be achieved by two processes; one is direct and another is phonon assisted tunneling. There are various BTBT tunneling models such as Hurkx BTBT model, Schenk BTBT model, Simple (E1, E2, E1_5) BTBT model and the non-local model are available in Sentaurus TCAD. Hurkx BTBT model, Schenk BTBT model, Simple (E1, E2, E1_5) BTBT model are the local models [31]. In both local and non-local models, the electron-holes generation profiles are different. In the former case, electron-holes generation profiles are same while in the latter case holes are generated at the beginning and electrons are generated at the end of tunneling. In TCAD tool, Schenk BTBT model bandgap narrowing model can be used in two ways. In the simple way, bandgap narrowing can be computed without depending on temperature (at T=0 K) and in the other way, temperature dependence is accounted. In Hurkx model, tunneling carriers are modelled by an additional generation-recombination process. The Hurkx model can be written as [32]:

$$R_{BTBT} = AD\varepsilon^{p} e^{\frac{-B}{\varepsilon}} \tag{1}$$

Where R_{BTBT} is the BTBT rate, and the coefficients *A, B, D* and *p* can be specified in the BTBT parameter set. These coefficient's values can be used to define carrier generation and recombination.E1, E2, E1_5 selects the simple models.

The Non-local BTBT model implements the nonlocal generation of electrons and holes that occurs because of the direct and phonon-assisted BTBT processes. In the direct bandgap semiconductors, the direct tunneling occurs. But in the indirect semiconductors (Si and Ge), phonon-assisted tunneling process dominates. The electron-holes generation rate is obtained by nonlocal path integration. Suppose atunneling path of length l is given that starts at x=0 and ends at x=l. The holes are generated at x=0 and electrons are generated at x=l. The net hole recombination rate due to phonon-assisted tunneling can be written as equation 3 [33].

$$R_{net}^{p} = |\nabla E_V(0)| C_p exp\left(-2\int_0^{x_0} \kappa_V dx - 2\int_{x_0}^{l} \kappa_C dx\right)\left[\left(exp\left[\frac{\varepsilon - E_{F,n}(l)}{kT(l)}\right]+1\right)^{-1} - \left(exp\left[\frac{\varepsilon - E_{F,p}(0)}{kT(0)}\right]+1\right)^{-1}\right] \tag{2}$$

$$C_p = \int_0^{l} \frac{g(1+2N_{op})D_{op}^2}{2^6\pi^2\,\rho\varepsilon_{op}\,E_{g,tun}} \sqrt{\frac{m_V m_C}{hl\sqrt{2m_r E_{g,tun}}}}\, dx \left(\int_0^{x_o}\frac{dx}{\kappa_V}\right)^{-1}\left(\int_{x_o}^{l}\frac{dx}{\kappa_C}\right)^{-1}\left[1 - exp\left(-k_{vm}^2\int_0^{x_0}\frac{dx}{\kappa_V}\right)\right]\left[1 - exp\left(-k_{cm}^2\int_{x_0}^{l}\frac{dx}{\kappa_C}\right)\right] \tag{3}$$

where, h is the Planck's constant, g is the degeneracy factor, ρ is the mass density, κ_V and κ_C are the magnitude of imaginary vectors. D_{op}, $\varepsilon_{op}$and N_{op} are the deformation potential, energy, and number of optical phonons, respectively. Figure 4 shows the simulation results of proposed Ge-source L-TFET with pocket using different models. Both local and non-local has been used one by one and results were obtained. It clearly observed that non-local BTBT model gives the best results among all the models.

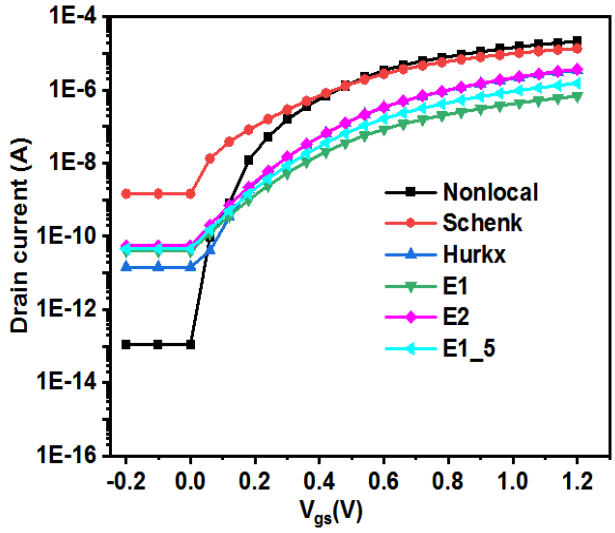

Fig. 4: Proposed L-TFET analysis using different TCAD models

B. Doping Variation in Source and Pocket

The effect of doping concentration variation in source region and pocket region has been discussed in this sub-section. For both, source and pocket region, three different concentration values were considered for optimization and shown in Fig.5 . As shown in Fig. 5 (a), for source doping region, the concentration values 1E17, 1E18 and 2E18 has been taken and it is clear from plot that the source concentration 1E18 can be considered for further analysis as it shows high on-state current and low off-state current. In pocket doping concentration variation, 1E18 shows low off-state current and high on-state current as shown in Fig. 5(b). For further analysis the source and pocket doping concentration values are fixed i.e. 1E18.

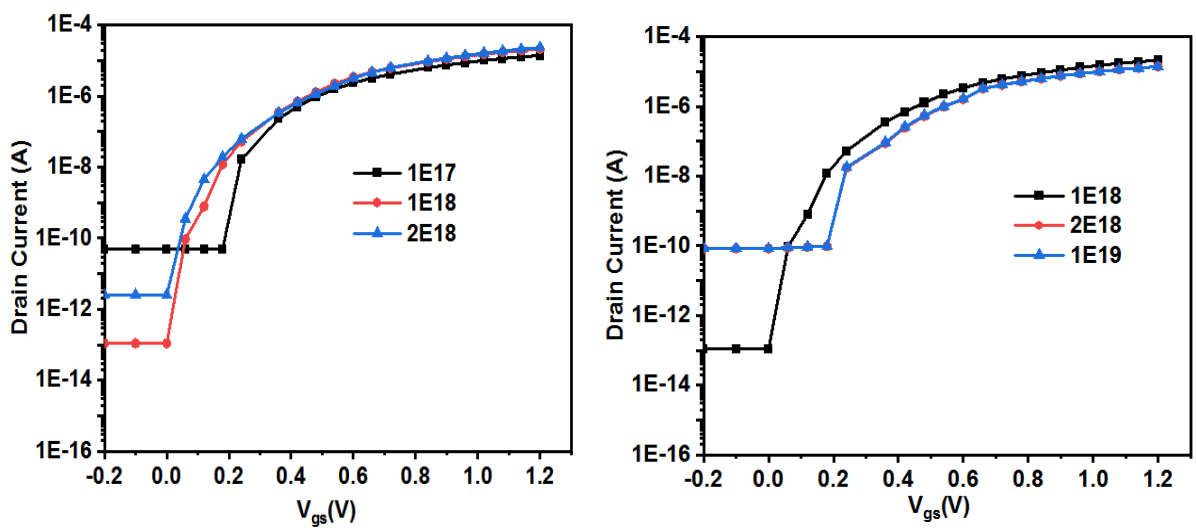

Fig. 5 : I_d-V_{gs} curve for variation in (a) source doping concentration (b) pocket doping concentration

C. Gate Oxide Material

The gate dielectric should be chosen carefully to achieve high ON current and low subthreshold swing. The physical gate oxide thickness of 4 nm has been considered with different materials such as SiO_2, HfO_2, and Si_3N_4, respectively.

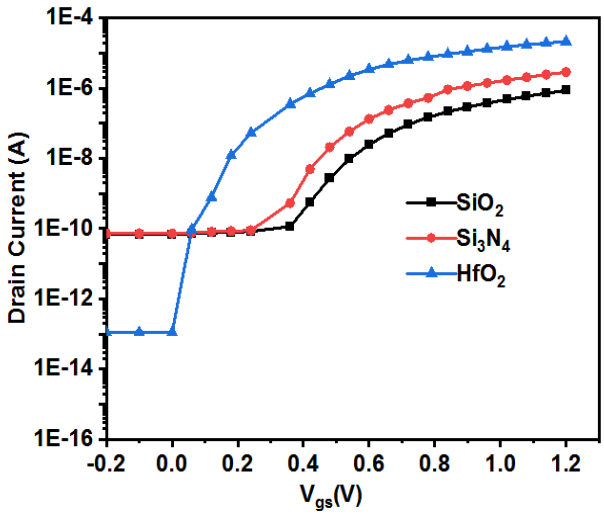

Fig. 6: I_d-V_{gs} curve for different dielectric material

It is very clear from Fig. 6 that high dielectric constant material HfO_2 shows superior performance over other two materials (SiO_2 and Si_3N_4). On increasing the dielectric constant, the on-state current increases. The small dielectric thickness offers the solution to the problem of low on-state current.

D. Work Function variation

The effect of gate work function variation on drain current has been observed in this sub-section. The work function value considered for variation are from 4.3 eV to 4.7 eV. Fig. 7 shows the simulated results of drain current vs gate voltage for different work functions. It is observed that increasing the work function reduces the on-state current. The work function value of 4.3 eV has been considered for the proposed L-TFET exhibits high on-state current and low off-state current. The variation in work function causes the variation in threshold voltage, on-state current and off-state current.

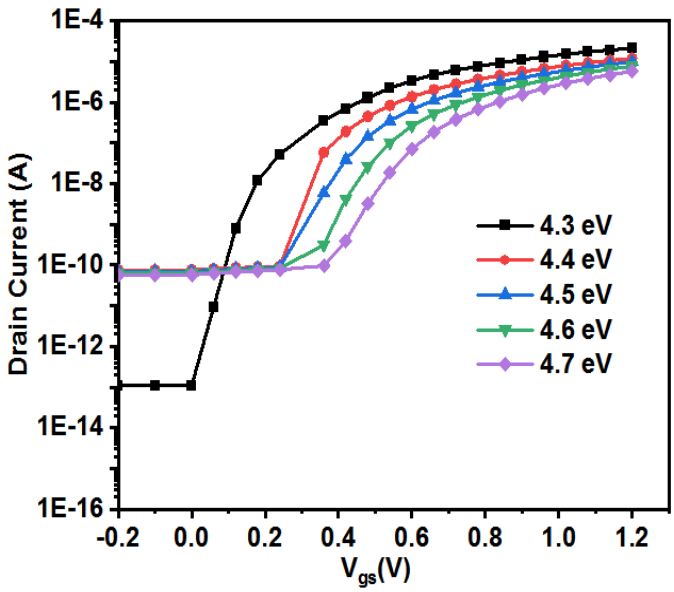

Fig. 7 : I_d-V_{gs} curve for different work function

5. Fabrication details of the proposed device

The proposed L-TFET may be fabricated by using CMOS compatible process flow as shown in figure 8. Following steps have been required for the possible fabrication of the proposed device. Firstly, intrinsic silicon layer is deposited over SiO_2 (fig 8 (a)).

Thermal Oxidation and Diffusion: Thermal oxidation is used to grow the oxide layer for passivation of i-channel region. However, the diffusion method is used to dope the silicon layer (n+ layer) for the formation of pocket and drain regions (fig 8 (b)).

Etching: The etching of Si can be done by using the dry etching method or the wet etching method. In dry etching, gas plasma etches Si (isotropic/anisotropic) depending upon the gas recipes used. In the wet etching method, chemicals are used to etch Si. After patterning the oxide, etching of Si layer is done (fig 8 (c)(d)).

Low-Pressure Chemical Vapour Deposition (LPCVD): LPCVD method is used to deposit a 40 nm thick Ge layer to form the source region. Further, the Ge layer is p+ doped using the diffusion method(fig 8 (e)).

Atomic Layer Deposition: This technique is used to deposit hafnium oxide as gate oxide (fig 8 (f)).

Sputtering: This method is used to deposit thin films of various materials. Aluminum gate can be formed using the sputtering method(fig 8 (g)). At last the spacer layer, Si_3N_4 can be deposited using LPCVD/ Plasma Enhanced Chemical Vapour Deposition (PECVD) method.

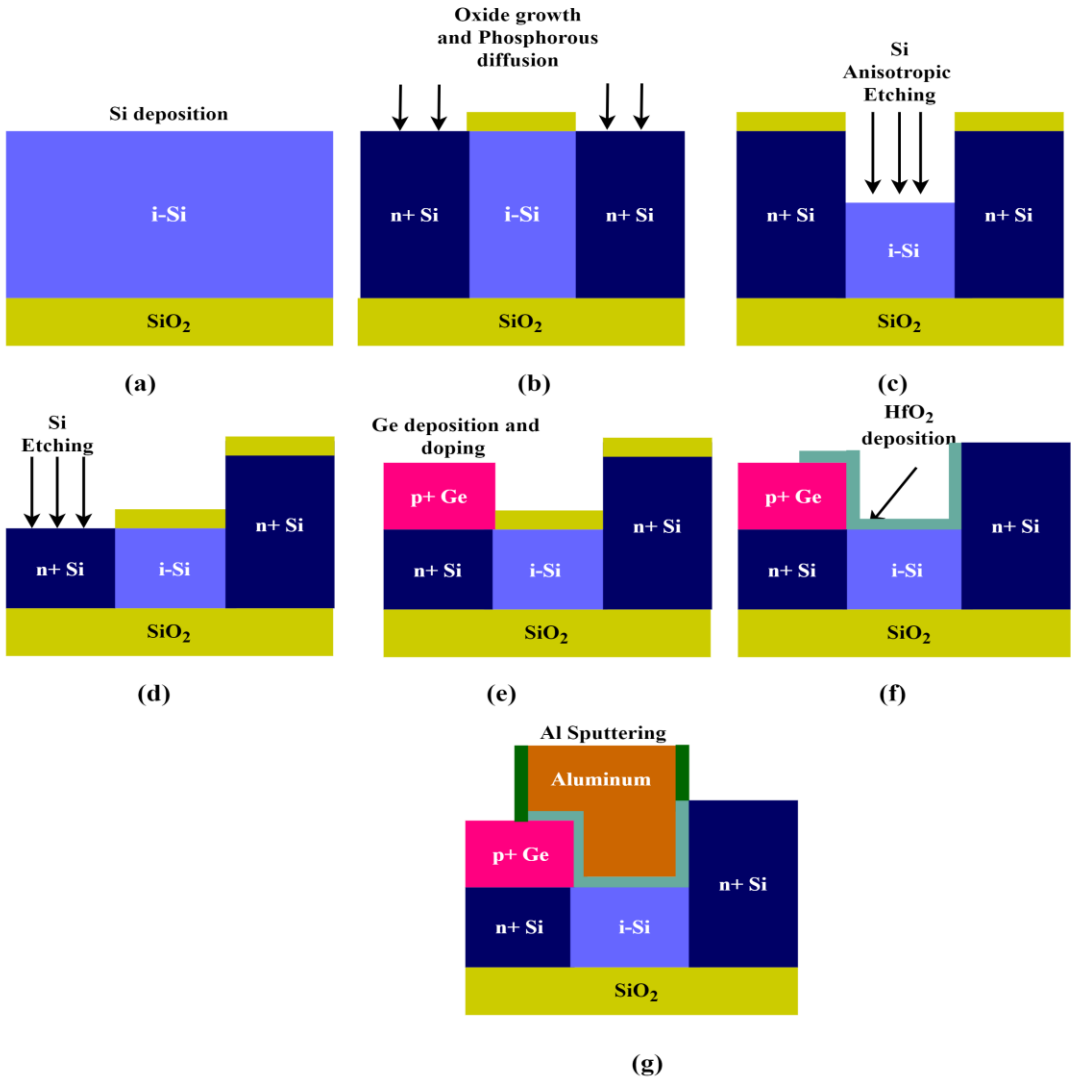

Figure 8: Fabrication process flow of proposed LTFET

6. Results and Discussion

The simulated results of the L-TFET device have been presented in this section. The back gate has been kept at ground potential. Also, the effects of variation in different parameters on the device performance are presented in subsections. The proposed LTFET structures are simulated in a Sentaurus TCAD environment. The interband tunneling phenomena in L-TFET is encounter by using the non-local BTBT model. To account the effect of high doping concentration on carrier mobility, Doping Dependent Mobility' model has been used. Also, Shockley-Read-Hall (SRH) Recombination Model has been used. The accurate modelling of charge carrier transport in L-TFET is achieved by activating, doping density, band gap narrowing, and thermionic models. Fig. 9 shows the simulated L-TFET device simulated by Sentaurus TCAD tool and differently doped regions are indicated by different colours.

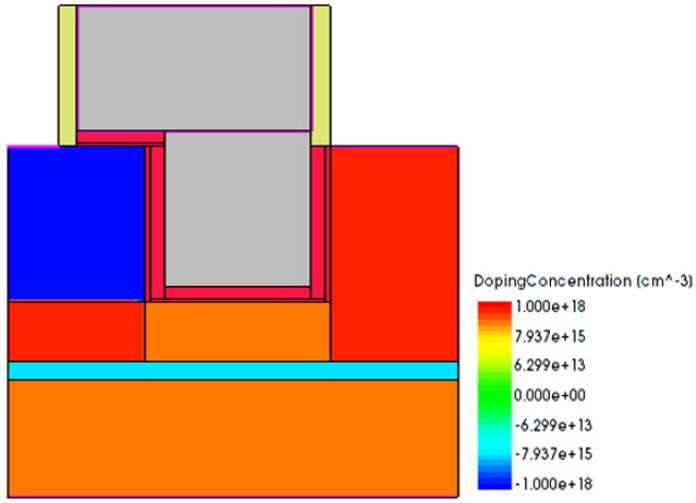

Fig. 9: Simulated L-TFET device

A. Energy Band Diagram:

The L-TFET has been simulated using optimized device dimensions and the electric potential distribution is shown in Fig. 10 (a). Fig. 10 (b) depicts the energy band diagram of Si and Ge LTFET with pocket structures. When the gate overlaps the source, line tunneling occurs, and such a TFET structure is also known as line TFET [34], as shown in figure 10 (a) (b). In this case, increasing the V_{gs} bends the energy band towards the gate oxide until the conduction band edge crosses the valence band edge and BTBT happens. The uniform electric field beneath the gate oxide implies that in line tunneling the effect of V_d on source can be ignored. Below the gate-source overlap, all tunnel paths are available at the same amount of band bending but the paths get shorten as V_{gs} is increased. As the tunneling is located near the gate region and both electric field and tunnel path are aligned, small amount of V_{gs} is sufficient for band bending. When the TFET is conducting, stronger the band bending makes shorter the tunnel path. In short, I_{ON} depends upon the overlapping between gate and source. It is observed from Fig. 10 (b) that the use of Ge as source material in L-TFET shortens the tunneling path and more tunneling occurs as compared to Si based L-TFET.

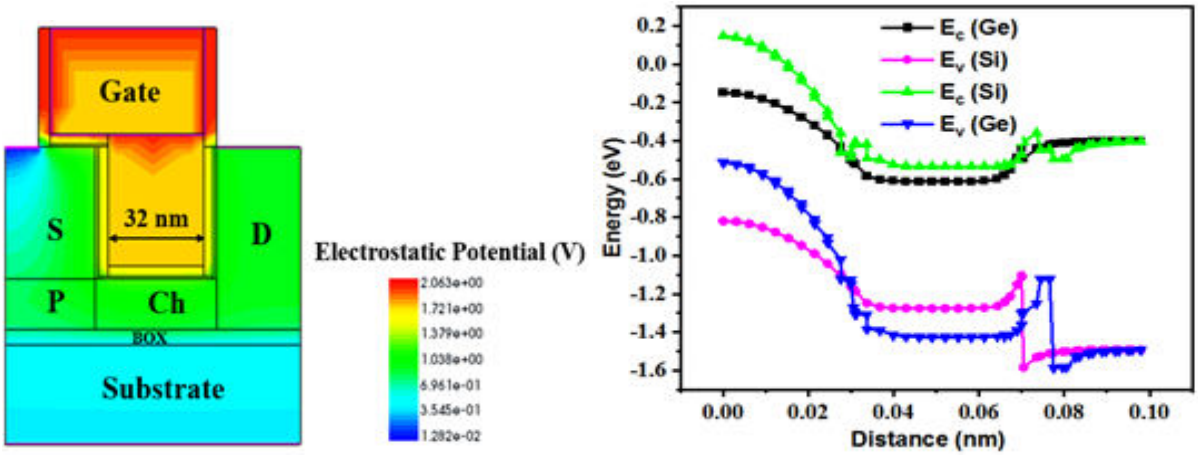

Fig. 10: (a) 2D contour of electric field (b) Ge, Si TFETs with pocket structures

B. *Input and Output Characteristics*

The transfer characteristic of the proposed L-TFET is shown in Fig. 11(a). It is evident from the results that the proposed LTFET works very efficiently from for. The I_{ON} of 4.4 µA, $2.12*10^{-5}$ A, $4.32*10^{-5}$ A and I_{OFF} of $1.03*10^{-13}$ A was observed for different V_{ds} i.e. 0.3 V, 0.5 V, 0.7 V, respectively. It is clear from the plot that the increase of drain voltage increases only ON current and does not change the SS and threshold, which is one of the important requirements of the devices voltage of the device. So we can say that, the proposed L-TFET structure works very efficiently with high on-state current, low off-state current and no ambipolar behaviour has been observed.

The output characteristics of proposed L-TFET for the drain voltages ranges from 0 to 2.5 V for different gate voltages are shown in figure 11 (b). For small values of V_{ds}, BTBT is inefficient because of low carrier density but BTBT rises as V_{ds} is increased. The drain current increases as the V_{ds} is increased until the edge of conduction band in drain region falls below the edge of the conduction band in the channel. After that drain current saturates and V_{ds} has no longer affect on the tunneling. On increasing the gate voltage, the exponential rise in drain current demonstrates better gate control. The flat saturation region indicates that the effects like kink effects are highly suppressed in this proposed L-TFET.

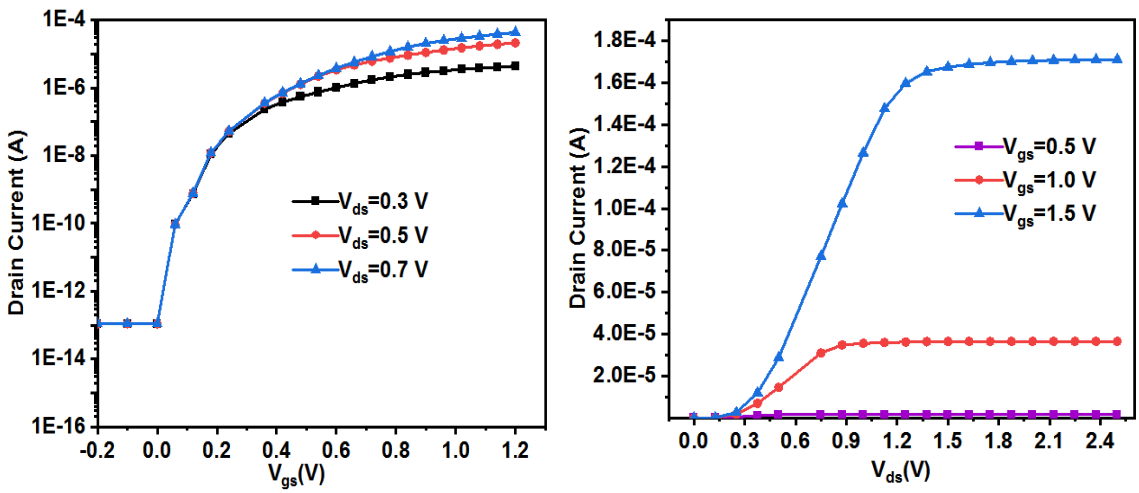

Fig. 11: (a) I_d vs V_{gs} for different drain voltages (b) I_d vs V_{ds} for different gate voltages

7. Impact of Drain Voltage Variation

Fig. 12 shows the influence of V_{ds} variation on threshold voltage, transconductance (g_m), and subthreshold swing (SS). In the given plot of Fig. 12 (a), as V_{ds} is increased, the threshold voltage obtained by constant current method remains the same wheras the threshold voltage obtained by transconductance method increases. The impact of drain voltage variation on point and average SS is shown in Fig. 12 (b). It is clear from plot that both SS slightly increases as drain V_{ds} > 0.7 V, which the proposed device is suitable for low power application. The increase of drain voltage increases the g_m, as shown in Fig. 12 (c), which indicates that the device operates with higher frequency of unit gain.

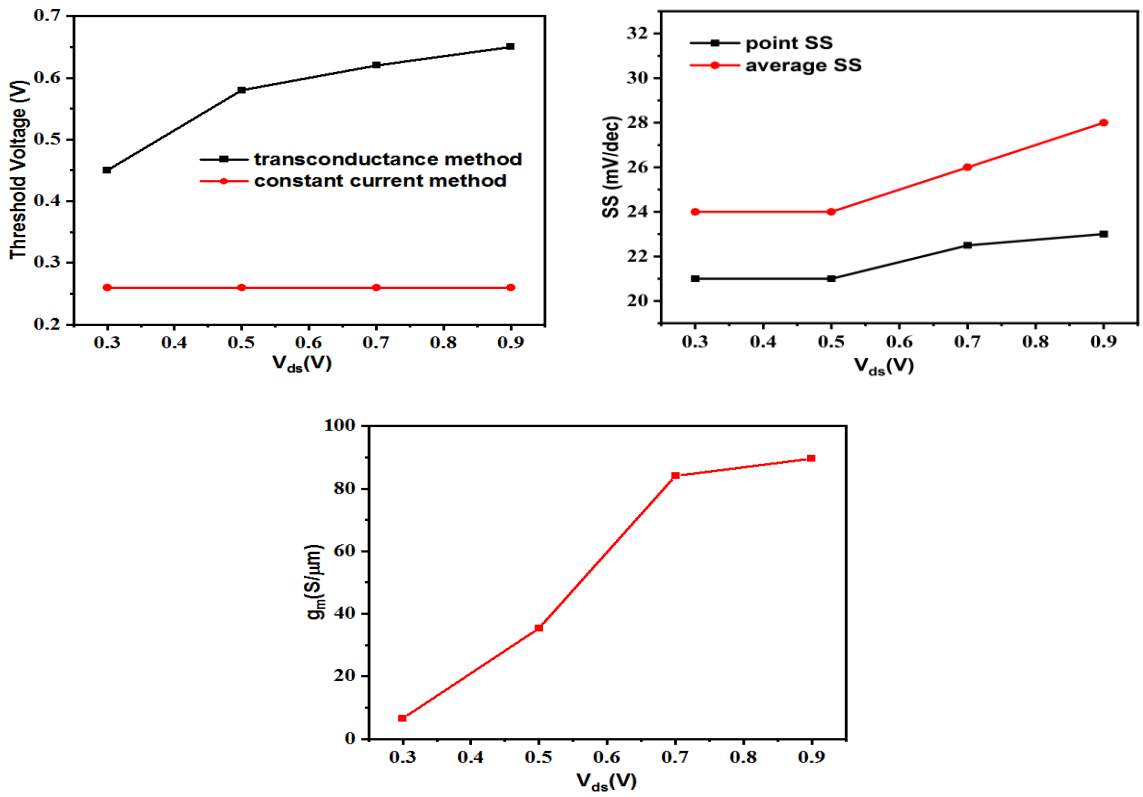

Fig. 12: V_{ds} variation for (a) Threshold voltage (b) SS (c) g_m

8. Comparison with other LFETs

This section discuss the comparison of the proposed L-TFET device with already reported TFET devices like Si TFET, fully depleted (FD) SOI-TFET with Ge source, Si LTFET, TFET using III-V, etc is given in Table 2. From the comparison it can be concluded that the proposed LTFET using Ge as source region is very performing efficiently and further RF and AC analysis can be done to observe the performance.

Table 2: Comparison of proposed LTFET with other TFETs

Ref. no.	V_{dd} (V)	I_{ON} (A/μm)	I_{OFF} (A/μm)	I_{ON}/I_{OFF}	SS (mV/decade)	EOT (nm)	Device specification
[35]	0.75	10^{-7}	10^{-16}	10^{9}	26	1	Si TFET
[36]	0.4	$18*10^{-6}$	$6*10^{-15}$	10^{9}	20	0.682	FD SOI –TFET
[37]	1	10^{-7}	10^{-15}	10^{8}	------	1	Si LTFET
[38]	0.5	10^{-4}	10^{-12}	10^{8}	14	0.5	III-V heterojunction TFET
[39]	-1	------	------	------	27-56	2-4	Cylindrical gate TFET
Proposed work	0.5	$2.12*10^{-5}$	$1.09*10^{-13}$	$2*10^{9}$	21	0.57	Ge sourcebased LTFET

9. Conclusions

The papers investigated the performance of the heterojunction L-Tunnel Field Effect Transistor (LTFET) with different engineering techniques such as bandgap engineering, pocket engineering, work-function engineering, and gate dielectric engineering, respectively. The proposed Ge-source L-TFET device with n-type pocket offers ON-state current of $2.12*10^{-5}$ Aμm^{-1}, OFF-state current of $1.09*10^{-13}$ Aμm^{-1}, current ratio of $2*10^{8}$, SS of 21 mV/decade and the threshold voltage of 0.26 V and compared to the conventional Si/Ge source L-shaped TFETs without pocket simulation result. The pocket engineering techniques suppress the leakage without degrading the ON current and SS of the proposed device. All the simulation are done by using Sentaurus TCAD simulator. The proposed device can be used to develop low-power switching devices.

References:

1. M. S. Lundstrom, "The MOSFET revisited: Device physics and modeling at the nanoscale", *Proc. IEEE,* pp. 1–3, 2006.

2. T. Sakurai, "Perspectives of low-power VLSI's", *IEICE Trans. Electron.*, vol. E87-C, no. 4, pp. 429–437, 2004.

3. S. Chander, S. K. Sinha, S. Kumar, P. K. Singh, K. Baral, K. Singh and S. Jit, "Temperature analysis of Ge/Si heterojunction SOI-tunnel FET", *Superlattices and Microstructures*, vol. *110*, pp. 162-170, 2017.

4. D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur and H. S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies", *Proc. IEEE*, vol. 89, no. 3, pp. 259–287, 2001.

5. S. K. Sinha and S Chander, "Investigation of DC Performance of Ge-Source Pocket Silicon-on-Insulator Tunnel Field Effect Transistor in Nano Regime", *Inderscience, International Journal of Nanoparticles*, Vol. 13, No. 1, pp. 13-20, 2021.

6. R. Chaudhary, A. Sharma, S. Sinha, J. Yadav, R. Sharma, R. Mukhiya and V. K. Khanna, "Fabrication and characterisation of Al gate n-metal–oxide–semiconductor field-effect transistor, on-chip fabricated with silicon nitride ion-sensitive field-effect transistor", *IET Computers & Digital Techniques*, vol. 10, no. 5, pp. 268-272, 2016.

7. I. A. Pindoo, S. K. Sinha and S. Chander, "Improvement of Electrical Characteristics of SiGe Source Based Tunnel FET Device", *Springer, Silicon*, Vol. 13, No. 9, pp. 3209-3215, 2021.

8. S. M. Turkane and A. K. Kureshi, "Review of tunnel field effect transistor (TFET)", *International Journal of Applied Engineering Research*, vol. 11, no. 7, pp. 4922-4929, 2016.

9. M. Patnala, A. Yadav, J. Williams, A. Gopinath, B. Nutter, T. Ytterdal, and M. Rizkalla, "Low power-high speed performance of 8T static RAM cell within GaN TFET, FinFET, and GNRFET technologies–A review", *Solid-State Electronics*, pp. *163*, pp. 107665, 2020.

10. B. Raad, K. Nigam, D. Sharma and P. Kondekar, "Dielectric and work function engineered TFET for ambipolar suppression and RF performance enhancement*", Electronics Letters,*vol. 52, no. 9, pp. 770-772, 2016.

11. G.V. Luong, K. Narimani, A.T. Tiedemann, P. Bernardy, S. Trellenkamp, Q.T. Zhao and S. Mantl, "Complementary Strained Si GAA Nanowire TFET Inverter With Suppressed Ambipolarity", *IEEE Electron Device Letter,* vol. 37, no. 8, pp. 950-953, 2016.

12. C. Anghel, P. Chilagani, A. Amara and A. Vladimirescu, "Tunnel field effect transistor with increased ON current, low-k spacer and high-k dielectric", *Applied Physics Lett.,* vol. 6, no. 12, pp. 122104-1–122104-3, 2010.

13. G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros , R. Kotlyar, W.K. Liu, D., Metz, M. Lubyshev, N. Mukherjee and P. Oakey, "Fabrication, characterization, and physics of III-V heterojunction tunneling field effect transistors (H-TFET) for steep subthreshold swing", *Proc. IEEE IEDM,* pp. 1–4, 2011.

14. R. Jhaveri, V. Nagavarapu and J. C. S. Woo, "Effect of pocket doping and annealing schemes on the source-pocket tunnel field-effect transistor", *IEEE Trans. Electron Devices,* vol. 58, no. 1, pp. 80-86, 2010.

15. G. Rupam, B. Brinda and B. Srimanta, "Effect of scaling on noise in circular gate TFET and its application as a digital inverter", *Microelectronics Journal,* vol. 53, pp. 16-24, 2016.

16. W. Li, L. Hongxia, W. Shulong, C. Shupeng and Y. Zhaonian, "Design of High Performance Si/SiGe heterojunction tunneling FETs with a T-shaped gate", *Nanoscale Res Lett,* vol. 12, pp. 198, 2017.

17. Y. Zhaonian, "Tunnel field-effect transistor with an L-shaped gate", *IEEE Electron Device Letters,* vol., 37, pp.839–842, 2016.

18. I. A. Pindoo and S. K. Sinha, "Increased sensitivity of biosensors using evolutionary algorithm for bio-medical applications", *Radioelectronics and Communications Systems*, vol. 63, no.6, pp. 308-318, 2020.

19. K. B. Parizi, N. Peyvast, B. K. Mousavi, S. Mohajerzadeh and M. Fathipour, "Schottky barrier nano-MOSFET with an asymmetrically oxidized source/drain structure", *Solid-State Electron.* vol. 54, no. 1, pp. 48-51, 2010.

20. N. Damrongplasit, S. H. Kim and T. J. K. Liu, "Study of random dopant fluctuation induced variability in the raised-Ge-source TFET", *IEEE electron device letters*, vol. *34, no.* 2, pp. 184-186, 2013.

21. S. W. Kim, W. Y. Choi, M. C. Sun, H. W. Kim, and B. G. Park, "Design guideline of Si-based L-shaped tunneling field-effect transistors", *Japanese Journal of Applied Physics*, vol. *51, no.* 6S, pp. 06FE09, 2012.

22. S. Kumar, K. S. Singh, K. Nigam, V. A. Tikkiwal and B. V. Tikkiwal, "Dual-material dual-oxide double-gate TFET for improvement in DC characteristics analog/RF and linearity performance", *Appl. Phys. A,* vol. 125, pp. 1–8, 2019.

23. B. V. Chandan, K. Nigam, D. Sharma and V. A. Tikkiwal, "A novel methodology to suppress ambipolarity and improve the electronic characteristics of polarity-based electrically doped tunnel FET", *Appl. Phys. A,* vol. 125, pp. 1-7, 2019.

24. S. Sahay and M.J. Kumar, "Controlling the drain side tunneling width to reduce ambipolar current in tunnel FETs using hetero dielectric BOX", *IEEE Trans Electron Devices,* vol. 62, no. 11, pp. 3882–3886, 2015.

25. S. Saurabh and M. J. Kumar, "Novel attributes of a dual material gate nano scale tunnel field-effect transistor", *IEEE Trans Electron Devices,* vol. 58, no. 2, pp. 404–410, 2011.

26. K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high-k gate dielectric", *IEEE Trans Electron Devices*, vol. 54, no.7, pp. 1725–1733, 2007.

27. S. Garg and S. Saurabh, "Suppression of ambipolar current in tunnel FETs using drain-pocket: proposal and analysis', *Superlattices and Microstructures,* vol. 113, pp.261–270, 2018.

28. E. O. Kane, "Theory of tunneling", *J. Appl. Phys.,* vol. 32, no.1, pp. 83-91, 1961.

29. A. C. Seabaugh and Q. Zhang, “Low-voltage tunnel transistors for beyond CMOS logic”, *Proc. IEEE*, vol. 98, no. 12, pp. 2095-2110, 2010.

30. S. H. Kim, H. Kam, C. Hu and T. J. K. Liu, “Germanium-source tunnel field effect transistors with record high ION/IOFF”, *VLSI SymposiumTech. Digest*, pp. 178–179, 2009.

31. S. Chander, S. Baishya, S. K. Sinha, S. Kumar, P. Singh, K. Baral, M. Tripathy, A. Singh and S. Jit, “Two-dimensional analytical modeling for electrical characteristics of Ge/Si SOI-tunnel FinFETs,” Elsevier, Superlattices and Microstructures vol. 131,pp.30-39, 2019.

32. J. Yipeng, W. Kangliang, W. Taihuan, D. Gang and L. Xiaoyan “Comparison of band-to-band tunneling odels in Si and Si—Ge junctions”, *Journal of Semiconductors,* vol. 34, no.9, pp. 092002, 2013.

33. S. D. U. Guide, version K-2015.06, 2015.

34. K. H. Kao, A. Verhulst, W. Vandenberghe, B. Soree, G. Groeseneken and K. D. Meyer, Direct and indirect band-to-band tunneling in germanium-based TFETs," *Electron Devices*, vol. 59, pp. 292-301, 2012.

35. H. W. Kim and D. Kwon, “Steep Switching Characteristics of L-Shaped Tunnel FET With Doping Engineering”, *IEEE Journal of the Electron Devices Society*, vol. 9, pp. 359-364, 2021.

36. S. Chander, B. Bhowmick and S. Baishya, “Heterojunction fully depleted SOI-TFET with oxide/source overlap”, *Superlattices and Microstructures*, vol. 86, pp. 43-50, 2015.

37. J. H. Kim, H. W. Kim, Y. S. Song, S. Kim and G. Kim, “Analysis of Current Variation with Work Function Variation in L-Shaped Tunnel-Field Effect Transistor”, *Micromachines*, vol. 11, no. 8, pp. 780, 2020.

38. P. K. Dubey and B. K. Kaushik, “T-shaped III-V heterojunction tunneling field-effect transistor”, *IEEE Transactions on Electron Devices*, vol. 64, no. 8, pp. 3120-3125, 2017.

39. S. Dash and G. P. Mishra, “A 2D analytical cylindrical gate tunnel FET (CG-TFET) model: impact of shortest tunneling distance”, *Advances in Natural Sciences: Nanoscience and Nanotechnology*, vol. 6, no. 3, pp. 035005, 2015.