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Research Article

Keywords: Thermal noise, Thermal contact resistance, Ambient temperature, Lattice temperature, Electrothermal, Drain current, Phonons

Posted Date: December 20th, 2021

DOI: https://doi.org/10.21203/rs.3.rs-816886/v1

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A Rigorous Analysis of Self-Heating Effects in Nanoscale Dielectric Pocket Double-Gate-All-Around (DP-DGAA) MOSFETs

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Abstract—Dielectric Pocket Double-Gate-All-Around (DP-DGAA) MOSFETs are one of the preferred choices for ULSI applications because of significantly low off-current, reduced power dissipation, and high immunity to short channel effect. However, DP-DGAA MOSFETs suffer from self-heating owing to the unavailability of proper heat take-out paths. In this paper, the electrothermal (ET) simulations have been performed with hydrodynamic and thermodynamic transport models to analyze the self-heating effects (SHEs) in DP-DGAA MOSFETs. The electrothermal characteristics against various device parameters such as spacer length, device thickness, thermal contact resistance, and drain voltage have been investigated. The effect of SHE on the drive current has also been evaluated. Further, the impact of thermal contact resistance and ambient temperature variations of the device on SHE and thermal noise have been analyzed using Sentaurus TCAD simulator.

Index Terms—Thermal noise; Thermal contact resistance; Ambient temperature; Lattice temperature; Electrothermal; Drain current; Phonons
1. Introduction

In recent years, information and communication technologies have been developed aggressively with the sustainable progress in MOS technology. The last decade’s micrometre (μm) technology of field-effect transistors (FETs) have now been replaced with the nanometre technology node delivering high computing speed for smaller device dimensions [1]. But, the downscaling of device dimensions is achieved at the cost of degraded short channel effects immunity (SCEs) [2-3], which restrain the goal of achieving high performance with smaller power dissipation, especially in Off-state. Multigate MOS structures provide better control over the channel, among which, Gate-All-Around (GAA) structures are seen as the most competent one [4-6]. They exhibit superb electrostatic control over the channel, less influenced by short channel effects (SCEs), and superior packing density with steep subthreshold characteristics [7-8]. However, in our previous investigation, the Dielectric Pocket (DP) GAA and Double-gate-all-around (DGAA) have been shown as potential candidates to achieve high performance and ultra-low power dissipation due to reduced off-state current [9-10].

Nowadays, high power dissipation causes the electronic chips with high MOS density to suffer from self-heating problems. With the shrinking in device dimensions, there is unbalanced scaling of device parameters and supply voltages that cause high electric fields (~1MV/cm) near the channel-drain junction [11]. This high electric field energizes the charge carriers to higher energy levels, and hence they become hot carriers. An ample number of hot carriers in the channel provoke the self-heating problem in the device [12-16]. The self-heating effects (SHEs) severely deteriorate the device performance owing to mobility reduction and must be investigated [17]. The saturation drain current is also affected by the SHEs significantly, which results in mitigated thermal noise effects [18-19]. Further, electrothermal issues like the wide variation in ambient temperature and increase in hot-carrier injection tend to degrade device performance.
Various researchers have investigated the self-heating problem in silicon-based GAA MOSFETs [20-23]. Park et al. [20] studied the electrothermal (ET) effects and degradation of drain current in GAA MOSFETs with vertically stacked multiple silicon-based nanowire channels. An ultrafast high-resolution thermoreflectance (TR) imaging technique was reported by Shin et al. [21] for investigating the increase in local surface temperature and high-resolution measurements by heating and cooling at constant time. The device performance degradation by the electrothermal (ET) conductivity was studied by Kompala et al. [22] and attributed to the lower thermal conductivity of gate oxide, spacer region material, and higher thermal contact resistance ($R_{tc}$). Pala et al. [23] studied the effect of self-heating with quantum confinement effects (QCEs) in the Tri-Gate transistor. To date, the influence of ambient temperature ($T_{Amb}$), drain voltage ($V_{DS}$), and device parameters such as spacer length, spacer conductivity, device length, and thermal contact resistance on carrier temperature, lattice temperature, along with its effect on thermal noise has not been investigated in detail for DP-DGAA MOSFETs.

In the present work, a detailed study of variation in the lattice temperature and carrier temperature-induced degradation against ambient temperature ($T_{Amb}$), drain voltage ($V_{DS}$), and various device parameters of DP-DGAA MOSFET using electrothermal (ET) simulations have been carried out. The work also includes the effect of self-heating on thermal noise. The remaining part of this work is ordered as follows: Section II reports the device architecture and models used for simulation. Results and discussion have been described in section III, which includes the heat transport and thermal behavior of DP-DGAA MOSFETs with various device parameters, and at last, section IV summarizes the work in brief.

2. Device Simulation Setup with Calibration

The three-dimensional (3D) schematic of DP-DGAA MOSFET for the simulation-based investigation is presented in Fig. 1. In this configuration, the silicon-based nanotube channel
region has been covered by thin oxide layers and inserted between inner and outer gates. On the both gates, contact metal is used named Tungsten Nitride with a 4.7eV work function [24]. The contact metal of source and drain are used as Molybdenum (Mo). All other physical parameters of DP-DGAA MOSFET design for simulations are listed in Table I, and the thermal parameters used for electrothermal (ET) simulations are listed in Table II. The Sentaurus 3D TCAD device simulator [25] has been used to simulate the proposed DP-DGAA device structure. Hydrodynamic (HD) and Thermodynamic (TH) transport models have been used for carrier and heat transport respectively. The density gradient model is applied for solving the quantum confinement effects (QCEs) of the charge carriers in the channel region. For the electrothermal (ET) simulations, the all-dependent thermal conductivity ($T_C$) model [11,25] is applied for Silicon. The Lombardi (CVT), Philips unified mobility, and high field saturation models have been used to simulate the temperature, carrier concentration, and carrier-to-carrier scattering dependent carrier mobility. The constant thermal contact resistance value at an isothermal ambient temperature of 300K has been used for device terminals’ thermal boundary conditions. In Fig. 2, the simulation models are calibrated with the experimental data from Refs. [26] and [11].

3. Results and Discussion

A. Lattice and Carrier Temperature Variations

The carrier energy significantly increases with an increase in the drain-to-source voltage ($V_{DS}$), and consequently, there is an increase in equivalent carrier temperature ($T_C$). The carriers with high energy suffer from scattering with lattice atoms, and the heat is transferred to the crystal lattice. Thus, the carrier temperature ($T_C$) is significantly higher than the lattice temperature ($T_L$) and ambient temperature ($T_A$) (i.e., $T_C$ $>$ $T_L$ $>$ $T_A$). In Fig. 3, the variation of the optimum value of lattice and carrier temperature against $V_{DS}$ at gate-to-source voltage ($V_{GS}$) = 1V is
shown. The optimum carrier temperature ($T_{C_{\text{max}}}$) and the optimum lattice temperature ($T_{L_{\text{max}}}$) increases slowly against $V_{DS}$ up to 0.1V because of low-field transport ($LFT$) [11]. However, above 0.1V, the $T_{L_{\text{max}}}$ and $T_{C_{\text{max}}}$ increase more significantly from 304K to 420.7K and 382K to 2694.3K because of high-field transport ($HFT$) [11]. Hence, the carrier temperature enhances, and carriers go through energy relaxation with optical phonons. Fig. 4 demonstrates the variation of the maximum lattice temperature ($T_{L_{\text{max}}}$) and maximum electron temperature ($T_{C_{\text{max}}}$) versus different spacer lengths ($L_{SP}$) at $V_{DS} = V_{GS} = 1V$. The up-scaling of spacer length ($L_{SP}$) with a fixed channel length results in extended gaps between source and drain contacts with the channel, and casts two effects, namely: (a) the electric field gets weaker along the channel length at constant $V_{DS}$ and $V_{GS}$. Consequently, the energy of charge carriers and $T_{C_{\text{max}}}$ are reduced significantly. (b) decrease in heat dissipation through the cooling sinks (metallic contacts of S/D) of the device, which causes rise in maximum lattice temperature ($T_{L_{\text{max}}}$). It can be observed in Fig. 4 that when the $L_{SP}$ is increased from 5nm to 25nm, the $T_{L_{\text{max}}}$ increases from 332.9K to 420.7K (~26.3% increase), and $T_{C_{\text{max}}}$ decreases from 2962.6K to 2694.3K (~9.05% decrease). The plot in Fig. 5 shows the variation of $T_{L}$ and $T_{C}$ along the device length at $V_{DS} = V_{GS} = 1V$. The $T_{L}$ varies from 392.4K to 415.7K, with a 420.68K peak value in the drain region. On the other hand, the $T_{C}$ varies from 423.8K to 648.4K, with a 2676.9K peak value at the interface of channel and drain.

**B. Output Characteristics and Thermal Noise under SHE**

The impact of self-heating effects on the output characteristics is shown in Fig.6. Self-heating causes the frequent scattering of hot carriers near the drain side, owing to which populated carriers suffer from degraded charge carrier mobility in the channel region. The degradation results in the downfall of drain saturation current with the increase of $V_{DS}$ for the given value of $V_{GS}$. According to Fig. 6, the current reduces under self-heating effect (SHE) approximately by 9.93% at $V_{GS} = V_{DS} = 1V$ and $t_{si} = 6nm$ in DP-DGAA MOSFET, whereas for $t_{si} = 8nm$ the
reduction is 12.66% owing to the increased drain current and enhancement of phonon scattering in the channel region. The plot in Fig. 7 depicts the variation of thermal noise in the channel with SHEs and without SHEs against $V_{DS}$ for $V_{GS} = 1V$. In general, thermal noise depends on the conductivity of the channel. However, under the SHEs, channel conductivity mitigates significantly due to hot carrier scattering, and thermal noise goes down by 74.7% compared to normal conditions at $V_{DS} = 1V$ and $t_{si} = 6nm$. For $t_{si} = 8nm$, the thermal noise goes down by 77.12% as compared to the case of without SHEs.

C. Effect of Thermal Contact Resistance ($R_{tc}$) on SHE

Fig. 8 shows the variation of lattice temperature against device length for $V_{DS}$ and $V_{GS} = 1V$ for different contact thermal resistances ($R_{tc}$). Lattice temperature is the maximum in the drain region, i.e., 420.68K owing to the highest lattice scattering of hot carriers for $R_{tc} = 5 \times 10^{-5} \text{cm}^2 \text{KW}^{-1}$. The lattice temperature also depends on $R_{tc}$. Low $R_{tc}$ allows dissipation of more heat from the device and helps to decrease the lattice temperature. When $R_{tc}$ reduces from $5 \times 10^{-5} \text{cm}^2 \text{KW}^{-1}$ to $1 \times 10^{-5} \text{cm}^2 \text{KW}^{-1}$, the maximum lattice temperature of the drain sinks from 420.67K to 338.53K.

Fig. 9 shows the variation of maximum lattice temperature against thermal conductivity of spacer for $V_{DS}$ and $V_{GS} = 1V$ for different contact thermal resistances ($R_{tc}$). A high conductive spacer provides the precise heat flow path from the device. Fig. 9 verifies that with the increase of the thermal conductivity of the spacer from 0.014 to 0.185W/K-cm at $R_{tc} = 5 \times 10^{-5} \text{cm}^2 \text{KW}^{-1}$, the lattice temperature decreases from 420.7K to 409K. The variation of drain current against $V_{DS}$ at $V_{GS} = 1$ is displayed in Fig. 10. The high value of contact thermal resistance ($R_{tc}$) does not easily pass the heat from the device and provokes the high phonon scattering, and thus deterioration in mobility and drain saturation current occurs. Further, the downfall of around 7.2% in drain saturation current at $V_{DS} = 1V$ with the increase in $R_{tc}$ from $1 \times 10^{-5} \text{cm}^2 \text{KW}^{-1}$ to $5 \times 10^{-5} \text{cm}^2 \text{KW}^{-1}$ can be noticed in the figure. Fig. 11 depicts the variation of thermal noise against $V_{DS}$ at $V_{GS} = 1V$ for different values of $R_{tc}$. The increasing amount of $V_{DS}$ deteriorates the
channel conductance, and thermal noise is diminished accordingly. A lower value of thermal contact resistance ($R_{tc}$) improves the drain current and channel conductivity due to less phonon scattering. An enhanced amount of channel conductivity increases the thermal noise in the channel. As $R_{tc}$ increases from $1 \times 10^{-5}$ cm$^2$KW$^{-1}$ to $5 \times 10^{-5}$ cm$^2$KW$^{-1}$, thermal noise varies from $2 \times 10^{-25}$ A$^2$/Hz to $6.6 \times 10^{-26}$ A$^2$/Hz as shown in the figure.

### D. Effect of Ambient Temperature Variations

Fig. 12 demonstrates the variation of the maximum lattice temperature ($T_{L_{max}}$) versus ambient temperature ($T_{Amb}$) for various values of $R_{tc}$. The $T_{L_{max}}$ increases from 420.7K to 517.6K (~23.03% increase) with the rise of $T_{Amb}$ from 300K to 400K for $R_{th}=5 \times 10^{-5}$ cm$^2$KW$^{-1}$. Fig. 13 shows the variation of the drain current ($I_D$) versus ambient temperature ($T_{Amb}$) for different values of $R_{tc}$. At $R_{tc}= 5 \times 10^{-5}$ cm$^2$KW$^{-1}$, the $I_D$ decreases from 137μA to 126μA (~8.02% decrease) for rise in $T_{Amb}$ from 300K to 400K as the lateral electric field degrades the carrier mobility. The variation of thermal noise against ambient temperature at $V_{GS} = V_{DS} = 1$V for different values of $R_{tc}$ is depicted in Fig. 14. It is to be noted that thermal noise is indirectly related to the ambient temperature. At $R_{tc} = 5 \times 10^{-5}$, with the variation in $T_{Amb}$ from 300K to 400K, the thermal noise increases by approximately 10.05%. Fig. 15 demonstrates the cutline plot of the variation in lattice temperature ($T_L$) against device channel length at $V_{GS} = V_{DS} = 1$V for various $T_{Amb}$ values (300K to 400K in a step of 20K). The drain lattice temperature ($T_L$) is observed to be higher than the channel and source regions because the large electric field in the drain region renders high probability of carrier scattering near the drain region. However, the $T_L$ increases with an increase in $T_{Amb}$.

### 4. Conclusion

In this paper, the self-heating effects (SHEs) have been investigated in the Dielectric Pocket Double-Gate-All-Around (DP-DGAA) MOSFETs, and its implications are observed on
Thermal Noise. Because of SHEs, the saturation drain current reduces by 9.93% when the channel thickness is 6nm, however when the channel thickness is increased to 8nm the decrement in the current is found to be 12.66%. The thermal noise decreases from 74.7% to 77.12% at the same channel thickness variation. The lattice temperature increases with increasing thermal contact resistance; on the other hand, the drain current and thermal noise significantly reduce upon increasing the thermal contact resistance. The lattice temperature and thermal noise also increase by increasing the ambient temperature, but the drain current reduces monotonously. Moreover, the maximum lattice temperature increases with extension in source and drain length, but the electron temperature is reduced significantly. Thus, source and drain extension length and thermal contact resistance can be used as design parameters to mitigate the effects of self-heating.

**Declarations**

Funding: Not applicable

Conflicts of interest/Competing interests: The authors declare that there is no conflict of interest regarding the publication of this paper.

Availability of data and material (data transparency): Not applicable

Code availability (software application or custom code): Not applicable

Authors' contributions: All authors have made equal contributions to the conception, design, analysis and interpretation of results in the manuscript. The authors have been involved in drafting the manuscript critically for important intellectual content; and have given unanimous approval of the version to be published. Each author has participated sufficiently in the work to take public responsibility for appropriate portions of the content. All the authors have read and approved the final manuscript.

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https://doi.org/10.1063/1.2349313.

USA, 2016.

effect transistor with core-shell gate stacks for enhanced high-performance operation
https://doi.org/10.1021/nl202563s.
Table-1: Device parameters used for DP-DGAA MOSFET simulation.

<table>
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<th>SI. No.</th>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>1</td>
<td>Channel length</td>
<td>( L_C )</td>
<td>20 nm</td>
</tr>
<tr>
<td>2</td>
<td>Source/Drain doping</td>
<td>( N_D )</td>
<td>( 10^{20} \text{ cm}^{-3} )</td>
</tr>
<tr>
<td>3</td>
<td>Channel doping</td>
<td>( N_A )</td>
<td>( 10^{15} \text{ cm}^{-3} )</td>
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<tr>
<td>4</td>
<td>Oxide thickness</td>
<td>( t_{ox} )</td>
<td>1 nm</td>
</tr>
<tr>
<td>5</td>
<td>Channel thickness</td>
<td>( t_{si} )</td>
<td>6 nm, 8 nm</td>
</tr>
<tr>
<td>6</td>
<td>Inner gate radius</td>
<td>( T_c )</td>
<td>4 nm</td>
</tr>
<tr>
<td>7</td>
<td>Metal work-function</td>
<td>( \phi_M )</td>
<td>4.7 eV</td>
</tr>
<tr>
<td>8</td>
<td>Dielectric pocket length</td>
<td>( D_P_L )</td>
<td>4 nm</td>
</tr>
<tr>
<td>9</td>
<td>Dielectric pocket thickness</td>
<td>( D_P_D )</td>
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<tr>
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</tr>
<tr>
<td>11</td>
<td>Source/Drain Contact Length</td>
<td>( L_{SC}/L_{DC} )</td>
<td>5 nm</td>
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<tr>
<td>12</td>
<td>Thermal Contact Resistance</td>
<td>( R_{tc} )</td>
<td>( 1 \times 10^{-5} - 1 \times 10^{-4} \text{ cm}^2\text{KW}^{-1} )</td>
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</table>

Table-2: Thermal conductivity parameters used for device simulation using Ref. [11,14].

<table>
<thead>
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<th>Thermal conductivity (W/K-cm)</th>
</tr>
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<tr>
<td>1</td>
<td>Channel Region (Si)</td>
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<tr>
<td>2</td>
<td>Source/Drain Region (Si)</td>
<td>0.62</td>
</tr>
<tr>
<td>3</td>
<td>SiO(_2)</td>
<td>0.014</td>
</tr>
<tr>
<td>4</td>
<td>Si(_3)N(_4)</td>
<td>0.185</td>
</tr>
</tbody>
</table>
Fig. 1: (a) Three-dimensional (3D) schematic of DP-DGAA MOSFET, (b) Two-dimensional (2D) cross-sectional schematic view of DP-DGAA MOSFET.
Fig. 2: Comparison of transfer characteristics of 3D TCAD simulation with measured experimental data Ref. [26] for DGAA MOSFET with the same device parameters of Ref. [26]. and (b) Ref. [11] for DGAA MOSFET with the same device parameters.
Fig. 3: Variation of peak value of lattice and electron temperature (\(T_{L_{\text{max}}}\) and \(T_{C_{\text{max}}}\)) versus drain-to-source voltage (\(V_{DS}\))

Fig. 4: Variation of peak value of lattice and electron temperature (\(T_{L_{\text{max}}}\) and \(T_{C_{\text{max}}}\)) against spacer length (\(L_{SP}\))
Fig. 5: Variation of lattice and electron temperature ($T_L$ and $T_C$) along the device length (nm)

Fig. 6: Comparison of output characteristics of DP-DGAA MOSFET versus $V_{DS}$ with SHE and without SHE for different channel thickness ($t_{si}$)
Fig. 7: Comparison of thermal noise of DP-DGAA MOSFET versus $V_{DS}$ with SHE and without SHE for different channel thicknesses ($t_{si}$)

Fig. 8: Variation of lattice temperature ($T_L$) along the device length (nm) for various values of thermal contact resistances ($R_{tc}$)
Fig. 9: Variation of peak value of lattice temperature versus changing thermal conductivity of spacer for various values of $R_{tc}$

Fig. 10: Variation of the output characteristics against drain bias for different values of $R_{tc}$
Fig. 11: Variation of the thermal noise against drain bias for different values of $R_{tc}

0.0 0.2 0.4 0.6 0.8 1.0

-1.0x10^{-24} -2.0x10^{-24} -3.0x10^{-24} -4.0x10^{-24} -5.0x10^{-24}

0.0 1.0x10^{-24} 2.0x10^{-24} 3.0x10^{-24} 4.0x10^{-24}

$N_t = N_{th} = 6nm$ $t_{ox} = 1nm$

$V_{GS} = 1 V$

Fig. 12: Variation of the peak value of lattice temperature ('Hot Spot') against increasing ambient temperature ($T_{Amb}$) for various values of $R_{tc}$

$R_{tc} = 1x10^{-5} cm^2 K W^{-1}$

$R_{tc} = 5x10^{-5} cm^2 K W^{-1}$

$R_{tc} = 1x10^{-4} cm^2 K W^{-1}$

$V_{DS} = 1 V$ $V_{GS} = 1 V$

$T_{Amb}$
Fig. 13: Variation of the drain current against increasing ambient temperature ($T_{Amb}$) for various values of $R_{tc}$.

Fig. 14: Variation of the thermal noise against ambient temperature ($T_{Amb}$) for various values of $R_{tc}$. 
Fig. 15: Variation of lattice temperature ($T_L$) along device channel length (nm) for different values of ambient temperature ($T_{Amb}$).

- $t_d = 6$ nm, $t_{ox} = 1$ nm
- $R_{tc} = 5 \times 10^{-5}$ cm$^2$ K W$^{-1}$
- $V_{DS} = 1$ V, $V_{GS} = 1$ V

Increasing Ambient Temperature ($T_{Amb}$) from 300K to 400K in interval of 20K