Supplementary Information

All-solid-state Ion Synaptic Transistor for Wafer-scale Integration with Electrolyte of a Nanoscale Thickness

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1. Fabrication procedure for all-solid-state wafer-scale pEGST implemented on a silicon channel

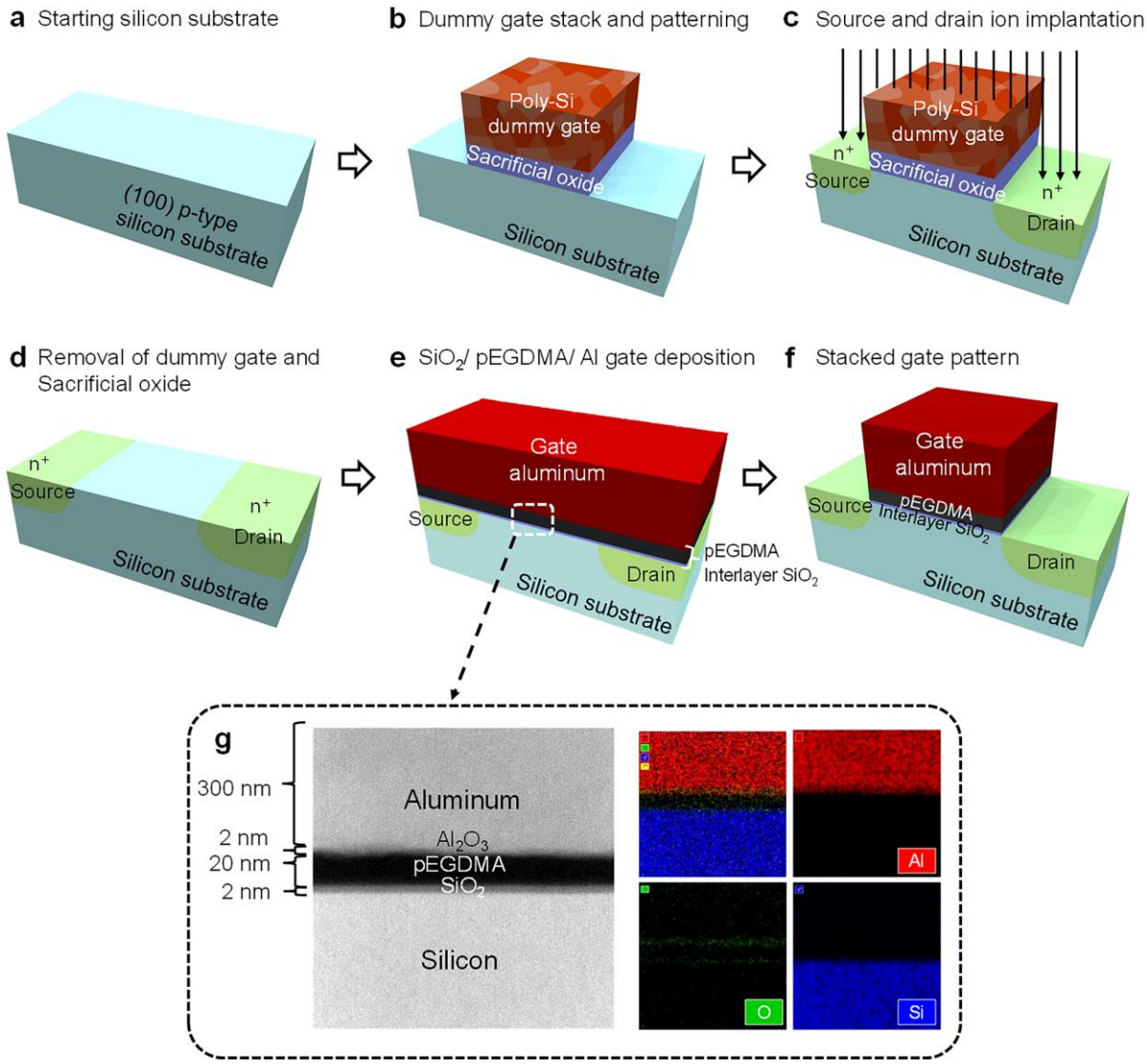

Figure S1| Schematics of the fabrication procedure for the all-solid-state polymer electrolyte-gated synaptic transistor (pEGST) integrated on a silicon channel with wafer-scale and a gate stack composed of aluminum/ Al_2O_3/pEGDMA/ SiO_2 layers.

- Bulk silicon wafer ((100), p-type, 1-10 Ω·cm)
- Sacrificial oxidation (T_{ox} = 50 nm)
- Si_3N_4 deposition by LPCVD
- Channel definition by photo-lithography and channel stop implantation
- LOCal oxidation of Silicon (LOCOS) for cell to cell isolation
- Si_3N_4 removal
- Poly-silicon deposition by LPCVD for dummy gate (T_{poly} = 250 nm)
- Source and drain area photolithography and implantation (P, 5×10^{15} cm^{-2}, 50 keV)
- Removal of poly-silicon dummy gate
- Body contact definition by photo-lithography and subsequent implantation (B, 5×10^{15} cm^{-2}, 20 keV)
- Standard cleaning and gate oxidation (2 nm)
- pEGDMA deposition by initiated chemical vapor deposition (iCVD) (20 nm)
- Gate aluminum deposition by DC magnetron sputter (300 nm)
- Gate definition by photo-lithography and gate etching

Figure S2| Step-by-step fabrication process flow for the pEGST.

The fabrication process flow of the pEGST is illustrated in Figure S1. Considering the thermal budget of the metal gate and polymer electrolyte, the pEGST was fabricated on an p-type (100) 4-inch bulk silicon wafer (**Figure S1 a**) by using a gate-last process. A sacrificial oxide of 50 nm served as a buffer layer and a Si_3N_4 of 170 nm layer were sequentially deposited prior to channel definition. A field oxide of 1 μm was thermally grown for electrical isolation on each device using local oxidation of silicon (LOCOS). Then, the remaining Si_3N_4 was etched away by hot phosphoric acid at 155 ºC. Afterwards, a dummy gate of poly-crystalline silicon (poly-Si) capable of protecting the channel from source and drain (S/D) ion implantation was deposited by low pressure chemical vapor deposition (LPCVD) and patterned by conventional photo-lithography and etching (**Figure S1 b**). The S/D regions were doped by phosphorus (P) implantation with a dose of 5×10^{15} cm^{-2} and energy of 50 keV. After the removal of the dummy gate (**Figure S1 c**), another implantation was performed with an extra mask for the back-biasing, was performed with boron (B) ions with a dose of 5×10^{15} cm^{-2} and energy of 20 keV.

Both dopants were simultaneously activated at 1000 °C for 7 s. In this way, the S/D junction of n^+-p and the ohmic body contact of p^+-p (not illustrated in **Figure S1 d)** were formed**.**

Actual gate stacks composed of an interfacial SiO_2, hydrogen-doped pEGDMA and aluminum were sequentially deposited with thicknesses of 2 nm (T_{SiO2}), 20 nm (T_{pEGDMA}) and 300 nm ($T_{aluminum}$), respectively. The interfacial thermal oxide was grown by thermal oxidation, the pEGDMA was deposited by initiated chemical vapor deposition (iCVD), and the Al gate was deposited by DC magnetron sputtering (**Figure S1 e**). The gate electrode with the gate dielectrics was patterned by conventional photo-lithography and etching. Specifically, the gate aluminum was etched using 'APAL-1' aluminum wet etchant, the unmasked region of the pEGDMA was removed by inductive coupled O_2 plasma ashing, and the interfacial SiO_2 was sequentially eliminated by (50:1) HF solution (**Figure S1 f**). **Figure S1 g** identified each of the gate stack layers with the aid of energy dispersive x-ray spectroscopy (EDS) mapping. **Figure S2** shows the step-by-step fabrication process flow for the pEGST.

2. Initiated chemical vapor deposition (iCVD) process for the polymer electrolyte of the pEGDMA

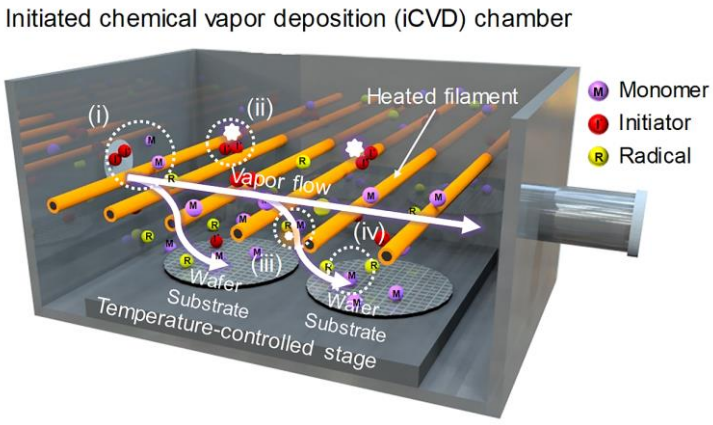

Figure S3| Schematic of the iCVD chamber for the pEGDMA electrolyte deposition.

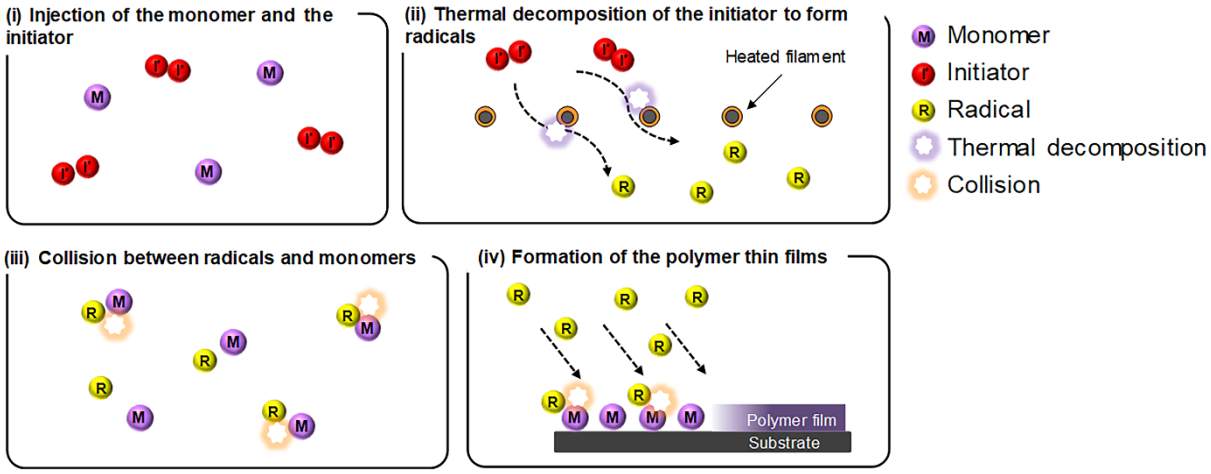

Figure S4| A brief chemical reaction in the iCVD process (i) Separated monomer and the initiator injection, (ii) Thermal decomposition of the initiator to form radicals, (iii) Collision between radicals and monomers (iv) Formation of the polymeric thin film.

It has been reported that the iCVD process supports the wafer-scale fabrication of a polymer gate dielectric transistor because of its several strengths[1]: 1) the conformal and uniform step coverage of an ultra-thin layer, even on 8-inch wafer; 2) the controllability of the ultra-thin layer, with thicknesses less than 10 nm; 3) the use of a crosslinking reaction for a dense film;

4) the stability and sustainability of the intrinsic polymer properties; and 5) a simple solvent-free and annealing-free process[2-4].

Figure S3 shows an inside-view schematic of the iCVD chamber used for polymerization of the ultra-thin and conformal film. In this work, the ethylene glycol dimethacrylate (EGDMA) monomer was polymerized to make a thin film of the poly-EGDMA (pEGDMA) for the all-solid-state electrolyte-gated synaptic transistor (pEGST). A brief summary of the iCVD polymerization is as follows (**Figure S4**): i) separated injection of monomer (EGDMA) and initiator (tert-butyl peroxide); ii) thermal decomposition of the initiator to form radicals; iii) inter-collisions between the radicals and the monomers; and iv) formation of a radical-free polymeric thin film. The properties of the iCVD polymer can be controlled over a wide range by modulating the major process parameters, such as the flux of the initiator or the monomer, the temperature of the filament, substrate temperature, and pressure in the chamber, etc. The ratio of the flow rate of the monomer and the initiator was 1:1, and the filament temperature was 130 °C for the thermal decomposition of the initiator and production of the radicals. The temperature of the substrate was maintained below 40 °C, and the chamber pressure was kept at approximately 60 mTorr by using a controller of proportional-integral-derivative (PID).

3. Temperature dependent characteristics of the pEGST

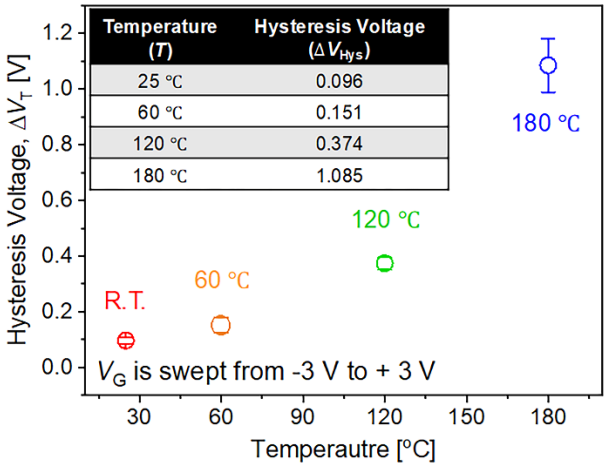

Figure S5| Temperature dependent hysteresis of the pEGST.

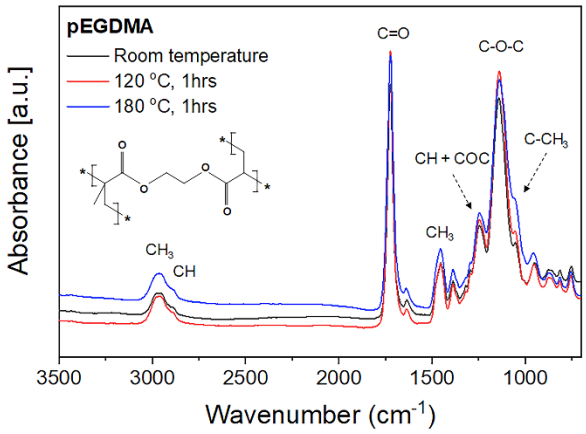

Figure S6| The pEGDMA film quality analyzed by Fourier-transform infrared (FT-IR) spectroscopy before and after high temperature treatment.

Figure S5 shows the temperature dependent hysteresis of the pEGST at various temperature (T) of 25 ºC, 60 ºC, 120 ºC, and 180 ºC. When V_G was swept from - 3 V to + 3 V, a hysteresis voltage (ΔV_T) corresponding to ΔV_T became wider as T increased. It was approximately 1 V at 180 ºC. This tendency is caused by the accelerated H^+ migration in the pEGDMA at high temperature. In **Figure S6**, it was additionally confirmed by Four transform infrared (FT-IR) spectroscopy that the chemical structure in the pEGDMA was not changed, even after high temperature treatment of 180 ºC for 1 hour.

4. Compact pEGST array with a vertical pillar structure

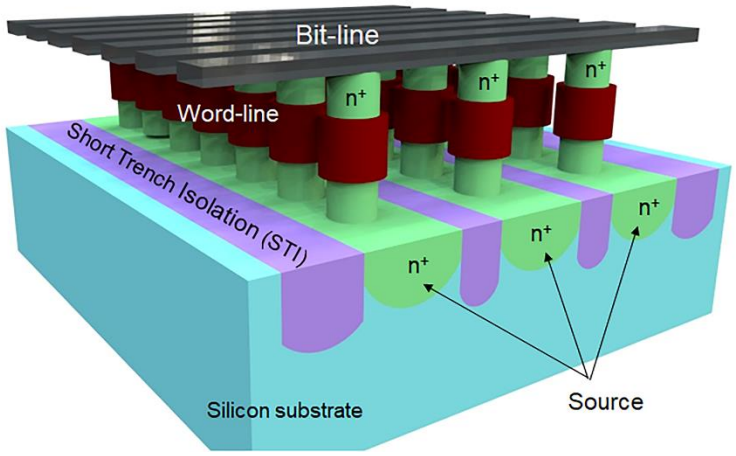

Figure S7| Overall schematic of a vertical pillar-type pEGST array.

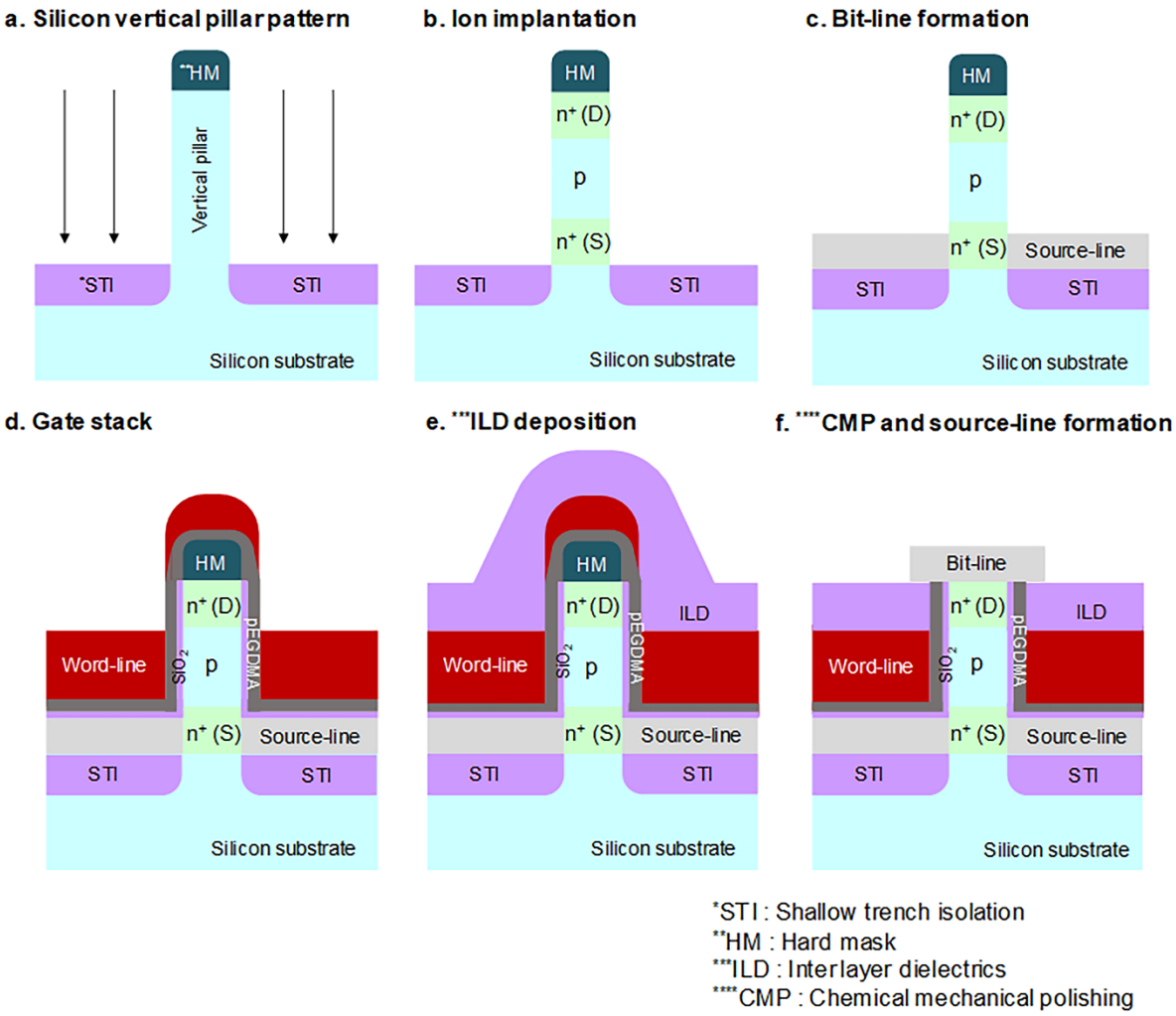

Figure S8| Fabrication procedure of the vertical pillar-type pEGST.

Figure S7 shows a schematic of a vertical pillar-type pEGST array. The proposed vertical pillar-type pEGST array can be fabricated with a solid-state conformal electrolyte film using the iCVD method. These fabrication methods can realize a large-scale neural network system with a densely packed synapse array. It can also be an optimal architecture in terms of defect-tolerance[5].

Figure S8 depicts feasible fabrication procedures for the vertical pillar-type pEGST. Firstly, a pillar-shaped silicon channel with hard mask (HM) is patterned (**Figure S8 a**). Subsequently, the source, channel, and drain are doped by iterative ion implantations, respectively with an appropriate projection range and are then activated by rapid thermal annealing (RTA) (**Figure S8 b**). Bit-line contact is formed after the ion implantations and RTA (**Figure S8 c**). The gate dielectric of SiO_2, electrolyte thin film (pEGDMA) and gate word-line are sequentially formed by thermal oxidation, iCVD and DC magnetron sputtering, respectively (**Figure S8 d**). Afterwards, another thick oxide is deposited by plasma-enhanced chemical vapor deposition (PECVD). This serves as an interlayer dielectric layer. Then, chemical mechanical polishing (CMP) is applied to etch away unwanted layers for planarization until the n^+ drain silicon is exposed. Finally, a bit-line contact is made on top of the n^+ drain (**Figure S8 e and f**).

5. Long-term durability

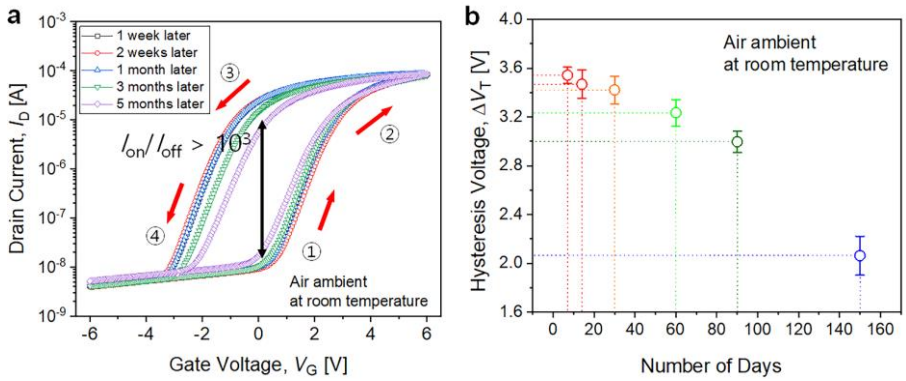

Figure S9| Long-term durability a, Change in transfer characteristics (I_D-V_G) and **b,** hysteresis voltage ($\Delta V_T = V_{T,forward} - V_{T,backward}$) over time.

Most of the electrolyte-gated synaptic transistors previously studied used ionic liquid or ionic gel-type electrolytes, which can cause chronic problems such as evaporation and contamination, as previously mentioned in the main paper. In this study, an all-solid-state polymer thin film was used as an electrolyte layer, fabricated with a reproducible and stable process. **Figure S9** shows the device durability as time goes by. Fabricated devices were even exposed to air ambient at room temperature more than 5 months, and show stable characteristics with a high on/off ratio (>10^3) at read voltage and a wide hysteresis window ($\Delta V_T = V_{T,forward}$-$V_{T,backward}$). Even after air exposure for 5 months without any passivation or protection layer, ΔV_T with a little narrowed compared to its initial value but remained at a high dynamic range (>10^3), showing more than 1000 conductance levels at a read gate voltage of 0.1 V. As a consequence, the fabricated pEGST would be attractive for a long-term durable synaptic device.

6. Depth profiling of various ions across the gate dielectrics by use of time-of-flight secondary ion mass spectrometry (ToF SIMS)

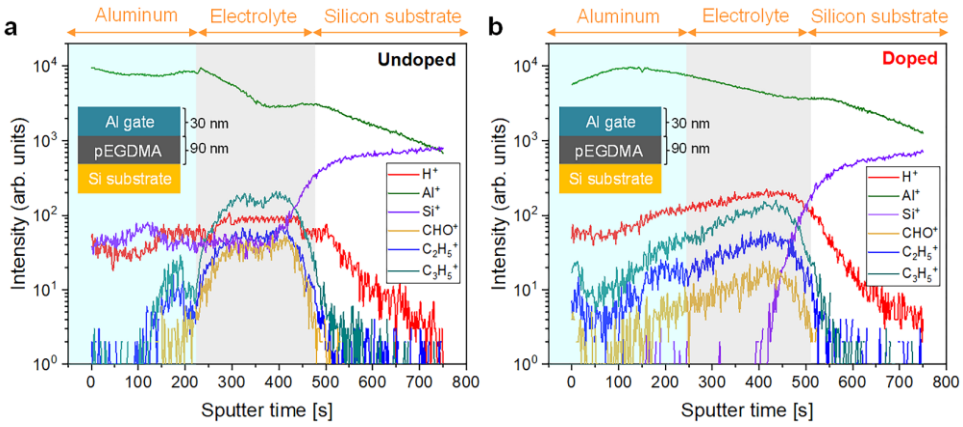

Figure S10| Ion concentration and its distribution across the polymer electrolyte **a,** with and **b,** without hydrogen doping.

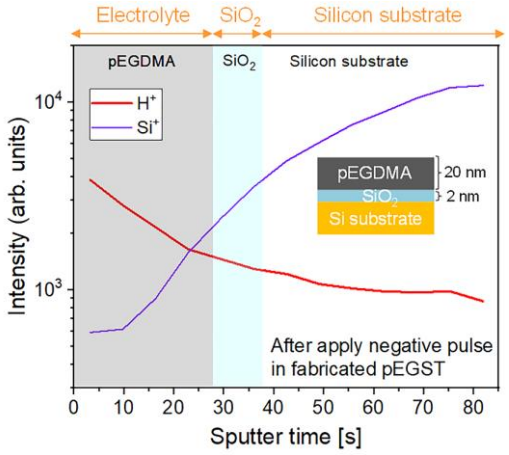

Figure S11| Depth profiling of proton concentration across the pEGDMA in the fabricated pEGST with the aid of ToF SIMS when negative gate voltage was applied.

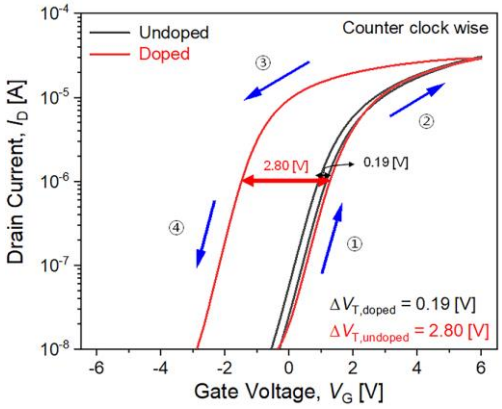

Figure S12| Transfer curve characteristics (I_D-V_G) with and without hydrogen doping. Large hysteresis can be observed only in the case of the doped electrolyte.

Figure S10 compares the ion concentration and its distribution across the polymer electrolyte, with and without proton doping. The concentration of protons (H^+) in the doped sample (experimental group) is larger than that in the undoped one (control group). **Figure S11** shows a depth profile of the proton with the negative gate voltage in the fabricated pEGST. It is confirmed that the proton concentration becomes higher toward the gate electrode, because the negative gate voltage attracts protons. Transfer curve characteristics (I_D-V_G) of the experimental group and control group are compared in **Figure S12**. The hysteresis window ($\Delta V_T = V_{T,forward} - V_{T,backward}$) was 2.80 V in the experimental group and was 0.19 V in the control group. The abovementioned data are consistent each other.

7. Gate pulse diagram, gate leakage current and energy consumption for weight update

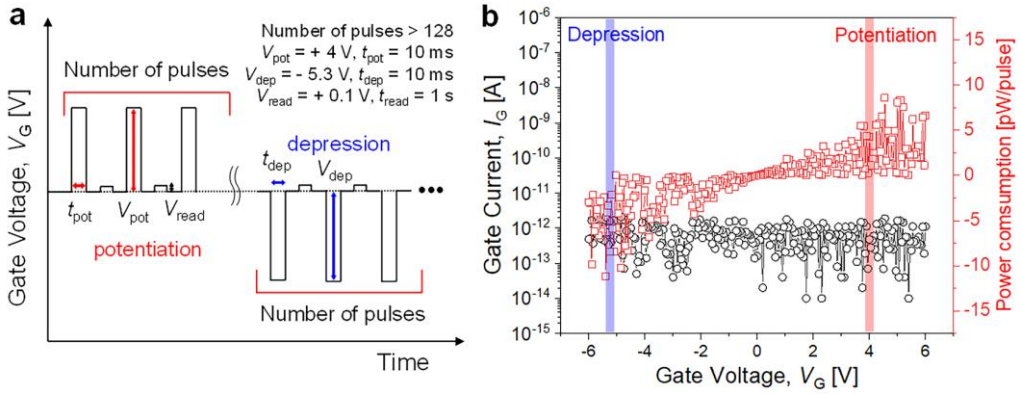

Figure S13| Gate pulse scheme, gate leakage current and power consumption. **a,** Pulse schematic for potentiation, depression and read. **b,** Gate leakage current (I_G) via the gate dielectrics and power consumption for weight update per each pulse.

In order to implement a synaptic device capable of on-chip learning, it is important to reduce energy consumption during weight update. In **Figure S13 a**, a gate voltage scheme with an identical pulse width and amplitude for potentiation, depression and read, is illustrated. An optimal gate switching pulse for the potentiation is + 4 V with 10 ms, that for the depression is – 5.3 V with 10 ms. The read pulse is V_{GS} = 0.1 V and V_D = 0.05 V with 50 ms. **Figure S13 b** shows the measured gate current (I_G) through the gate dielectrics composed of formed Al_2O_3, pEGDMA and SiO_2. At the optimized potentiation and depression, I_G is less than 1 pA, *i.e.*, I_G=0.48 [pA] for the potentiation and I_G=0.34 [pA] for the depression. Energy consumption can be calculated by $I_G \cdot V_G \cdot t$, where t is the time required for the potentiation and the depression. As a consequence, energy consumption per each pulse was 19.25 [fJ/pulse] for the potentiation and 18.02 [fJ/pulse] for the depression. This energy level in the pEGST is comparable to the approximated energy level of a 10 [fJ/spike] in a synapse of the human brain.

8. Conductance change according to the amplitude and width of the applied gate pulse

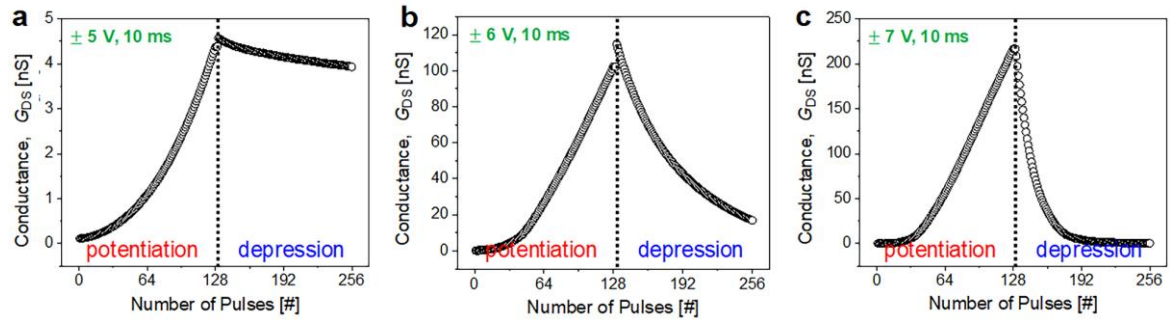

Figure S14| Conductance (G_{DS}) change for synaptic weight update according to various amplitudes at a fixed pulse width (10 ms) for potentiation and depression. a, ± 5 V, **b,** ± 6 V, **c,** ± 7 V.

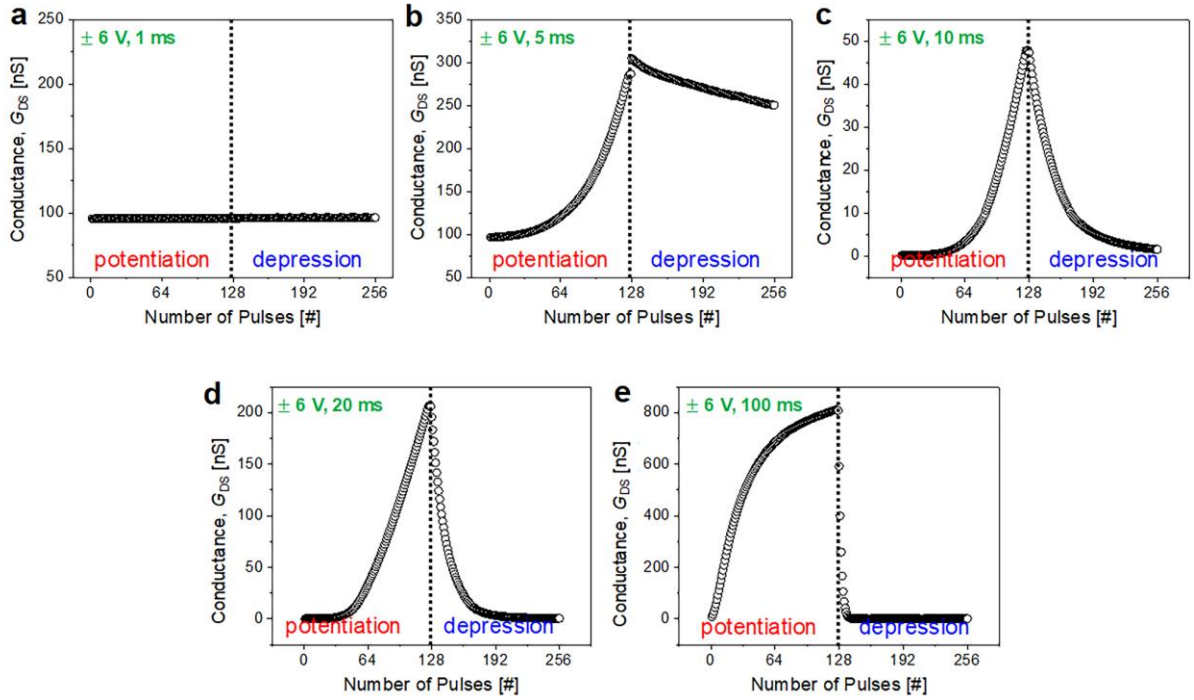

Figure S15| Conductance (G_{DS}) change for synaptic weight update according to various pulse widths at a fixed amplitude (± 6 V) for potentiation and depression. a, 1 ms, **b,** 5 ms, **c,** 10 ms, **d,** 20 ms, **e,** 100 ms.

Figure S14 shows the conductance (G_{DS}) change for synaptic weight update according to various pulses applied to the gate. For simple estimation, the number of multi-states was reduced to 256 (2^8, 8 bits) from 8192 (2^{13}, 13 bits). At the same pulse width (t_{pulse}=10 ms), the

curve shape of the potentiation and depression was altered by the pulse amplitude (V_G) only. As a consequence, linearity and symmetry were also changed. Accordingly, the V_G should be optimized. **In Figure S15**, the G_{DS} change for synaptic weight update was analyzed according to change in the t_{pulse} at a fixed V_G. When the t_{pulse} was shorter than 1 ms, there was no G_{DS} change. The curve shape of the potentiation and depression also varied with the t_{pulse}. Accordingly, linearity and symmetry also changed. Hence the t_{pulse} should be optimized as well.

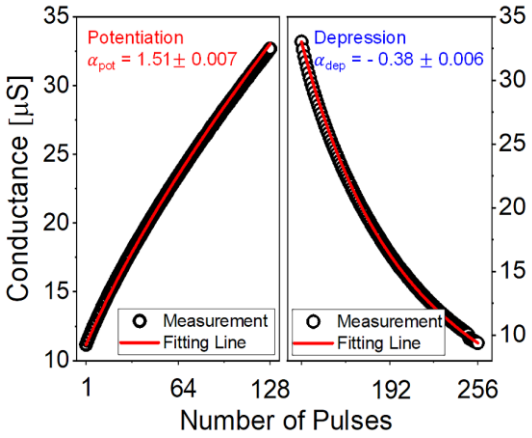

Figure S16| Optimized analog switching conductance levels (black circle) of the pEGST and its fitting curve (red line) in the simulations

Reflecting split experiments for updating synaptic weight, the pulse condition was optimized to improve linearity and symmetry, as shown in **Figure S16**. Thereafter the measured G_{DS} was fitted with the following equation:

$$G = \begin{cases} ((G_{max}^{\alpha} - G_{min}^{\alpha}) \times w + G_{min}^{\alpha})^{1/\alpha} & if\ \alpha \neq 0, \\ G_{min}^{\alpha} \times (G_{max}/G_{min})^{w} & if\ \alpha = 0. \end{cases} \quad (1)$$

The regression error between the measured G_{DS} from the fabricated pEGST and the linearly fitted G_{DS} from the above equation was 0.007 for the potentiation and 0.006 for the depression, respectively. Note that they are negligibly small. This feature is attractive not only for avoiding unstable operation induced by device variability but also for improving pattern recognition accuracy, and saving energy during the weight update.

9. Configuration of MLP for MNIST Pattern Recognition

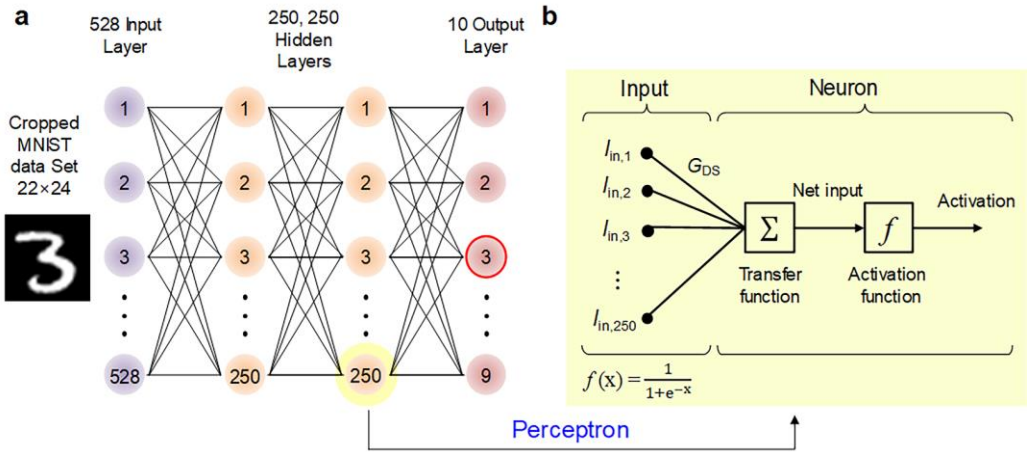

Figure S17| a, Configuration of the multi-layer perceptron (MLP) used to simulate the pattern recognition rate for the handwritten dataset of the MNIST. **b,** Signal processing and transmission via each layered neuron.

To evaluate the functionality of the fabricated pEGST for pattern recognition, supervised learning with backpropagation was carried out using a hand-written dataset provided by Modified National Institute of Standards and Technology (MNIST). The overall configuration of the multi-layer perceptron (MLP) used in the neural network simulations is shown in **Figure S17 a**. It is composed of 24×22 (=528) input neurons that are cropped from 28×28 pixels. This subtraction was performed to intentionally remove dummy pixels along with edges of a handwritten character, to improve computational efficiency. **Figure S17 b** shows the signal processing and transmission procedure in each neuron. There are two hidden layers, and each hidden layer is comprised of 250 neurons. Each neuron acts as a single perceptron. The 1st-hidden layer receives multiple inputs of 528 and the 2nd-hidden layer collects multiple inputs of 250. The collected input signals are multiplied by the synaptic weight represented by conductance change, then they are accumulated by the transfer function. The accumulated result is modified by an activation function (sigmoid function) and transferred to the input of

the next layer. To train the patterned images, 5,000 training sets were randomly selected from the total 60,000 images in the MNIST dataset at each epoch.

10. Comparison of various synaptic devices

Table S1| Comparison of interspecific synaptic devices and pEGST.

Reference number	Device	Potentiation pulse	Depression pulse	Non-linearity (α_{pot}/ α_{dep})	Asymmetry Ratio	# of Terminals	# of bits [N_{bit}] / (# of states)
[6]	PCM	0.5 ~ 0.9 V / 500 ns	2 ~ 4 V / 25 ns	-	-	2	6 / (100)
[7]	PCM	-	-	-	-	2	8 / (250)
[8]	RRAM (TiO_2)	2 V / 1 ms	- 2 V / 1 ms	2.1/ 0.45	≈ 0.55	2	6 / (64)
[9]	RRAM (PCMO)	- 3 V / 1 ms	3 V / 1 ms	3.68/ - 6.76	≈ 0.79	2	5 / (40)
[10]	RRAM (Ag:a-Si)	3.2 V / 300 µs	- 2.8 V / 300 µs	2.4/ - 4.88	≈ 0.43	2	6 / (100)
[11]	CNT FET	- 6 V / 5 ms	6 V / 5 ms	-	≈ 0.82	3	6 / (120)
[12]	FeFET	3.7 V / 75 ns	-3.2 V / 75 ns	5.54/ -8.08	≈ 0.83	3	4 / (32)
[13]	FeFET	3.7 V / 100 µs	- 3.2 V / 100 µs	1.98/ -4.73	≈ 0.45	3	5 / (50)
[14]	SONOS FET	-7 V/ 10 µs	7 V / 10 µs	-	≈ 0.51	3	5 / (31)
This work	Electrolyte-gated FET	4 V/ 10 ms	- 5.3 V / 10 ms	**1.38/ -0.51**	**0.29**	3	**13 / (8192)**

Table S1 compares various types of interspecific synaptic devices such as PCM, RRAM, and Ferroelectric FET (FeFET) with the pEGST in terms of pulse condition for weight update, linearity, symmetry, and the number of bits (N_{bit}). The pEGST showed good linearity (α_{pot} = 1.38 and α_{dep} = - 0.51) with symmetry (AR = 0.29) and much larger N_{bit}, which is an important factor to achieving high accuracy pattern recognition in an analog deep neural network (DNN). The larger N_{bit} is also advantageous to extract a specific fraction of the highest linearized zone in conductance changes from the entire P/D synaptic updates. The relatively high amplitude and wide pulse width are expected to be reduced when the thicknesses of the gate dielectrics are thinned further and the doping concentration of H^+ in the pEGDMA is increased.

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