18nm n-channel and p-channel Dopingless Asymmetrical Junctionless DG-MOSFET: Low Power CMOS Based Digital and Memory Applications

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Research Article

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18nm n-channel and p-channel Dopingless Asymmetrical Junctionless DG-MOSFET: Low Power CMOS based Digital and Memory Applications

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Abstract

In this paper, an 18nm dopingless asymmetrical junctionless (AJ) double gate (DG) MOSFET has been designed for suppressed short channel effects (SCEs) for low power applications. A desired ON and OFF state current ratio with subthreshold performance parameters under limit, is the major focus of the proposed transistor. Different sensitivity parameters of dopingless AJ DG MOSFET such as drain extension, length of gate overlapping and oxide thickness are compared with the AJ DG MOSFET with doped channel region. The ON-state current obtained is 3.80 x 10^{-6} A/μm with reduced OFF-state leakage current up to1.37 x 10^{-17} A/μm. The subthreshold slope (SS) and drain induced barrier lowering (DIBL) of the device obtained are 59.5 mV/decade and 10.5 mV/V respectively. Temperature analysis of proposed device at various temperature such as 250 K,300 K, 350 K and 400 K shows a small variation in OFF-state current (<15%). Additionally, a p-channel AJ DG MOSFET along with n-channel AJ DG MOSFET are designed and their performance is evaluated for CMOS inverter circuit and 6T SRAM cell. All the design and analysis has been done with a 2D/3D Visual TCAD device simulator.

Keywords: Asymmetrical DG MOSFET; dopingless; junctionless; subthreshold performance; low power; Inverter; SRAM.

1. Introduction

The size of the semiconductor devices is being continuously reduced and has entered into the nanoscale range[1]. Every two years the number of transistors doubles because the size of the MOSFET is reduced. oxide semiconductor field effective transistor (MOSFET) is a semiconductor device used in various applicationslike for analog and RF applications to handle the radio frequency signals that are high in power from devices like television, radio transmitter, amplifiers [2].For reduction in cost and to increase the speed of the device double gate MOSFETs are taken into consideration[3]. MOSFET's are used for biomedical applications that are used as a biosensor to detect biomolecules like enzymes, nucleotide, protein, and antibodies[4][5]. Application of MOSFET as a biosensor has benefited over other methods as it has more sensitivity, compatibility, mass production and miniaturization [5]. MOSFET is also used for memory applications to store data. 6T SRAM cell using MOSFET was designed to store data that occupies less area in the chip [6]. MOSFETs were also adopted by NASA to detect interplanetary magnetic fields and interplanetary plasma. Low power MOSFETs are desired in digital applications as a switch that prevents DC from flowing through gate thus, reducing power consumption and providing large input impedance. Reducing the size of the MOSFET reduces the size of the channel length which causes short channel effect and it increases the leakage current [7][8]. The reduction in the size of semiconductor devices has given rise to short channel effects (SCEs)[9]. The various short channel effects arise due to parasitic capacitances, drain induced barrier lowering, mobility degradation, hot carrier effects etc. To overcome these effects the devices, need to be engineered using different techniques like gate engineering and channel engineering [2] [10-14]. Gate engineering includes changing the material of the gate with different work functions, designing double gate, triple gate and multi-gate structures. Channel engineering includes changing the shape and size of the channel, drain and source regions. The cause of the SCEs is when the width of the drain barrier extends into the drain and source region barrier lowering.

Many MOSFET's structures such as double-gate MOSFET, gate all around MOSFET, triple gate MOSFET, SOI MOSFET, double step buried oxide has been designed to overcome SCEs. Sarkar et al. [14] proposed a Double gate MOSFET having three different gate metals with different work function for enhancement of RF and analog performances. Nasri et al. [15] proposed a tri- gate SOI MOSFET for analyzing the thermal performance of the device and reducing the thermal field in Tri- gate SOI MOSFET. Pakaree et al. [16] designed a class AB amplifier using Double Gate MOSFET for audio amplification and noise reduction. Abhinav et al.[17] design a junctionless Double Gate MOSFET for studying misalignment effects and thermal stability by varying the temperature from 200K to 500 K . Misalignment of the gate causes low performance of the device and reduces ON state current. Srivastava et al.[18] proposed a cylindrical surrounding Double Gate MOSFET. The MOSFET designed is used as A RF switch for the application in wireless telecommunication and is capable of storing more energy than the conventional device.Orouji et

al.[19] proposed a SOI MOSFET with double step buried oxide having the advantages of bulk structure as well as SOI structure. This device reduces the self-heating effects with degrade the device performance. Ajay etal.[20] proposed a junctionless Double gate MOSFET with an underlapped gate at the source and drain in two different structures for binding molecules.This structure is used as biosensor in biomedical applications for detecting various diseases. Ajay et al.[21] designed a device junctionless Double gate MOSFET using dielectric modulation technique for detecting biomolecules. Wang et al.[22] proposed a Double Gate MOSFET with asymmetric gates on both sides for improving the performance of the device and reducing the short channel effects(SCEs).Ramesh et.al[23] proposed a Generic Double-Gate MOSFET for better threshold voltage, subthreshold swing, DIBL etc. Andreas et al. [24] designed a threshold voltage model for an undoped symmetrical double-gate MOSFET. This model has been simulated by varying silicon thickness and gate oxide thickness.

In this paper an 18nm dopingless asymmetrical junctionless double gate (AJ DG) MOSFET has been proposed. The structure and dimensions of the device are discussed. Double-gate MOSFET has gate placed in an unsymmetrical manner with different doping in the drain, source and channel. Hf 0_2 is used as a gate oxide material. Gate contact material used is p+ polysilicon. Drain, source and channel regions are contained in thin silicon wafer. The sensitivity analysis of the proposed device is carried out by varying parameters like drain extension, length of gate overlapping and oxide thickness. The proposed device dopingless AJ DG MOSFET and different doping concentrations in the channel, drain and source region has lowered the DIBL ratio, near to ideal subthreshold slope and increased the I_{ON}/I_{OFF} ratio. The proposed transistor performance has been evaluated at different temperatures ranging from 250 K to 400 K. The paper is mainly divided into three sections. Section 1 describes the introduction of different types of MOSFETs and their applications in various field. It also describes the proposed device and its performance. Section 2 contains detail description of proposed device along with its dimensions. Section 3 contains four different parts. The first part describes the ON and OFF state current of the device. Second part contains the sensitivity analysis of the device and third part is based on the reduction in short channel effects. The section 4 includes design of an inverter circuit with proposed n-channel and p-channel AJ DG MOSFET for low power and low voltage CMOS based digital and memory applications.

2. Device Structure and Dimensions

The presented section deals with the design of asymmetric gate junctionless MOSFET for low power and steep subthreshold performance characteristics.

A. Proposed Dopingless Asymmetrical Junctionless Double Gate MOSFET of 18 nm channel length

The proposed structure has two gates asymmetrical to each other as shown in Figure 1. The proposed dopingless asymmetric junctionless double-gate MOSFET has gate placed in an unsymmetrical manner with different doping concentrations of drain, source and gate.The ON and OFF state of the MOSFET determines the length of the channel. When the MOSFET is in ON state the channel length is equal to the overlap region of the gate and when the MOSFET is in OFF state the channel length is equal to the total channel length of the gate minus the overlap region. The total channel length of MOSFET is 18 nm. During ON state the channel length becomes 4 nm (length of the overlap region) and during OFF state the channel length becomes 14 nm(total channel length of MOSFET minus overlap region). The source region is highly doped while the drain region is lightly doped and the channel is undoped. The high values of the I_{ON} (ON-state current) with supressed I_{OFF} (OFF-current) are proved to be a suitable choice for low power and high-speed applications.

This design is implemented using Visual TCAD which is based on drift diffusion model. Drift diffusion model depends on the values of electric field, lattice temperature and doping. For semiconductors the value of electric field E and doping concentation of holes and electrons are taken into consideration . The drift diffusion assumption is given by the equation 2.1

$$\vec{v} = \overrightarrow{v_d}(E) - \frac{D(E)}{n} \nabla n \quad (2.1)$$

where the drift part is $\overrightarrow{v_d}(E)$ and the diffusion part is $\frac{D(E)}{n} \nabla n$ .The above equation is most commonly used where $\overrightarrow{v_d}(E)$is linear in nature and *D(E)* is constant. However the size of the semiconductor has been reduced over the years , therefore the assumptions of equation 2.1 is insufficient.

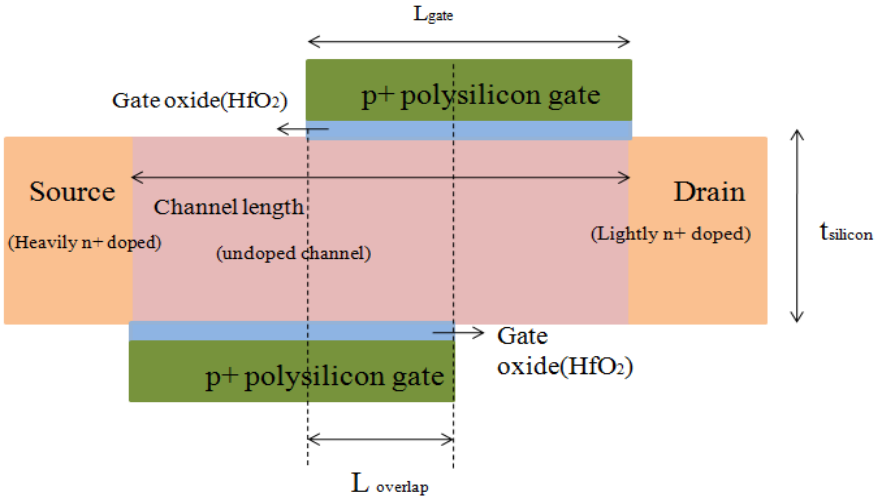

Figure 1:Dopingless Asymmetrical Junctionless DG MOSFET

Table 1: Dimensions of the proposed dopingless AJ DG MOSFET

Region	Dimension
Channel length	18 nm
Gate length	11 nm
Length of the overlap region	4 nm
Thickness of silicon	6 nm
Length of source/drain	8nm
Gate oxide thickness(Hf 0_2)	1 nm
Doping Concentration of source	$1x10^{19}\ cm^{-3}$
Doping Concentration of drain	$1x10^{15}\ cm^{-3}$

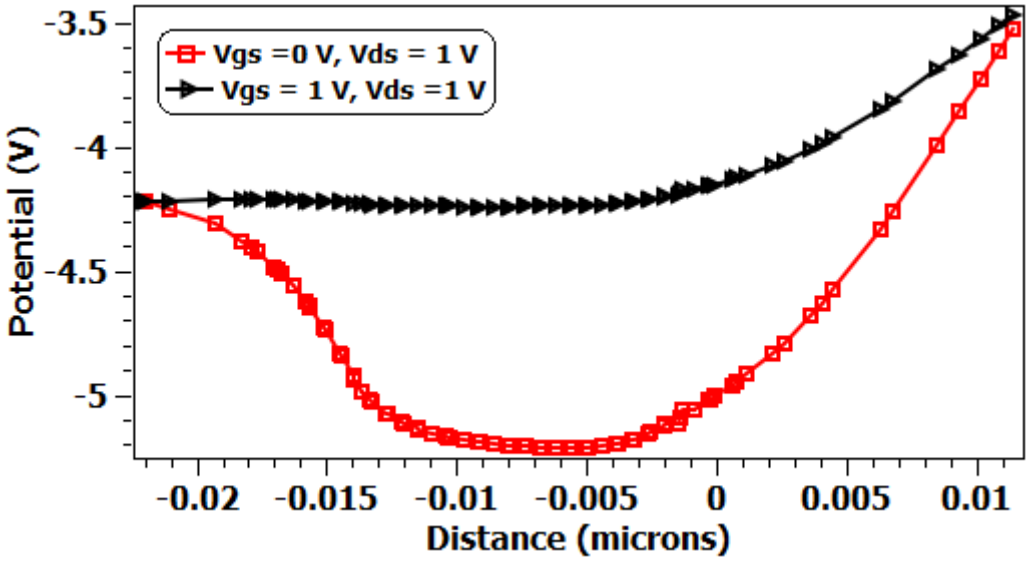

Figure 2 (a) Electric potential of dopingless AJ DG MOSFET

Figure 2 (a) shows the graph of the electric potential of dopingless AJ DG MOSFET. Electric potential is the potential difference between the surface of the polysilicon gate and the bulk of the MOSFET. When the gate voltage is low the potential of the channel region decreases, with an increase in the gate voltage the height of the barrier reduces (i.e force of electric field that forms the barrier reduces) and channel potential increases, therefore increasing the drain current. Figure 2(b) represents the electric field of dopingless AJ DG MOSFET. At low gate voltage, there is a sudden increase in the electric field in the channel region that suppresses the leakage current in the OFF-state. The spike in the electric field reduces with an increase in the voltage bias.
Figure 2 (c) represents the energy band diagram of dopingless AJ DG MOSFET. E_c and E_v are the conduction band edge and valence band edge respectively.

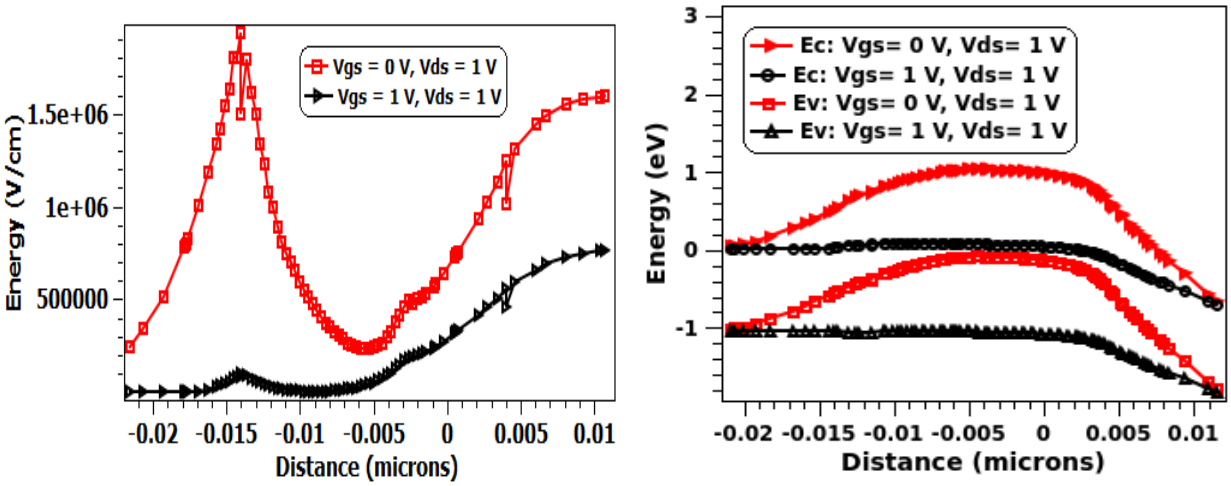

Figure 2(b) Electric field of dopingless AJ DG MOSFET (c) Energy band diagram of dopingless AJ DG MOSFET

When positive gate voltage i.e $V_{gs}>0$ is applied, electron concentration increases near the interface of oxide and semiconductor and the barrier reduce increasing the flow of electrons from source to drain region during the ON state. During OFF state the barrier increases reducing the leakage current.

3. Result and Discussion

A. ON state current and OFF state current of the proposed device.

The analysis of proposed dopingless asymmetrical junctionless double gate MOSFET with 18 nm channel length has been done by using drift diffusion model in visual TCAD device simulator. The majority charge carrier is n channel MOSFET is electrons. The doping concentration is different for drain, source and channel. Gate voltage and drain voltage increases by if the concentration of electron density is increased with the corresponding decrease in the concentration of holes. The doping concentration of source is increased to $1x10^{19}cm^{-3}$ equal to that of the channel region and the doping concentration of drain is reduced to $1x10^{15}cm^{-3}$.The channel region is undoped that is made of thin silicon wafer. The undoped channel has advantages of having a higher carrier mobility and suppresses the threshold voltage variation caused by random dopant fluctuation. Source, Drain and channel region is made of thin silicon wafer of 6 nm thickness.

The result obtained by dopingless AJ DG MOSFET is shown in Figure 4. From Figure 3, it can be seen that the ON-state current is increased and there is a reduction in OFF-state current therefore increasing the I_{ON}/I_{OFF} ratio and improving the performance of the device. It is observed that the introduction pocket region in the channel significantly suppresses the short channel effects (SCEs). Table 2 shows the comparison of ON state and OFF state current of dopingless AJ DG MOSFET and Doped AJ DG MOSFET of I_{ON} and I_{OFF} current. The Doped AJ DG MOSFET has same doping concentration of drain, source and channel. The doping concentration of source, drain and channel for doped AJ DG MOSFET is $1x10^{19}cm^{-3}$.

Table 2: Comparison of ON state and OFF state current of AJ DG MOSFET with n+ pocket region and AJ DG MOSFET without pocket region from Ref.[21].

Device structure	I_{OFF}	I_{ON}
Dopingless AJ DG MOSFET	1.37 x 10^{-17} A/μm	3.80 x 10^{-6} A/μm
Doped AJ DG MOSFET	1.15 x10^{-16} A/μm	7.49 x 10^{-5}A/μm

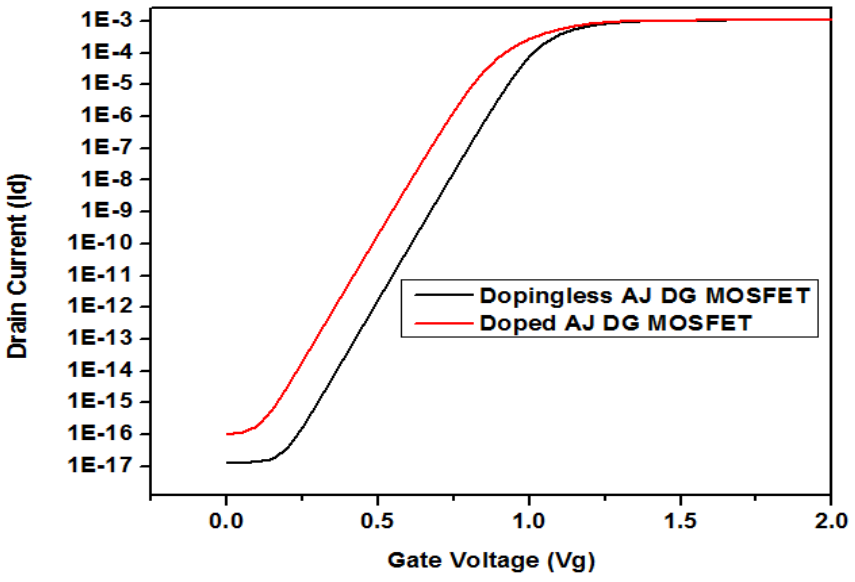

Figure 3: V_{gs} versus I_d graph for dopingless AJ DG MOSFET and Doped AJ DG MOSFET

B. Sensitivity analysis of the proposed device

Figure 4 (a) and (b) shows the sensitivity of dopingless AJ DG MOSFET with 18 nm channel length and AJ MOSFET with equal doping of 18nm channel length with a ±15% change in the oxide thickness. The oxide thickness taken is 1nm,

3nm, 5nm. When oxide thickness decreases, the gate has better control over the channel region. It can be seen from the graph that dopingless AJ DG MOSFET has uniform variation in the graph and the OFF-state current keeps on reducing with a decrease in oxide thickness. Doped AJ DG MOSFET with equal doping has a kink in the graph at a lower voltage and is not uniform as compared to dopingless AJ DGMOSFET. The kink in doped AJ DG MOSFET is formed due to surface trap at the gate. As the oxide thickness increases the surface trap density increases and gate control reduces causing the formation of the kink. Therefore, dopingless AJ DG MOSFET shows better performance and is less sensitive to change in thickness of the gate oxide.

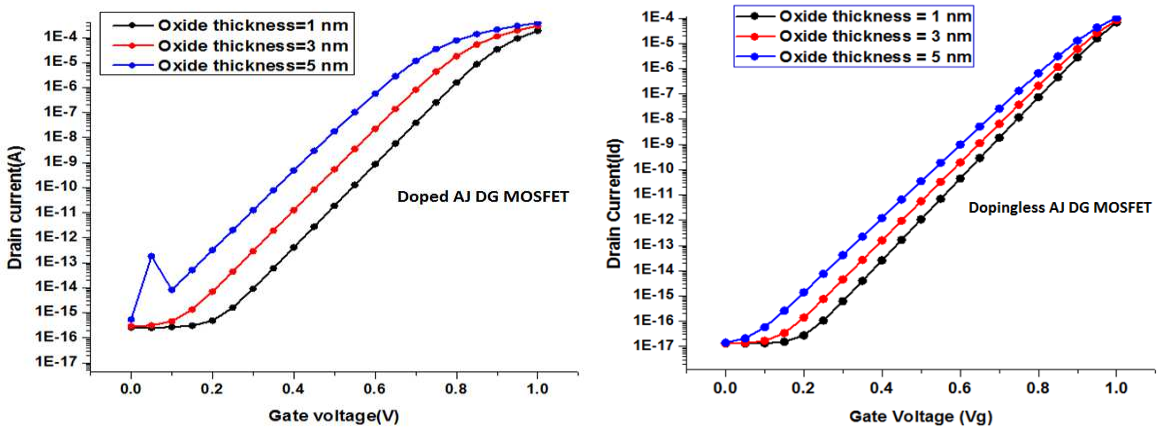

Figure 4 Gate voltage versus drain current graph of (a) Variation in oxide thickness of doped AJ DG MOSFET(b) Variation in oxide thickness of dopingless AJ DG MOSFET of 18 nm

Figure 5(a) and (b) shows the sensitivity of dopingless AJ DG MOSFET and AJ DG MOSFET with equal doping by changing the length of the drain (Lext). The length considered is 8nm, 10nm, and 15nm. It is observed that dopingless AJ DG MOSFET with 18 nm channel length shows reduced OFF state current than that of AJ DG MOSFET with equal doping. The leakage current reduces in Doped AJ DG MOSFET in the subthreshold region as there is random dopant fluctuation which causes variation in threshold voltage of the device. Therefore, dopingless AJ DG MOSFET is less sensitive as compared to the AJ DG MOSFET with equal doping [22], hence dopingless AJ DG MOSFET region is more robust and less sensitive to change in the length of extension of drain as there is no variation in OFF state current.

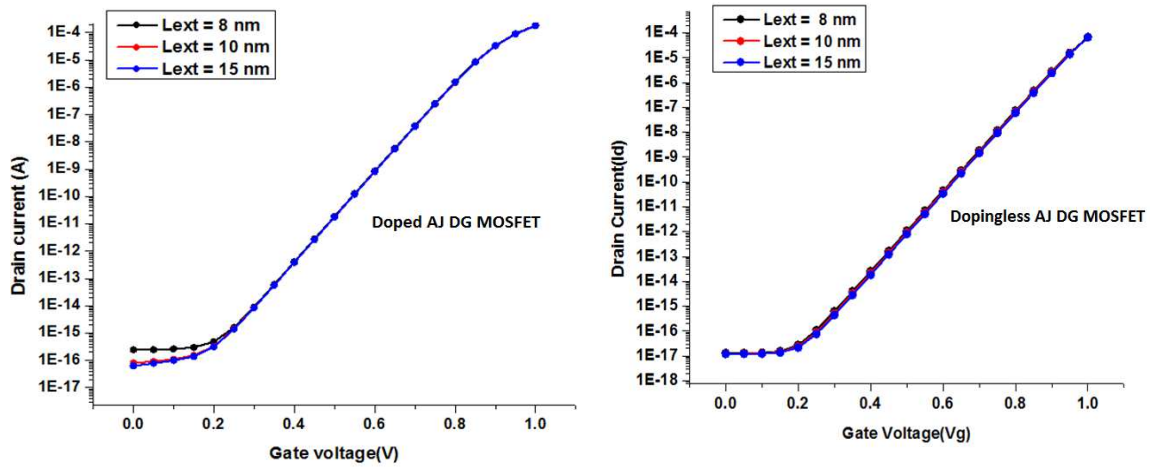

Figure 5: Gate voltage versus drain current graph of (a) Variation in length of drain extension of doped AJ DG MOSFET (b) Variation in drain extension of dopingless AJ DG MOSFET of 18 nm

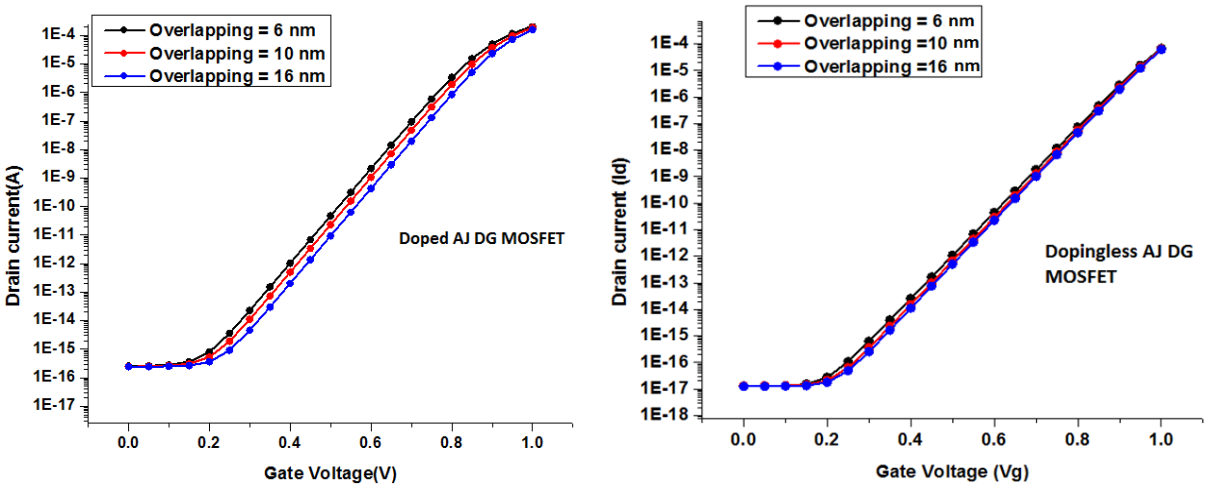

Figure 6: Gate voltage versus drain current graph (a) Variation in the overlapping region of doped AJ DG MOSFETof (b) Variation in an overlapping region of dopingless AJ DG MOSFET

Figure 6 (a) and (b) show the variation of the overlapping region in dopingless AJ DG MOSFET and AJ DG MOSFET with equal doping. The length of overlapping considered is 6nm, 10nm and 16 nm. It is observed that dopingless AJ DG MOSFET shows negligible variation in the graph compared to AJ DG MOSFET with equal doping. For fixed gate length the variation in overlap region has very less effect on subthreshold performance which is favourable in case of any misalignment.Such a dopingless AJ DG MOSFET can be compared with self-aligned FinFET in terms of lowself-alignment issues arises due to fabrication defects. Hence, dopingless AJ DG MOSFET can be a suitable choice for high performance and low power applications.

C. Reduction in Short Channel Effects (SCEs)

Drain induced barrier lowering (DIBL) is a short channel effect in which the threshold voltage reduces with increases in drain voltage. The DIBL ratio is calculated using $\delta V_{gs}/\delta V_{ds}$ mathematically. The DIBL ratio obtained is 10.5 mV/V at gate length 20nm.Subthreshold slope (SS=$\frac{dV_{gs}}{d(logI_d)}$) is a short channel effect which occurs in the subthreshold region when there is leakage in the current. The slope of the drain current and gate voltage during the subthreshold region gives SS. This parameter reduces the performance of the device. The proposed structure suppresses the SS to 59.5 mV/decade than the other structures as shown in Table 3. Figure 7 shows the comparison of the DIBL value and SS value for dopingless AJ DG MOSFET and Doped AJ DG MOSFET. The DIBL and SS value for dopingless AJ DG MOSFET are less compared to doped AJ DG MOSFET. Hence, the proposed structure gives better performance.

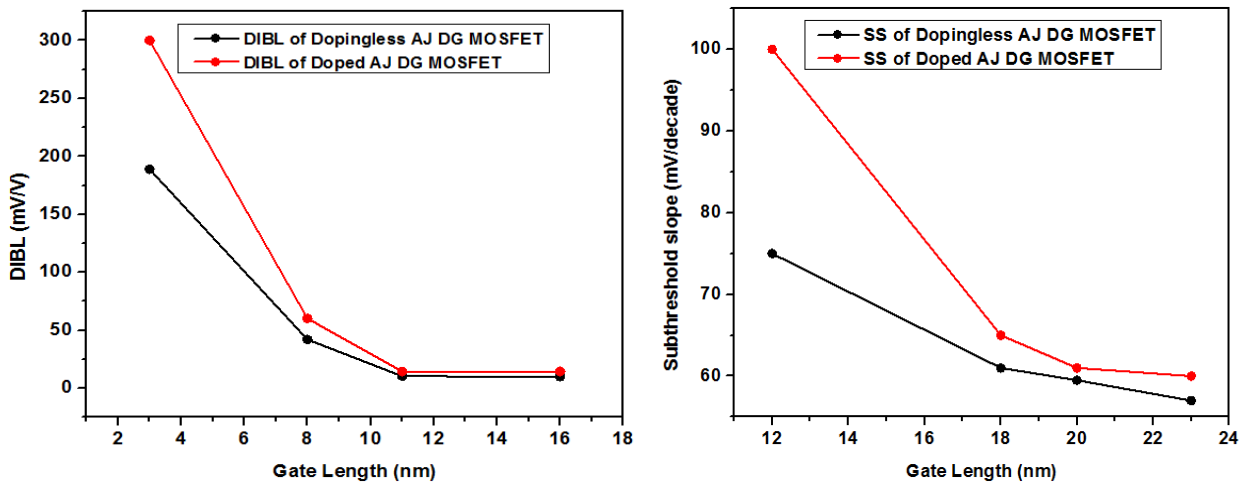

Figure 7(a) DIBL values at different gate length of dopingless AJ DG MOSFET and doped AJ DG MOSFET (b) SS values at different gate length of dopingless AJ DG MOSFET and doped AJ DG MOSFET

Table 3 : Comparison of performance parameters of different MOSFET structures ref[21].

Reference	I_{ON}	I_{OFF}	I_{ON}/I_{OFF}	SS(=$\frac{dV_{gs}}{d(logI_d)}$)	DIBL(=$\frac{\partial V_{gs}}{\partial V_{ds}}$)	Channel Length
(GC-DMGJL) MOSFET,(2018)[25]	7.695 x 10^{-4} A/μm	3.741×10^{-10} A/μm	2.057x10^{6}	73.42 mV/dec	21 mV/V	15 nm
AJ DG MOSFET,(2016)[22]	127 μA/μm	0.001 nA/μm	1.27 x10^{5}	68 mV/dec	65mV/V	20 nm
(DMSG) MOSFET,(2011) [26]		1.053x 10^{-16}A		64.7978 mV/dec		10 nm
JLDG, (2012)[27]			4.86 x10^{9}	62.32 mV/dec	75.98 mV/V	20 nm
DG MOSFET			4.03 x10^{9}	63.34 mV/dec	79.58 mV/V	20 nm
AJ DG MOSFET with n+ pocket region,(2020)[28]	1.88 x 10^{-4} A/μm	9.7 x 10^{-17} A/μm	5.15x10^{13}	59 mV/decade	13.4 mV/V	20 nm
Dopingless AJDG MOSFET(proposed)	**3.80 x 10^{-6} A/μm**	**1.37 x 10^{-17} A/μm**	**2.77x 10^{11}**	**59.5 mV/decade**	**10.5 mV/V**	**18 nm**

D. Temperature Analysis

Figure 8 shows the temperature analysis of dopingless AJ DG MOSFET. The temperature is varied from 250 K to 400 K with step size of 50 K. The increase in temperature increases the OFF state current and there is no significant change in the ON state current. OFF state current of the device at 250 K is 2.36×10^{-19}, 300 K is 3.50×10^{-17}, 350 K is 1.64×10^{-15} and 400 K is 5.56×10^{-14} .Therefore the ratio of ON state to OFF state current reduces thereby degrading the performance of the device. As the temperature increases, the OFF state current or the leakage current increases due to two reasons 1) current due to thermal generation 2) current due to impact ionization(process in which electron hole pairs are formed in huge amount that leaks through the depletion region generating current.

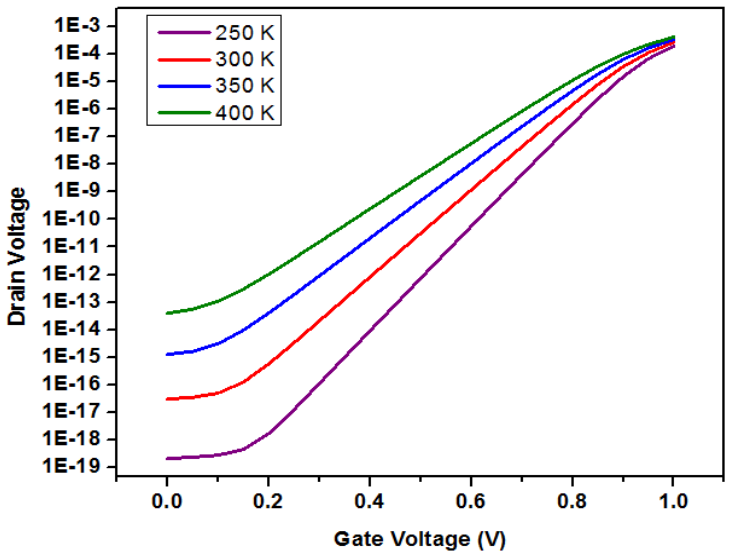

Figure 8 Temperature Analysis of dopingless AJ DG MOSFET

P - channel dopingless asymmetrical junctionless double gate MOSFET

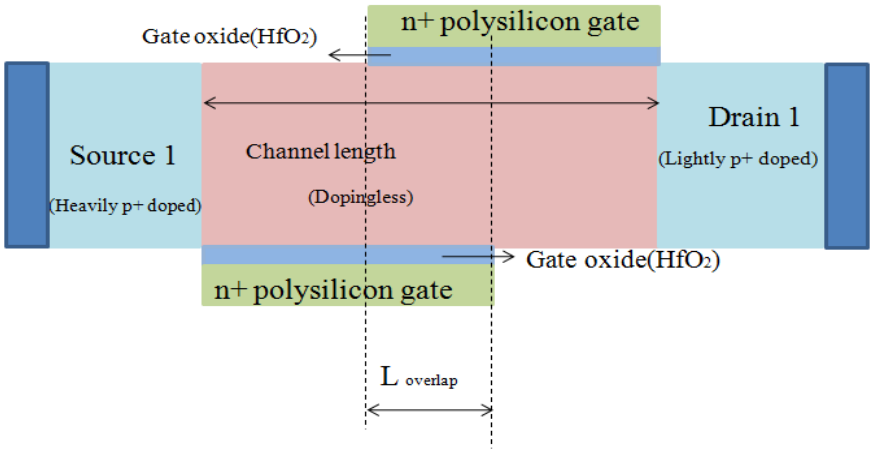

Figure 9 Design of p channel dopingless AJ DG MOSFET

Figure 9 represents the p-channel dopingless AJ DG MOSFET asymmetric has gate placed in an unsymmetrical manner with different doping concentrations of drain, source and gate which gate contact as n+ polysilicon. Gate oxide (HfO_2) has thickness 1 nm. Source and drain region has p type doping with concentration of $1x10^{19}\ cm^{-3}$ and $1x10^{15}\ cm^{-3}$ respectively. Channel region is undoped. Length of the channel region is 18 nm. Length of overlapping region $L_{overlap}$ is 4 nm. Length of the drain and source regions is 8 nm. Figure 10 shows that matching of nmos and pmos . Both pmos and nmos are compatible with each other. Both nmos and pmos have same threshold voltage magnitude and drain current through nmos is equal to drain current through pmos at all times.

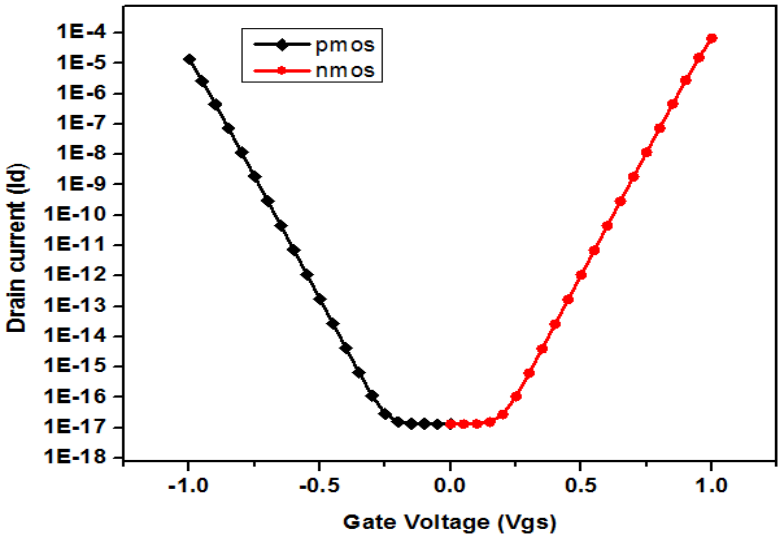

Figure 10 Matching of nmos and pmos of dopingless AJ DG MOSFET

4. Low power applications

i) Proposed Complementary CMOS Inverter design

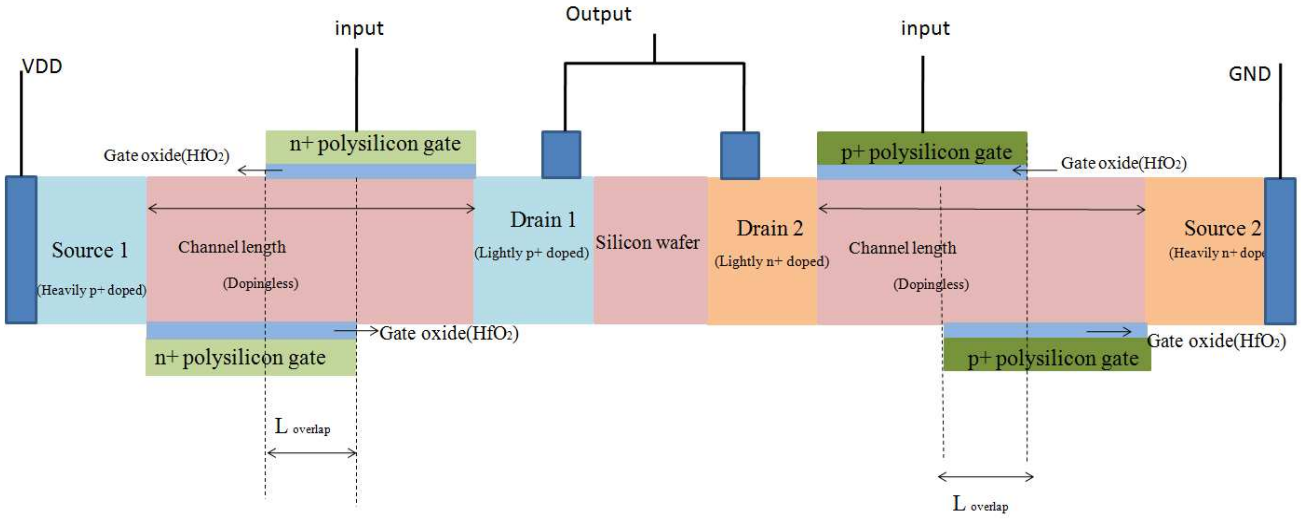

Figure 11 Design of inverter using nmos and pmos of dopingless AJ DG MOSFET

Figure 9 represents inverter design using n-channel and p-channel of dopingless AJ DG MOSFET (proposed NMOS and PMOS). The input of the device is given through the gate contact of both NMOS and PMOS. The ratio of the width of PMOS and NMOS is taken as 2:1.All the four gates are interconnected to each other. Output of the device is received through the drain 1 and drain 2 interconnected to each other. When the input given to NMOS is smaller than the threshold voltage of NMOS then NMOS of the inverter remains in cut off region. The PMOS in this case is in linear region and drain current of NMOS and PMOS is zero. Therefore, the output voltage becomes equal to the supply voltage. When input voltage is greater than threshold voltage of PMOS+ supply voltage, then PMOS works in cut off region and NMOS in linear region and the drain current is zero therefore the output obtained is zero as NMOS is connected to the ground. Both the drains are interconnected to each other. Source 1 is connected to VDD and source 2 is connected to

GND. Figure 10 shows the output obtained from the inverter. When the input is 1 the output received is 0.The inverter output shows an ideal behaviour. This shows that the proposed dopingless AJ DG MOSFET is compatible with CMOS technology and useful for low power digital circuit and memory design such as SRAM and DRAM cell.

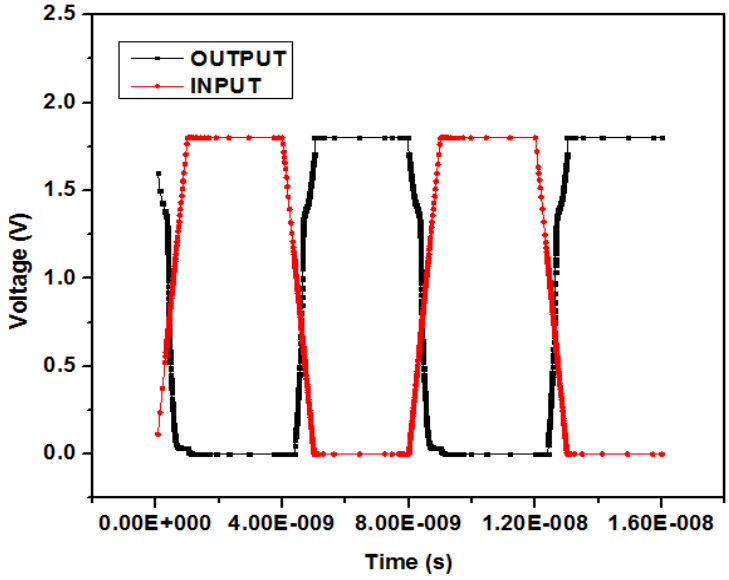

Figure 10 INPUT v/s OUTPUT graph for the inverter with respect to time.

Fabrication steps of Inverter

Fabrication of CMOS inverter is designed using NMOS and PMOS integrated over the same silicon wafer. Silicon wafer of doping concentration of $1x10^{16}cm^{-3}$ is taken as the as the substrate that is thinned down to 6 nm. Gate oxide $Hf0_2$ of 1 nm is grown on both sides of the wafer for NMOS and PMOS. Ion implantation is used to add impurities to drain and source region . This method accelerates the dopants to 20- 100 keV and the depth of penetration can be decided by increasing or decreasing the accelerating voltage of the ions. Polysilicon gate is layer is deposited over the oxide region using the chemical vapour deposition process. Polysilicon gate is deposited using silane or trichlorosilane. Pure silane or solution of silane with 70% to 80% nitrogen is used to ensure the growth of the layer with temperature range between 600 and 650^0C with pressure of 25 and 150 Pa.

ii) 6T SRAM CELL with proposed transistors

Figure 11 represents 6T SRAM cell [30] that is designed using dopingless AJ DG MOSFET. It has nodes WI, BI, Blb, these nodes are connected to the probe for studying the voltage level on the probe. The probe is based on inverters that are cross connected. The drain of the PMOS of the first inverter is connected to the drain of the NMOS of the first inverter and the drain of the PMOS of the second inverter is connected to the drain of the NMOS of the second inverter. The source of both the PMOS of the inverter is connected to Vdd, and source of both the NMOS of the inverter is connected to ground. The gate of NMOS and PMOS of first inverter is connected together and to the node connecting the drain of PMOS and NMOS of the second inverter. The gate of the NMOS and PMOS of the second inverter are connected together and to the node connecting the drain of NMOS and PMOS of first inverter. Figure 12 presents the hold state of 6-T SRAM cell using proposed complementary MOS transistors. Figure 13 describes read operation of 6-T SRAM cell with proposed NMOS and PMOS transistors.

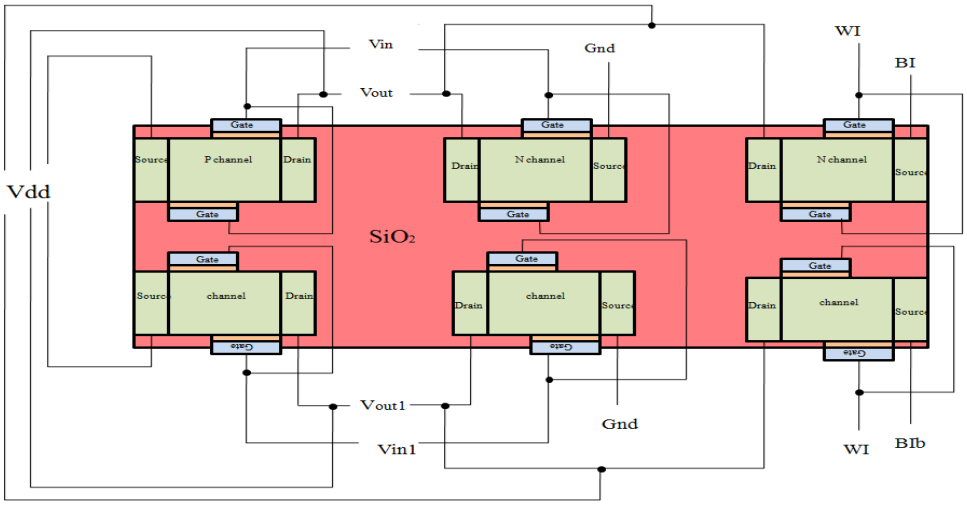

Figure 11 6T SRAM cell using dopingless AJ DG MOSFET [30]

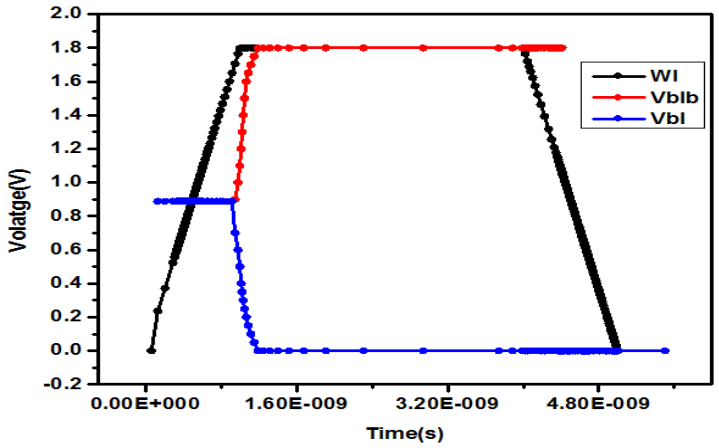

Figure 12 Hold state analysis of proposed 6T SRAM cell

Hold operation

In hold operation the SRAM cell is in static state and stores the data. When the Word line is 0V the transistor n3 and n4 are in OFF state and from the figure it can be seen that 0 and 1 value is retained in the inverter.

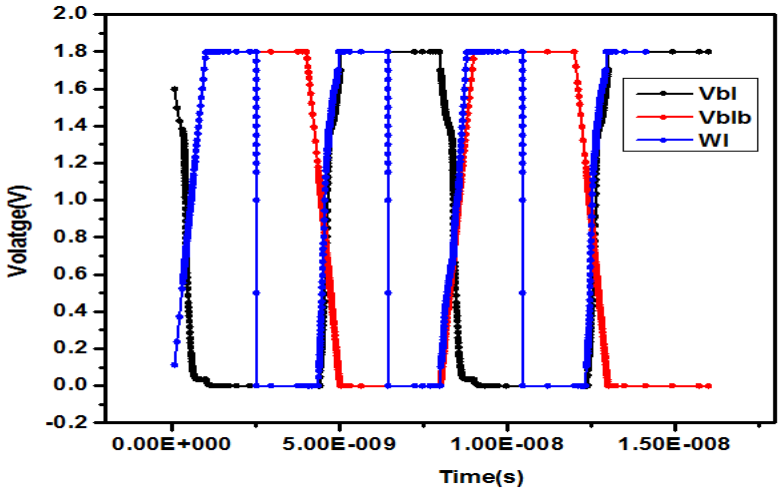

Figure 13 Read analysis of proposed 6T SRAM cell

Read Operation

During the read operation both the bit lines BL and BLB are pre-charged. When the word line is raised to 1.8 V, the node that is storing 0 pulls down one of the bit lines whereas the other bit line remains pre-charged. The data stored is read through the voltage that is present at the bit line. Therefore, from the graph it can be seen that the voltage in the bit line BL and BLB has the same data as that of V_{out} and V_{out} when the word line (WL) is V_{DD}.

Write operation

Write operation can be performed using either one of the transistors n3 or n4 which is connected to V_{DD} or GND. To write 1 to V_{out1} both the bit lines BL and BLB is charged to V_{DD}. The word line is asserted to V_{DD} to enable the transistor n3 and n4. From the figure it can be observed that when the values of BL and BLB is forced to 1 or 0 the output of inverter 1 and inverter2 is changed accordingly.

5. Conclusion

The proposed 18nm dopingless AJ DG MOSFET has gate placed in an unsymmetrical manner with different doping concentration in the drain, source and channel. The short channel effects (SCEs) which arise due to scaling of MOSFET is suppressed more in Dopingless AJ DG MOSFET, therefore improving the performance of the device. The I_{ON}/I_{OFF} ratio increases (~$2.77x10^{11}$), the ideal value of subthreshold slope (59.5 mV/V) and DIBL (10.5 mV/V) value is lowered. Analysis of Sensitivity between dopingless AJ DG MOSFET and AJ DG MOSFET with equal doping has been compared and observations are made. Different sensitivity parameters of dopingless AJ DG MOSFET such as drain extension, length of gate overlapping and oxide thickness are varied for both the device structures. It is observed that Dopingless AJ DG MOSFET is less sensitive to change in the parameters and the device is more robust thandoped AJ DG MOSFET. The proposed structure dopingless AJ DG MOSFET is less sensitive and provides better subthreshold performance. Different temperatures such as 250 K, 300 K, 350 K and 400 K were considered for temperature analysis of the device. With increasing temperature, the leakage current increases due to increase in thermal current and impact ionization current which increases the OFF state current and reduces I_{ON}/I_{OFF} current ratio. This shows the device suitability for low power digital and CMOS based large capacity memory applications. P-channel dopingless AJ DG MOSFET is designed. Matching of nmos and pmos of AJ DG MOSFET is shown in the paper. A complimentary dopingless AJ DG MOSFET (n-channel and p-channel) is used to design a lower power inverter circuit and 6T SRAM cell with ideal voltage characteristics.

Declarations

Funding

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Conflicts of interest/Competing interests

There is no conflict of interest at any stage.

Availability of data and material

The associated data will be made available on request.

Code availability

The simulation work has been carried out Cadence virtuso.

Authors' contributions (optional): NA

Additional declarations

Ethics approval: NA

It is a simulation-based design and analysis. So, it does not produce any environmental hazards.

Consent to participate

Yes, we are ready to participate.

Consent for publication

We are ready for publication with your journal.

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