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Short Report

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Enhancement of Breakdown Voltage in SOI MOSFET using buried p-type Silicon

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Abstract

Semiconductor industry is still looking for the enhancement of breakdown voltage in Silicon on Insulator (SOI) Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Thus, in this paper, heavy n-type doping below the channel is proposed for SOI MOSFET. Simulation of SOI MOSFET is carried out using 2D TCAD physical simulator. In the conventional device, with no p-type doping is used at the bottom silicon layer. While, in proposed device, p-type doping of 1×10^{18} cm^{-3} is used. Physical models are used in the simulation to achieve realistic performance. The models are mobility model, impact ionization model and ohmic contact model. Using TCAD simulation, electron/hole current density, impact generation, recombination and breakdown phenomena are analyzed. It is found that the proposed with p-type doping of 1×10^{18} cm^{-3} for SOI MOSFET yields high breakdown voltage. In contrast to conventional device, 20% improvement in breakdown voltage is achieved for proposed device.

Keywords: *SOI MOSFET; p-type Doping and Breakdown Voltage; simulator; breakdown*

1. Introduction

SOI MOSFET is fabricated on insulator that separate from bulk substrate. Therefore, compared to

conventional MOSFET, SOI MOSFET offers several benefits. The benefits are: (i) vertical and horizontal isolation, (ii) diminished leakage conduction, (iii) enhanced latch up free operation and (iv) reduced drain induced barrier lowering. Further, the body capacitance is lower in SOI MOSFET, which leads to enhanced switching speed [1]. The other technological advancement in SOI devices are optimization of Si film thickness [2], suppressing floating body effects [3-4], buried insulator [5-6], SC1 standard cleaning [7], control of bipolar effects, modeling of self-heating [8], charge based modeling [9], modeling of chart channel effect [10]. This device could be classified as fully and partially depleted devices. In partially depleted MOSFET, the depletion region does not extend to the entire silicon body. The nominal thickness of silicon in partially depleted SOI device is greater than 0.15μm. The depletion area does not deplete all the carriers in the body, thereby, it is referred to as partially depleted SOI MOSFET. Thick film devices are also often considered as partially depleted SOI devices. On the other hand, the silicon in fully depleted devices is thinner than that in partially depleted device. Further, one of the advantages is that electrostatic charge in the thin channel of SOI MOSFET is controlled by gate voltage. The doping in the silicon is also lower for fully depleted devices [11]. Overall, the charge depletion is an important phenomenon that determines the breakdown voltage and leakage conduction. Apart from charge depletion, the defect induced trap can participate in leakage conduction. In addition, interface traps at Silicon channel/oxide interface limits the gate control over the channel. This trap also acts as the source of the noise. Quantification of trap concentration is required for technology development and to develop accurate model. With aforementioned issues, the SOI device also suffers from body contact. As the device body is floating, the body contact lacks. Without body contact, capacitance voltage (C-V) measurement and charge pumping technique cannot be applied to extract the energy landscape and density of the traps. The trap density can also be determined using subthreshold voltage. The difficult, yet, is that the subthreshold slop method is effective for double gate device rather than SOI MOSFET. Therefore, SOI device has issues to be addressed and performance has to be improved to meet the application demands. The industry or application demands are lower subthreshold swing, enhanced breakdown voltage,

reduced carrier leakage, better switching speed and improved device linearity. In this paper, enhancement of breakdown voltage is focused. To attain higher breakdown voltage, p-doping in the bottom of the silicon region is proposed and investigated.

2. Device Schematic

The device schematic considered for the investigation is shown in Fig. 1. The device consists of two silicon region, buried oxide, gate oxide. In a conventional device a single silicon body will be there. In this work, the silicon region is divided into two regions. A heavy p-type doping with the value of 1×10^{18} cm^{-3} is proposed for bottom silicon region. In the conventional device, the nominal p-type doping in the entire silicon region is 1×10^{17} cm^{-3}. Further, p-type doping of 5×10^{17} cm^{-3} in the bottom silicon region is also benchmarked with conventional device and proposed device to provide more details. Thickness of the top and bottom silicon region are 30 nm and 20 nm, respectively. Thickness of gate oxide and buried oxide are 12 nm and 500 nm, respectively. The gate length is 2 µm.

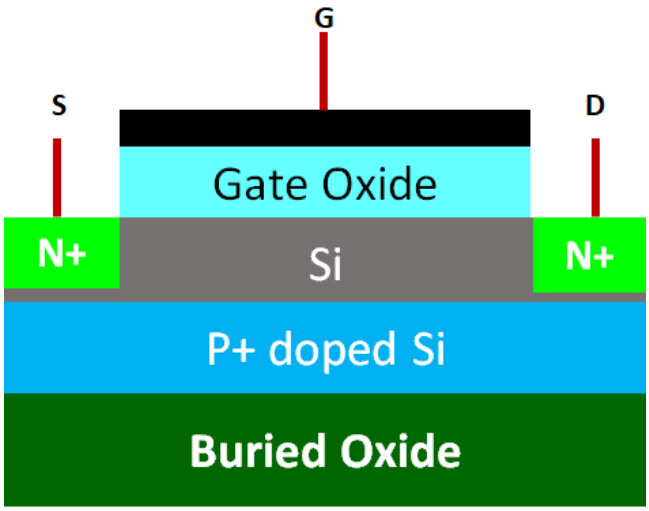

Fig. 1. SOI MOSFET schematic with gate length of 2 µm

The device in Fig. 1 is implemented in TCAD physical simulator to investigate the device. Physics based models have to be used for realistic simulation. The source and drain are doped heavily with n-type doping to make them ohmic contact. Field dependent and concentration dependent mobility are used to

incorporate the effect of carrier concentration and electric field in the mobility. The field dependent mobility model is an important model as the hole and electron accelerates with electric field. Therefore, the carrier scatter and thereby reduces the conduction current significantly. The field dependent mobility is expressed as

$$\mu = \frac{\mu_l + v(E^{m-1}/E_c^m)}{1 + k\left(\frac{E}{E_T}\right)^n + \left(\frac{E}{E_T}\right)^m} \quad \text{---------- (1)}$$

where, E and v electric field and velocity, respectively. The k, m and n are user defined parameters in the simulation. The E_T and μ_l are critical electric field and low field mobility. The low field mobility model governs the operation of the device in linear region of drain current. Further, band gap narrowing model is also used to account the concentration dependent band profile. The breakdown mechanism is facilitated in the simulation using the selb model. Newton method is used to solve the Poisson and transport equation.

3. Results and Discussion

In order to validate the simulation, the potential distribution along the channel is analysed. Fig. 2 shows the potential distribution for conventional and proposed device. For both device, the potential shows a sharp increase at gate edge. It is due to the potential difference between gate and drain terminal. In the source side potential is low as the potential difference between gate and source is lower. Compared to proposed device with doping 1×10^{18} cm^{-3}, the potential gradient is higher in conventional device with no doping. The lower potential gradient is a welcome feature in the proposed device. Further, the potential distribution is divided as the low and high field region. It is well known phenomena is that electric field (E) is the gradient of potential over space, which is expressed as

$$E = \frac{\nabla V}{\nabla x} \quad \text{---------- (2)}$$

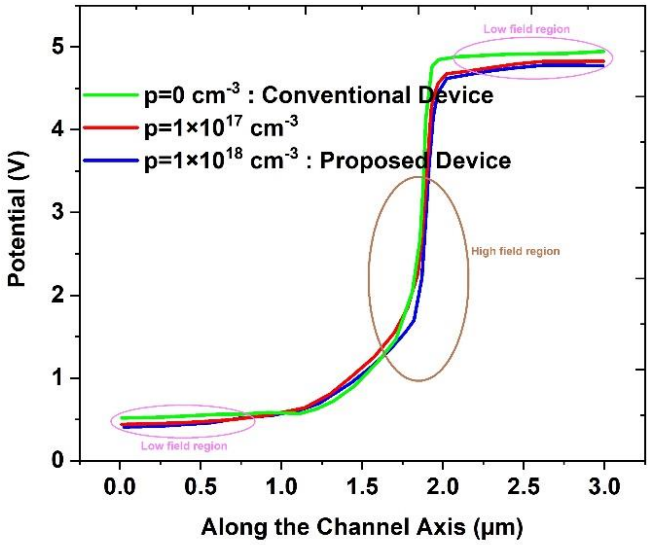

Fig. 2. Potential distribution along the channel axis (source-to-drain axis)

Where, ∇V is the small change in potential and ∇x is a small change in space. According to Eq. 1, if there is no change in potential (V) over space(x), the E approaches zero and is considered as low field region over space. If there is a great change in potential over space, the value of field approach high. Therefore, the region of constant potential is circled as a low field region and the region of potential gradient is circled as a high field region in Fig. 2. The observation shows that the electric field is high at gate edge of drain side.

Table 1
Impact generation rate for various p-doping doping in the device.

p-doping (cm^{-3})	**Impact generation rate ($cm^{-3}\ s^{-1}$)**
0	9×10^{28}
1×10^{17}	7.5×10^{28}
1×10^{18}	2×10^{28}

Impact generation is the root cause for device breakdown. Thus impact generation is extracted and given in table I. For doping concentration of 0, 1×10^{17} and 1×10^{18} cm^{-3}, the impact generation rate is 9×10^{28}, 7.5×10^{28} and 2×10^{28} $cm^{-3}\ s^{-1}$, respectively. The device with doping of 0 cm^{-3} is considered as conventional

device. The device with doping of 0 cm^{-3} is considered as conventional device. The device with doping of 1×10^{18} cm^{-3} is considered as proposed device. Among various doping concentrations, the device with doping of 1×10^{18} cm^{-3} shows a least generation rate, which leads to provide a higher breakdown voltage.

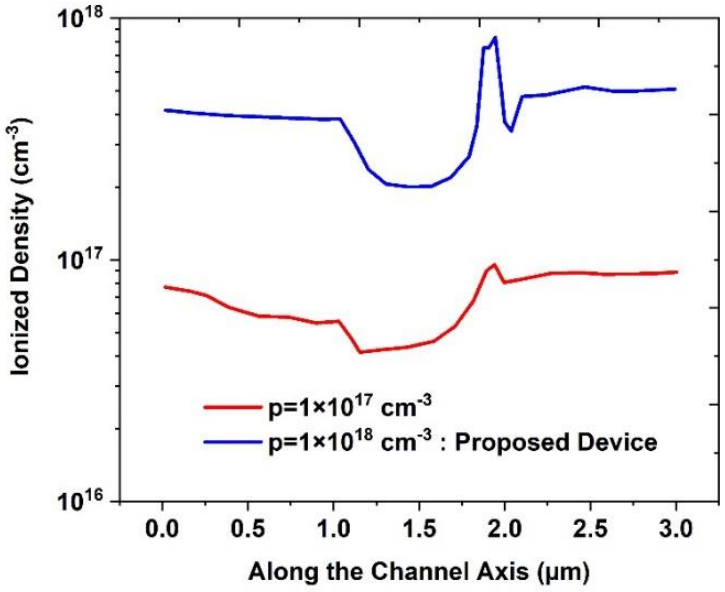

Fig. 3. Ionized concentration along the channel axis for 1×10^{17} and 1×10^{18} cm^{-3} in bottom silicon layer

Carrier ionization is shown in Fig. 3 for doping concentration of 1×10^{17} and 1×10^{18} cm^{-3}. The ionization is extracted along the channel axis. The ionized carrier is more pronounced for the doping of 1×10^{18} cm^{-3}. Higher ionization indicates that more carriers are captured. Therefore, the captured carriers could not be involved in the avalanche process in the proposed device. Further, it is interesting to note that the ionization is more pronounced near gate edge of drain side. It is attributed to high electric field near gate edge as shown in Fig. 2. As electric field is low under source and drain region, the ionization is almost constant on these regions. It indicates that ionization has strong dependency on electric field distribution. Further, the ionization density spikes at gate edge of drain side. It is because of higher electric field at gate edge as discussed in the potential distribution in Fig. 2. The ionization density is almost constant under drain and source region since the electric field is low on these regions. A similar kind of electric

field phenomena is detailed elsewhere [12].

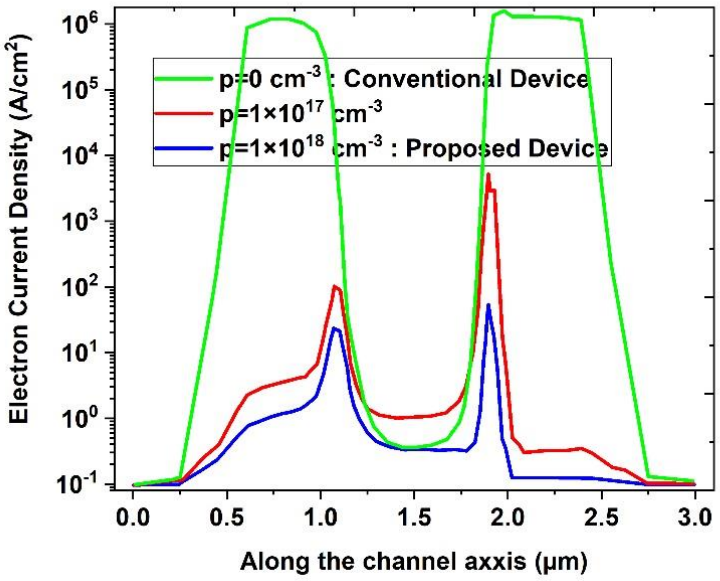

Fig. 4. Electron current density various doping at the bottom silicon layer.

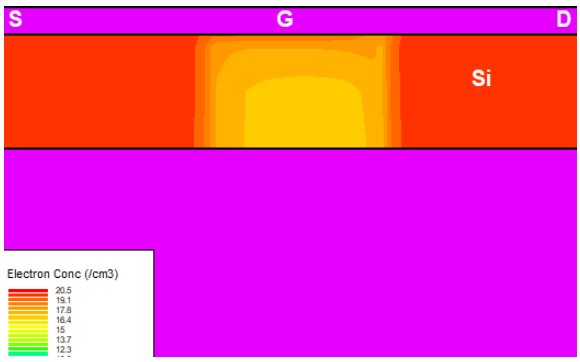

Fig. 5. Electron concentration. G, S, D are gate, source and drain, respectively. Si is silicon body.

Electron current density is shown in Fig. 4. The current density is extracted using x-plane cut (or cut along the channel). The current density is consistent with reported data in [13-14]. As it can be seen, the variation in electron current density is attributed to the potential spread [14]. Compared to high doping concentration, device with no doping demonstrate higher electron current density. It is due to participation of more number of carriers in transport. It is also observed that current density is lower under gate terminal. This indicates that the channel region under gate is more resistive. The lower current

density for highly doped device is attributed to inadequate electron concentration below channel.

Contour of electron concentration is depicted in Fig. 5. As it can be seen, the electron concentration is lower under gate since the conduction band is higher on this region. Contrarily, electron concentration is higher under source and drain region since lower conduction band energy. Under the drain and source side, the concentration is around 1×10^{20} cm^{-3}. Under gate terminal the, the electron concentration is around 1×10^{17} cm^{-3}. The above observed electron concentration in this work is consistent with the data reported in [15]. The trend of electron distribution in Fig. 5 is reflected on electron current density as in Fig. 4. This phenomenon could be well corroborated using electron current transport as

$$J_n = nq\mu\nabla V \quad ----------(3)$$

where, J_n is the electron current density. The $n, q, \mu,$ and ∇V are electron concentration, electronic charge, mobility and gradient of potential, respectively.

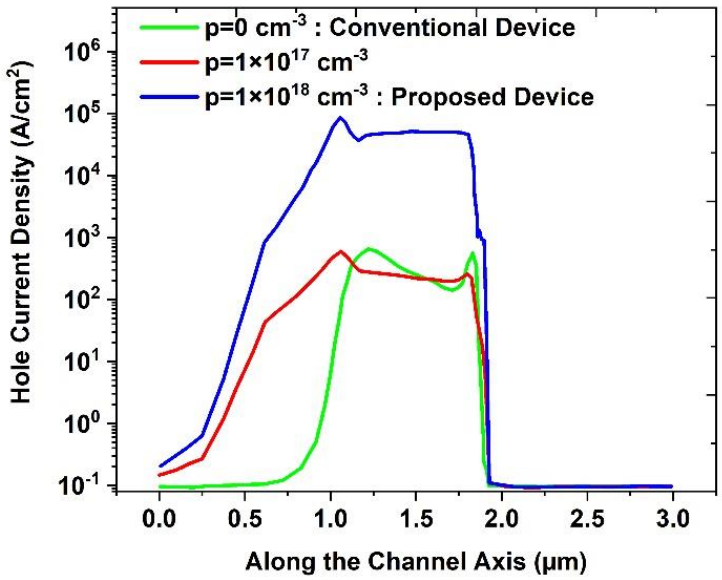

Fig. 6. Hole current density for various doping at the bottom silicon layer.

In contrast to electron current density in Fig. 4, hole current density demonstrates different behaviour, which is shown in Fig. 6. Hole current density is more pronounced in source side rather than drain side. It is due the hole collection or accumulation in source side [16]. These holes are injected from drain electrode.

Hole current density for device with doping of 1×10^{18} cm^{-3} is higher, while rest of the device is lower. The peak value of hole current density is almost the same for both conventional device and device with doping of 1×10^{17} cm^{-3}. Overall, it is observed that both electron and hole current density are non-uniformly distributed.

Table 2
Magnitude of current component in SOI MOSFET for various doping concentration (Dop. Con.)

Dop. Con. (cm^{-3})	Lateral electron current density (A/cm^2)	Vertical electron current density (A/cm^2)	Lateral hole current density (A/cm^2)	Vertical hole current density (A/cm^2)
0	1.2×10^{6}	1.8×10^{5}	1.1×10^{5}	1.2×10^{4}
1×10^{17}	8×10^{5}	1.6×10^{5}	7.4×10^{4}	3.9×10^{4}
1×10^{18}	4×10^{5}	1.2×10^{5}	7.3×10^{4}	7.4×10^{4}

Lateral and vertical current components of SOI MOSFET are given in table II. Both electron and hole current component is higher in lateral direction than that of vertical direction. Further, electron current density is higher compared to electron current density. It is due to higher electron mobility than that of hole mobility. Therefore, electron current density is a significant factor in the avalanche process.

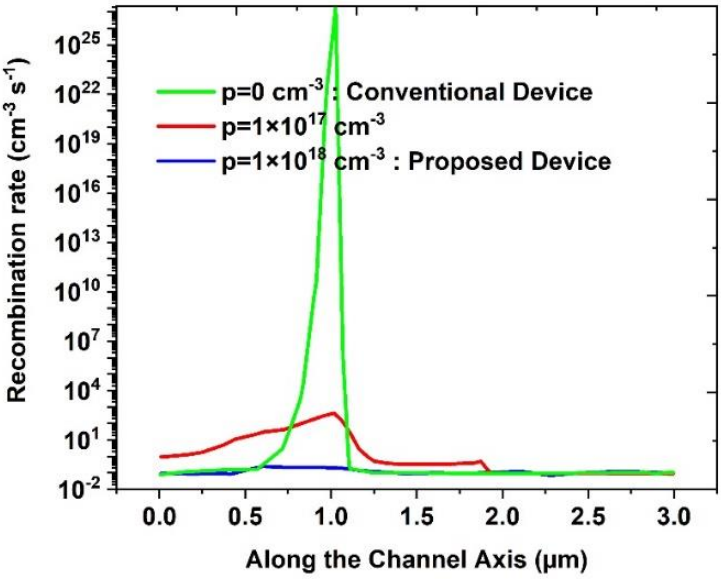

Fig. 7. Recombination in the device for various doping at the bottom silicon layer.

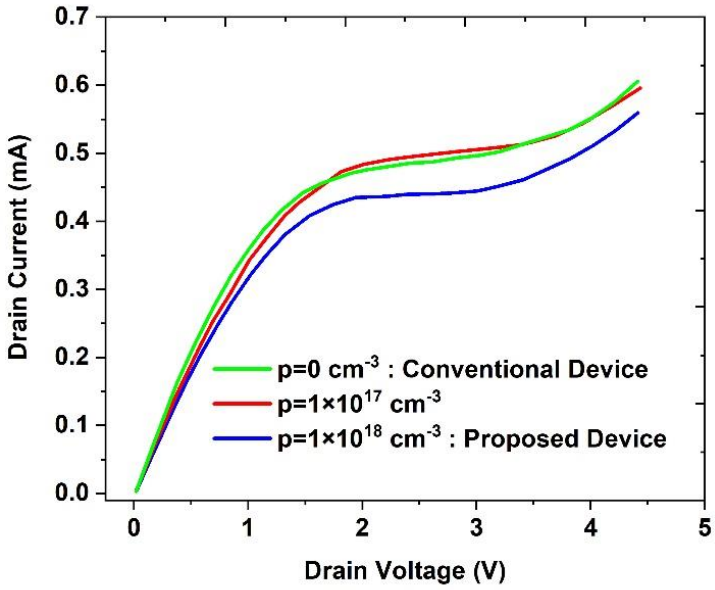

Fig. 8. Output drain current versus drain voltage.

Generation and recombination are the mechanism that leads to the breakdown phenomena in SOI MOSFET. Thus, recombination along the channel axis extracted and demonstrated in Fig. 7. For all device, the recombination spikes at gate edge of drain side. It is due to enhanced electric field at gate edge of drain side. Proposed device with p-doping of 1×10^{18} cm^{-3} shows lower recombination rate. This feature is desirable since it reduce the heat in the device. Therefore, the device reliability could be improved. Fig. 8 shows the comparable drain current of conventional and proposed device. In this analysis, the drain voltage is swept from 0 V to 4V and drain current is observed. The drain current linearly increases with drain voltage till 1.5 V. Beyond 1.5 V, the drain current saturates due to high field induced carrier scattering. As drain voltage increases further, the drain current again increase rapidly. It is due to avalanche breakdown. The breakdown voltage of device with no p-doping, with p-doping of 1×10^{17} cm^{-3} and with p-doping of 1×10^{18} cm^{-3} are 3.25 V, 2.9 V, and 3.9 V, respectively. The breakdown voltage is measured at the compliance current of 0.5 mA. SOI MOSFET with p-doping of 1×10^{18} cm^{-3} demonstrates the higher breakdown voltage. In contrast to SOI MOSFET with no p-doping, the improvement in the device with p-doping of 1×10^{18} cm^{-3} is 20 %.

5. Conclusion

A heavy p-type doping (1×10^{18} cm^{-3}) is introduced at the bottom of the silicon body in SOI-MOSFET. The distinction of p-type doping is benchmarked with conventional SOI MOSFET using TCAD simulation. In this paper, it is found that electron current is a dominant current component in the avalanche breakdown process rather than hole current. Further, it is found that proposed SOI MOSFET with heavy p-type doping yield higher breakdown voltage than that of conventional device by 20%. It is attributed to p-type dopant induced carrier ionization. The proposed SOI MOSFET is a promising candidate for analog and switching application.

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Competing Interests

The authors declare that there is no competing interest.

Availability of data and materials

All the data's and material are embedded within the article.

Authors Contributions

Conceptualization, Methodology, Resources, Formal analysis, Writing - original draft preparation, review and editing, Supervision and investigation were carried out by Deivakani M, Sumithra M.G, Chandran Venkatesan, Korhan Cengiz.

Writing - original draft preparation, review and editing were carried out by Deivakani M, ,Anitha P, Jenopaul P, Priyesh P. Gandhi.

Ethical Approval

Not Applicable

Consent to Participate

Not Applicable

Consent to Publish

Not Applicable

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