

New Electronically/Resistively Tunable Floating Emulators to Realize Memristor and Inverse Memristor

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New Electronically/Resistively Tunable floating emulators to realize Memristor and Inverse Memristor

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Abstract: This article presents the architectures of two emulator circuits, which realize the behaviour of a floating memristor and inverse memristor respectively. Both the presented emulator circuits are based on modified Voltage Differencing Current Conveyor (MVDCC) and grounded passive elements only. The feature of Electronic/Resistance tunability is found in both the emulator circuits. Furthermore, no employment of any external multiplier circuitry can be viewed as an important advantage of the proposed emulators. Also, the utility of the inverse memristor has also been discussed in theoretical discussions. The simulations have been performed to verify the working of all the presented emulator circuits, under PSPICE environment. Moreover, these MVDCC based emulators are also designed using commercially available ICs, LM13700 and AD844.

Keywords: Memristor, Inverse Memristor, MVDCC, Tunable Emulator

1. Introduction

L. Chua was the first, who laid the theoretical framework of the memristor in his article published in 1971 [1]. After which, various memristor emulators based on different active building blocks (ABBs) have been developed, given in the literature [2-30]. The detailed comparison of these emulators circuit is presented in Table. 1.

Table. 1. Detailed summary of previously reported memristor emulators given in [2-30]

| Ref. no. | Type and number of employed active element(s) | Number of used external voltage multiplier circuits / IC (AD-633) | Number and state of employed capacitor (s) (F (Floating) /G(Grounded)) | Number and state of employed resistor (s) (F/G*) | Availability of electronic control (Yes/No) | Availability of Resistance tunability (Yes/No) | Need for component matching/parameter matching | Range of Operating frequencies | Power Supply used | Number of employed BJT/MOS Transistors |
|----------|---|---|--|--|---|--|--|--------------------------------|-------------------|--|
| [2] | 4 MO-OTAs | Nil | 1G | 1F/2G | Yes | Not Shown | Yes | 150 KHz | ±2.5V | 84 MOS |
| [3] | 4 CCIIIs | 1 | 1G | 2F/1G | Not shown | Not Shown | No | 40 KHz | ±10V | 88 BJTs |
| [4] | 5 OPAMPs | 1 | 1G | 5F/3G | Not shown | Not Shown | Yes | 800 Hz | ±5V | 125 BJTs + 10 MOS |
| [5] | 4 CCIIIs, 1 | 1 | 1G | 6F/2G | Not | Not | Yes | 120 Hz | ±15V | 110 |

| | | | | | | | | | | |
|------------------------------------|--|------------|-----------|-----------|------------|------------|-----------|---------------|-------------|----------------------|
| | OPAMP | | | | shown | Shown | | | | BJTs |
| [6] | 4 CCII _s | 1 | 1F | 2F/3G | Not shown | Not Shown | No | 100 Hz | ±10V | 88 BJT _s |
| [7] | 4 CCII _s , 3 OTA _s | Nil | 1G | 3F/3G | Yes | Not Shown | No | 10 KHz | ±15V | 112 BJT _s |
| [8] | 2CCII | 1 | 3G | 3F/1G | Not shown | Not Shown | Yes | 270 KHz | ±0.7V | BJT _s |
| [9] | 1CCII+ | 1 | 2G | 4F/2G | Not shown | Not Shown | Yes | 860 KHz | ±10V | 22 BJT _s |
| [10] | 6 DDCC _s , 10 Transistor _s | Nil | 1G | 5G | Not shown | Not Shown | No | Not mentioned | ±1.25 V | 114 BJT _s |
| [11] | 1 CCTA, 1 CCII | Nil | 1G | 1F/1G | Not shown | Not Shown | No | 5 MHz | ±10V | 39 MOS |
| [12] | 3 CFOA | Nil | 2G | 2F/2G | Not shown | Not Shown | Yes | 700 Hz | ±5V | 66 BJT _s |
| [13] | 1 OTA, , 2 Transistor _s | 1 | 2G | 0 | Not shown | Not Shown | No | 12KHz | ±1V | 26 MOS |
| [14] | 1CBTA | Nil | 2G | 0 | Not shown | Not Shown | No | 1MHz | ±1.25 V | 32MOS |
| [15] | 2 VDTA | 1 | 1G | 2G | Yes | Not Shown | No | 55 KHz | ±0.9V | 20 MOS |
| [16] | 3 CCII | 1 | 1G | 4G | Not shown | Not Shown | No | 5 KHz | ±5V | 66 BJT _s |
| [17] | 2AD844 | 2 | 4G | 5F/2G | Not shown | Not Shown | No | 10 Hz | ±5V | 44 BJT _s |
| [18] | 2CFOA, 1OTA | | 2G | 3G | Not shown | Not Shown | No | 600 Hz | ±12V | 52 BJT _s |
| [19] | 4 OPAMPS | 1 | 1G | 7F/2G | Not shown | Not Shown | Yes | 1 KHz | ±12V | 90 BJT _s |
| [20] | 1 CCTA | Nil | 1G | 2F/1G | Not shown | Not Shown | No | 500KHz | ±1.5V | 29 MOS |
| [21] | 1 VDTA | 1 | 1G | 2G | Yes | Not Shown | No | 100KHz | ±5V | 22 MOS |
| [22] | 12 OTA _s | 1 | 1G | 2F/2G | Not shown | Not Shown | No | 1 KHz | ±10V | 95 MOS |
| [23] | 4 CCII, 3 OTA | Nil | 1G | 3F/3G | Yes | Not Shown | No | 5 KHz | ±15V | 110 BJT _s |
| [24] | 5 CFOA | 2 | 1G | 8F/1G | Not shown | Shown | Yes | 100 Hz | ±2V | 100 BJT _s |
| [25] | 1 CCII, 2 Op Amps, 2 BJT | Nil | 1G | 3F | Not shown | Not Shown | Yes | 20 KHz | ±12V | 100 BJT _s |
| [26] | 1 FB-VDBA | NIL | 1G | NIL | Not shown | Not shown | No | 1 MHz | ±0.9V | 19 CMOS |
| [27] | 1 OTA, 1 CDTA | NIL | 1G | NIL | Not shown | Not shown | No | 2 MHz | ±0.9V | 36 CMOS |
| [28] | 1 OTA, 1 CDBA | NIL | 1G | NIL | Not shown | Not shown | No | 1 MHz | ±0.9V | 28 CMOS |
| [29] | 4 AD844, 1 OP-Amp and 1 Diode | NIL | 1F | 4F/1G | Not shown | Not shown | No | 8KHz | 3V | BJT |
| [30] | 1 DO-OTA, 1 DVCC | NIL | 1G | NIL | Not shown | Not shown | No | 1.5 MHz | ±0.9V | 25 CMOS |
| Proposed Memristor Emulator | 2 MVDDCs | Nil | 1G | 2G | Yes | Yes | No | 500KHz | 0.9V | 52 MOS |

| | | | | | | | | | | |
|--|--------------------|------------|-----------|-----------|------------|------------|-----------|--------------|-------------|------------------|
| Proposed Inverse – Memristor Emulator | 1 MVDCCs | Nil | 1G | 1G | Yes | Yes | No | 15KHz | 0.9V | 26 MOS |
|--|--------------------|------------|-----------|-----------|------------|------------|-----------|--------------|-------------|------------------|

*F=Floating/G=Grounded

From the thorough literature, it has been concluded, that the reported memristor emulator circuits [2-30] exhibit one or more of the following design related disadvantages;

- (1) Three or more ABBs are employed [2-7, 10, 12, 18, 19, 22-23, 25]
- (2) More than two resistances are used in circuit [2-12, 15-20, 22-25]
- (3) Employment of more than one capacitance [8-9, 12-14, 17-18]
- (4) Floating passive element(s) are used [2-9, 11, 12, 17, 19-20, 22-25]
- (5) Use of external voltage multiplier IC/circuit [3-5, 8-9, 13, 15- 17, 19, 21-22, 24]
- (6) Non-availability of electronic tuning i.e. memristive behaviour cannot be controlled through biasing voltage and/or current [3-6, 8-22, 24-30]
- (7) Non-availability of resistance tuning [2-22, 24-30]
- (8) Need of matched value of passive elements [2-5, 8, 9, 12, 19, 24-25]
- (9) Partial utilization of employed ABB(s) (one or more ports are unoccupied) [2-29].
- (10) Excessive number of MOS transistors employed in the CMOS implementation [2-7, 10, 12, 16, 19, 22-25]

Also, from the performance point of view, these previously reported emulator circuits exhibit one of more of the following shortcomings:

- (1) Low operating bandwidth [2-9, 12-13, 15-25]
- (2) Poor frequency Dependency i.e. lobe area does not vary significantly for frequency variation [6-12, 18-28]
- (3) Non-symmetry in v-i lobes [6, 10, 13, 17, 19, 27, 30]
- (4) Absence of non-volatility (pulse excited response is not shown) [2, 5-8, 10, 13, 15-18, 20-22, 24-25, 29-30]
- (5) Demonstrated small lobe area at lower operating frequencies for chosen parameters [2, 3, 8, 10-13, 20, 25-26, 28-29]

While, as compared to the emulators reported in [2-30], the proposed floating memristor emulation configuration has the following advantageous features:

- (1) Use of only two ABBs namely MVDCC
- (2) Use of only three passive elements (two resistances and single capacitance)
- (3) All the employed passive elements are grounded
- (4) No use of external voltage multiplier circuit/IC
- (5) Facility of Electronic/Resistance tuning through bias voltages of MVDCCs
- (6) No requirements for matched valued passive elements.
- (7) Only fifty-two MOS transistors will be required in the CMOS implementation
- (8) Satisfactory range of operating frequencies
- (9) Excellent frequency dependency of lobes' area
- (10) Perfectly symmetrical lobes in two opposite quadrants
- (11) Presence of non-volatile nature
- (12) Demonstrated larger lobe area

Similarly, the proposed inverse memristor is also an optimized configuration consisting only single MVDCC and two grounded passive elements. It has no need to satisfy any component/parameter matching condition and it also offers Electronic/Resistance tunability.

Concept of Memristor and Inverse Memristor

The memductance of an ideal memristor depending upon the flux “ ϕ ”, can be given by Eq. (1) as follows;

$$G_M = a_0 + a_1\phi \quad (1)$$

Where,

$$\phi = \int_0^t v(\tau)d\tau \quad (2)$$

And $v(t)$ is applied input voltage.

For a sinusoidal input, $v(\tau)=v_m\sin\omega\tau$, the current-voltage relationship for memductance G_M given in Eq. (1) can be given as;

$$i = a_0v_m \sin \omega t + \frac{v_m^2 a_1}{\omega} (1 - \cos \omega t) \sin \omega t \quad (3)$$

Now, for an ideal memristor, the well-known signature property is the availability of pinched hysteresis loop with cross-over at the origin in transient $v-i$ plot (Plotted in Fig. 1 by using Eq. 3). But, several researchers have also observed and tried to demonstrate a similar type of characteristics in several electrical circuits and components. Due to the absence of other defining properties of ideal memristor, these circuits cannot be considered as ideal memristor and may be termed as non-ideal memristors. The inverse memristor is also a type of non-ideal memristor.

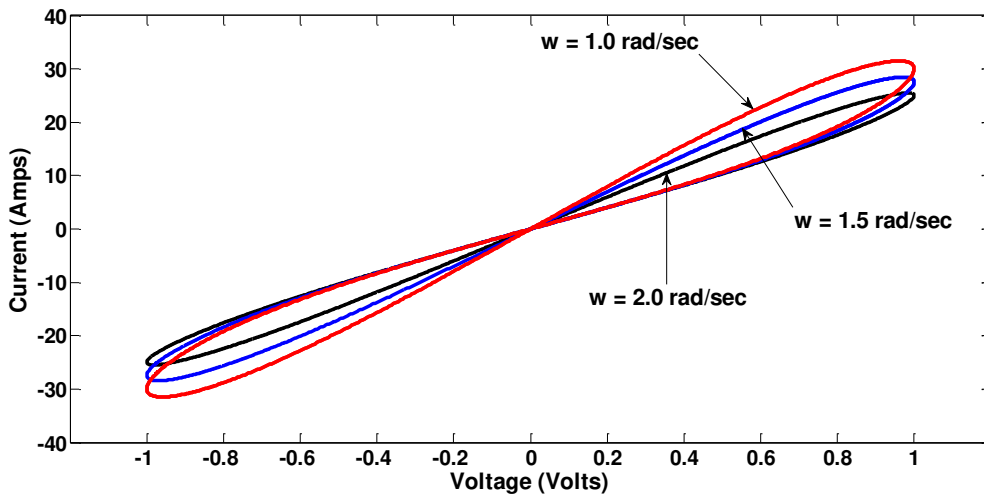


Figure. 1. $v-i$ curves of an ideal memristor plotted at different operating frequencies by using Eq. 3

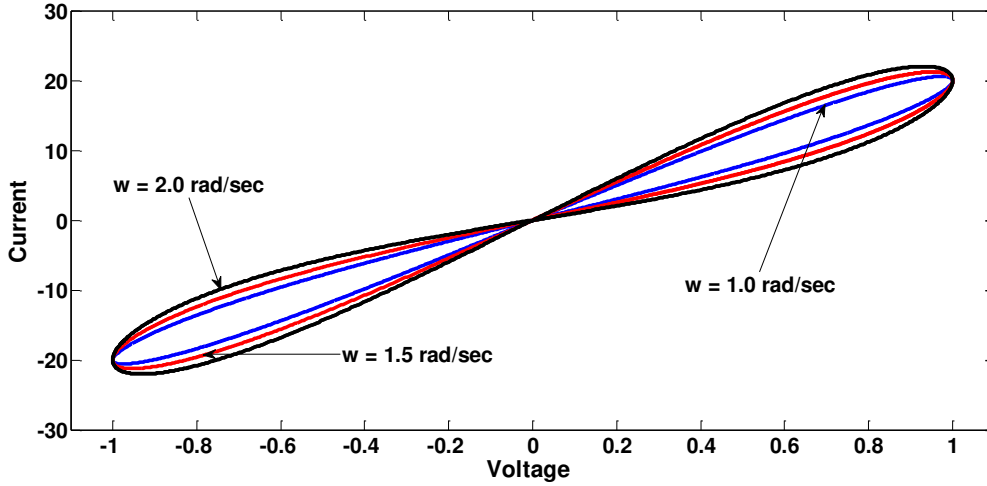


Figure. 2. PHLs of an inverse memristor at different operating signal frequencies

The current-voltage relation for an inverse memristor can be defined as,

$$i = b_0 v + b_1 \left(\frac{dv}{dt} \right) v \quad (4)$$

On putting $v = v_m \sin \omega t$, Eq. (4) becomes,

$$i = b_0 v_m \sin \omega t + \omega b_1 v_m^2 \cos \omega t \sin \omega t \quad (5)$$

The transient current-voltage characteristics for (Eq. 5), is presented in Fig. 2. It can be observed that the characteristics are found to be exhibiting two lobes in the v - i plane originating from the origin. It can be seen that on raising the value of frequency “ ω ” gives rise to increase in the area enclosed under the v - i lobes, which is an inverse (contrary) characteristic with respect to an ideal memristor (whose area expands for rising frequencies).

Therefore, due to the fact, inverse memristor does not follow all the signature properties of an ideal memristor, it cannot be used as a worthy element in various memristor related applications. But due to its unique frequency dependence characteristics, it can be used to control and enhance the performance of an ideal memristor as described below.

Now, we investigate the effect of connecting inverse memristor in parallel to an ideal memristor (as shown in Fig. 3), considering the case of flux dependent memductance. From Eq. 3 and 5, for the shunt connection of an ideal memristor (M) and inverse memristor (M’), the overall current I_{Parallel} flowing through the connection will be the sum of memristive and inverse memristive current as below;

$$I_{\text{Parallel}} = a_0 v_m \sin \omega t + \frac{v_m^2 a_1}{\omega} (1 - \cos \omega t) \sin \omega t + b_0 v_m \sin \omega t + v_m^2 \omega b_1 \cos \omega t \sin \omega t \quad (6)$$

Now, to demonstrate to the effect of connecting M’ with ideal memristor M, the area enclosed under lobes of the composite structure plays an important role. The expression given in Eq. 7 can be useful to find the area enclosed under any v - i curve;

$$A = \int_0^{T/2} i \frac{dv}{dt} dt \quad (7)$$

From Eq. 3 and 7, the area for ideal memristive case can be given as,

$$A_{mem} = -\frac{2a_1 v_m^2}{3\omega} \quad (8)$$

And similarly for the shunt connection shown in Fig. 3, it can be found by using Eq. 6 and 7 as;

$$A_{mem-inv} = \frac{2}{3} \left(-\frac{a_1 v_m^2}{\omega} + \omega b_1 v_m^2 \right) \quad (9)$$

By using Eq. 9, we can plot the area ($A_{mem-inv}$) versus frequency (ω) response for circuit given in Fig. 3, which is shown in Fig. 4. From this response, it can be observed that controlling the coefficient of inverse memristor, we can alter the frequency dependency of the lobe area. Therefore, we can conclude, connecting inverse memristor in shunt with memristor, we can achieve better controllability over memristor performance in $v-i$ plane.

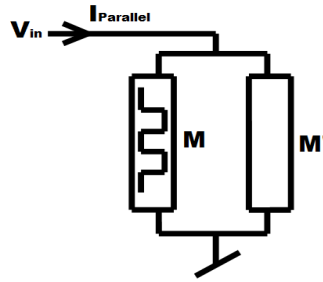


Figure. 3. Parallel connection of Memristor (M) and inverse memristor(M')

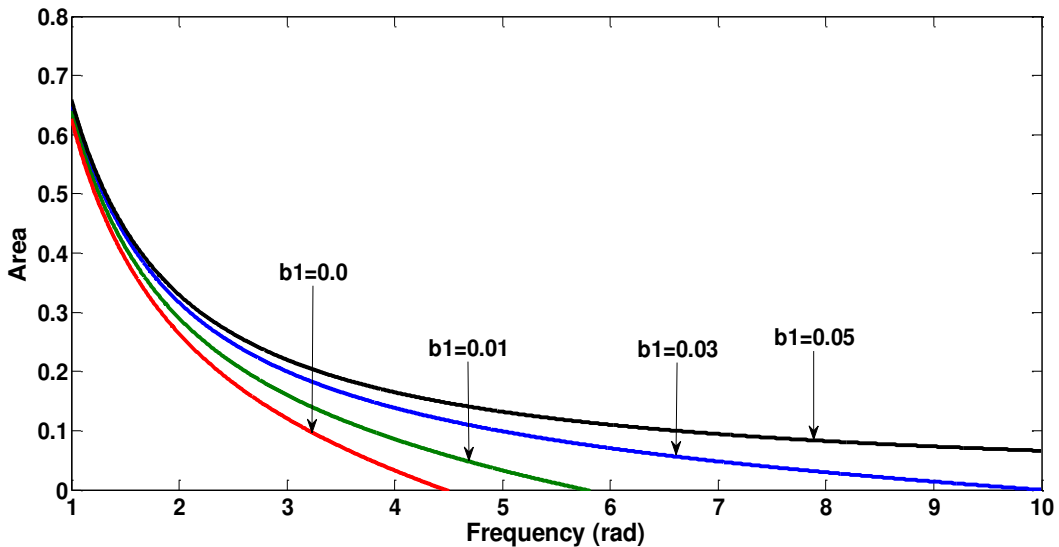


Figure. 4. Response of area with respect to frequency for different values of coefficient b_1

2. The idea of MVDCC

The MVDCC (modified VDCC), whose symbol and CMOS implementation have been shown in Fig. 5 and 6 respectively, is a modified version of VDCC. The VDCC, which is an acronym for Voltage Differencing Current Conveyour was first proposed in [35]. It is a popular

element and finds its applications in higher order filters, modern oscillators [36-37] and also passive element simulators. It can be found in the articles like [31-34] that previously some researchers have employed the modified form of VDCC to obtain the Z+ and/or Z- copy current to utilize in their circuit. But it was done without affecting the other port functions of VDCC. On the other hand, we have taken a Z-copy terminal and equalize the different voltage of Z- and Z+ terminal to the voltage of X port. The resultant modified function can also be understood from the current-voltage relationship of MVDCC shown in Eq. 10.

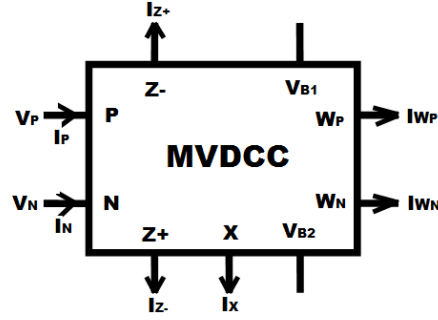


Figure. 5. Block depiction of modified VDCC (MVDCC)

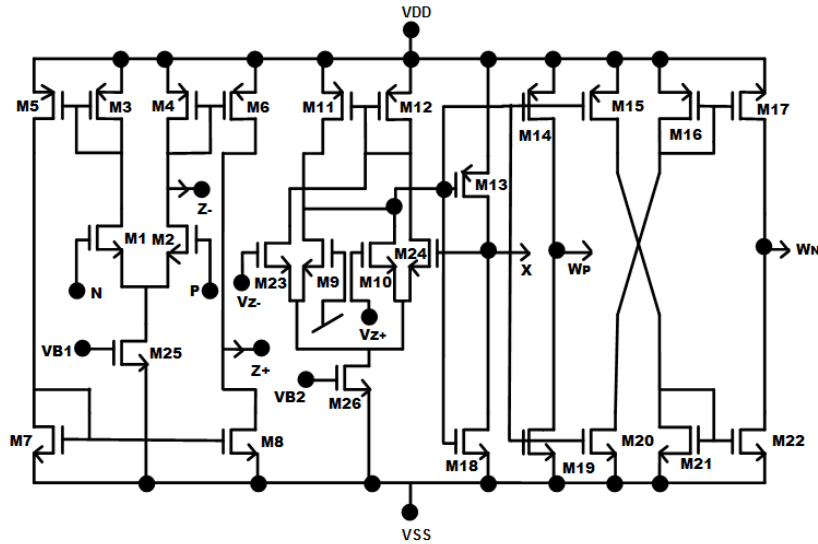


Figure. 6. CMOS implementation of realizing modified VDCC (MVDCC) concept

$$\begin{bmatrix} I_P \\ I_N \\ I_{Z+} \\ I_{Z-} \\ V_X \\ I_{Wp} \\ I_{Wn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \\ g_m & -g_m & 0 & 0 & 0 \\ -g_m & g_m & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & -1 \end{bmatrix} \begin{bmatrix} V_P \\ V_N \\ V_{Z+} \\ V_{Z-} \\ I_X \end{bmatrix} \quad (10),$$

Where, g_m is input stage transconductance. The transconductance of the input stage can be controlled by the biasing voltages V_{B1} according to the relation given in Eq. 11.

$$g_m = k(V_{B1} - V_{th} - V_{SS}) \quad (11)$$

3. Proposed MVDCC based floating memristor emulator

The Fig. 7 presents the proposed configuration of the Floating memristor based on MVDCC. It consists of two MVDCCs and three grounded passive elements. The presented circuit does not employ any voltage multiplier circuit/IC, which can be considered as the most attractive feature of this emulator.

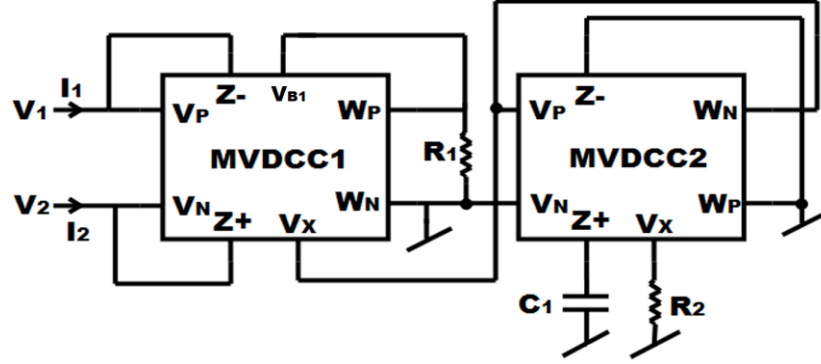


Figure. 7. Proposed configuration of Floating memristor emulator realized using MVDCCs (the other biasing voltages (other than V_{B1}) are applied through external voltages)

On applying Eq. 10 and 11, and using circuit analysis for above emulator, the admittance matrix for the given floating circuit architecture is found as;

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = k_1 \left(g_{m2} R_1 \frac{1}{R_2 C_1} \int_0^t (V_2 - V_1) dt - V_{SS} - V_{th} \right) \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (12)$$

From Eq. 12, it can be easily concluded that this equation is representing an ideal memristor whose memductance G_M can be given as,

$$G_M = k_1 (-V_{SS} - V_{th}) + k_1 g_{m2} R_1 \frac{1}{R_2 C_1} \int_0^t (V_2 - V_1) dt \quad (13)$$

The memductance G_M given in Eq. 13 consists of two parts; the first part is representing the time-independent linear part whereas, the second part is non-linear and depends upon the time-varying input voltage.

From the designed emulator it can be observed that in MVDCC2 block, the terminals Z-, W_P are connected to the ground, which may be considered as a minor wastage of circuit resources. This drawback can be easily overruled by using conventional VDCC in place of MVDCC2.

4. Frequency-dependent behaviour of proposed memristor

After careful observation, it can be concluded from the memductance of proposed memristor emulator found in Eq. 13, that memductance G_M can be viewed as representing a lossy non-linear inductor which is a parallel combination of time-dependent inductor $L_{time-dependent}$ and an equivalent resistance R_{Eq} . In the G_M expression given in Eq. (13), the time-varying part is corresponding to $L_{time-dependent}$ whose value depends upon the input voltage having a unit of Henry-Volt and R_{Eq} is represented by the fixed part.

For a sinusoidal input, $V_m \sin \omega t$, the minimum value (at peak input voltage) of the inductance $L_{time-dependent}$ (Henry-Volts) can be calculated as,

$$L_{time-dependent} = \left(\frac{R_2 C_1}{k_1 g_{m2} R_1 V_m} \right) \quad (14)$$

Similarly, the R_{eq} can be evaluated as,

$$R_{eq} = 1/k_1(-V_{SS} - V_{th}) \quad (15)$$

Now, from Eq. (14) and (15), the time constant of parallel $L_{time-dependent}-R_{eq}$ of the circuit can be obtained as,

$$\tau = \frac{L_{Time-dependent}}{R_{eq}} \quad (16)$$

From Eq. 14, 15 and 16, τ is obtained as,

$$\tau = \frac{R_2 C_1 (-V_{SS} - V_{th})}{g_{m2} R_1 V_m} \quad (17)$$

Time constant “ τ ” in Eq. 17 can relate to cut-off frequency as follows,

$$f_c = \frac{1}{2\pi\tau} \quad (18)$$

Now, “ f_c ” given in Eq. (18) can be used to define the range operating frequency (f) for proposed floating memristor emulator circuit as follows:

1. When $f < f_c$, the hysteresis loop will not be present, due to a large value of time-dependent part with respect to the time-independent part.
2. When $f = f_c$, hysteresis loop will be maximum due to equal dominance of both time-varying and constant part.
3. When $f > f_c$, hysteresis will be present in the $v-i$ plane of a memristor

5. Proposed MVDCC based Floating Inverse Memristor Emulator

The proposed MVDCC based floating emulator structure for an inverse memristor (defined in Eq. (4)), has been shown in Fig. 8.

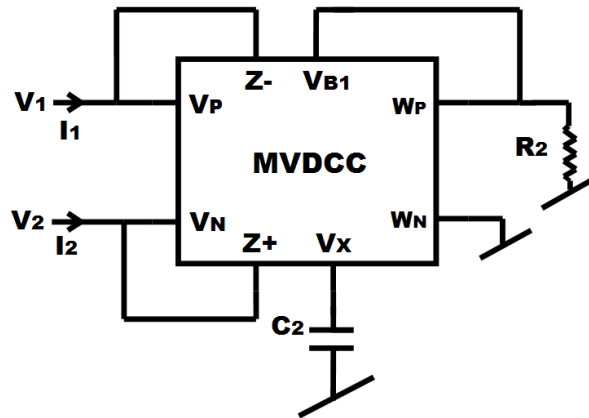


Figure 8. Proposed Floating inverse memristor emulator based on MVDCC

On applying Kirchoff's circuital laws and using Eq. 10, the admittance matrix of the inverse memristor has been found as;

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = k_1 \left(R_1 C_1 \frac{d}{dt} (V_2 - V_1) - V_{SS} - V_{th} \right) \begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \quad (19)$$

Therefore, using Eq. 19 the inverse memductance for the circuit shown in Fig. 8 can be given as;

$$G_{inv-mem} = k_1 \left(R_1 C_1 \frac{d}{dt} (V_2 - V_1) - V_{SS} - V_{th} \right) \quad (20)$$

6. Implementation of proposed memristor and inverse memristor emulator using LM13700 and AD844

The section presents the commercial IC-based implementations of memristor and inverse memristor discussed in the previous section. On careful investigation of these circuits it has been found that if we convert these floating circuits into grounded circuits, the commercial IC-based implementation is possible. Therefore, the grounded versions of these emulators have been realized by using ICs LM13700 and AD844S. The IC-based implementation of presented memristor emulator circuit described in Fig. 7 has been illustrated in Fig 9. Similarly, Fig. 10 illustrates the IC-based realization of proposed inverse memristor emulator shown in Fig 8.

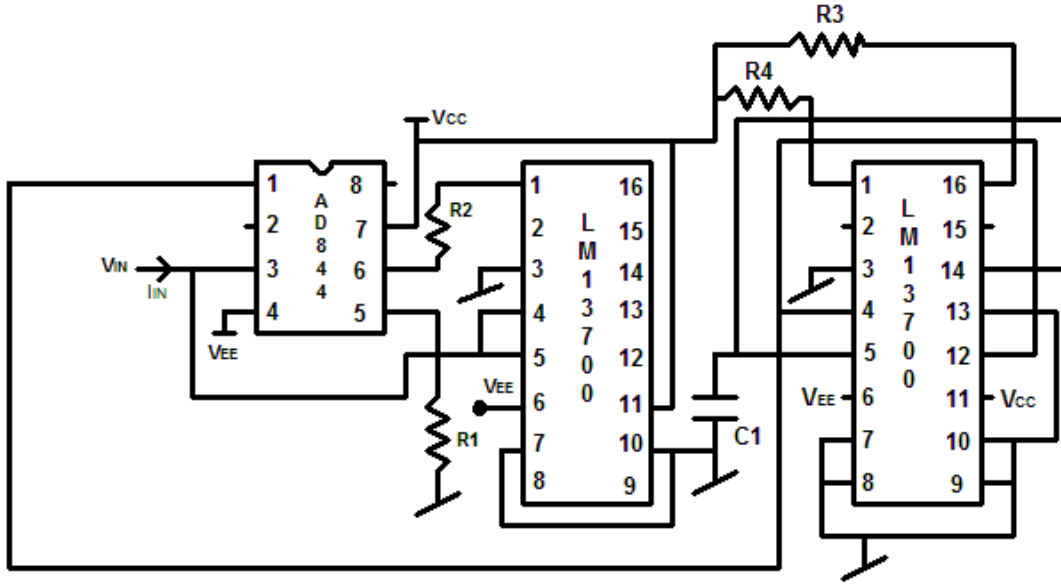


Figure. 9. Implementation of presented MVDCC based floating memristor using commercial analog ICs

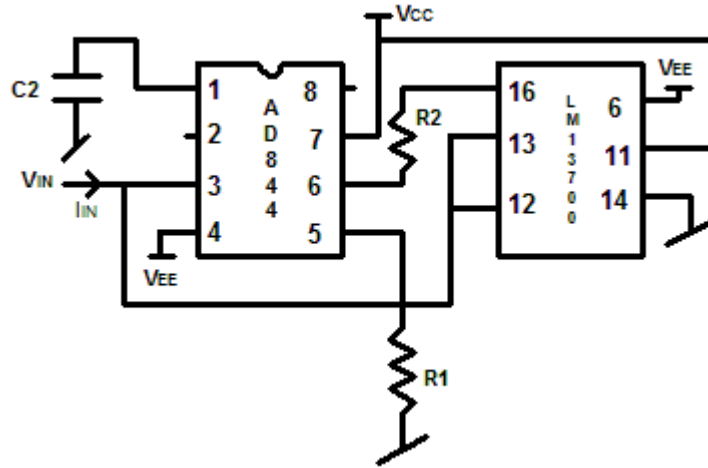


Figure. 10. Presented inverse memristor emulator (given in Fig. 8) realized using AD844 and LM13700

7. Memristor-Capacitor(MC) Low pass filter based on proposed Memristor Emulator

To demonstrate the usability of proposed memristor emulator, a memristor –capacitor (MC) low-pass filter (LPF) has been developed and shown in Fig.11.

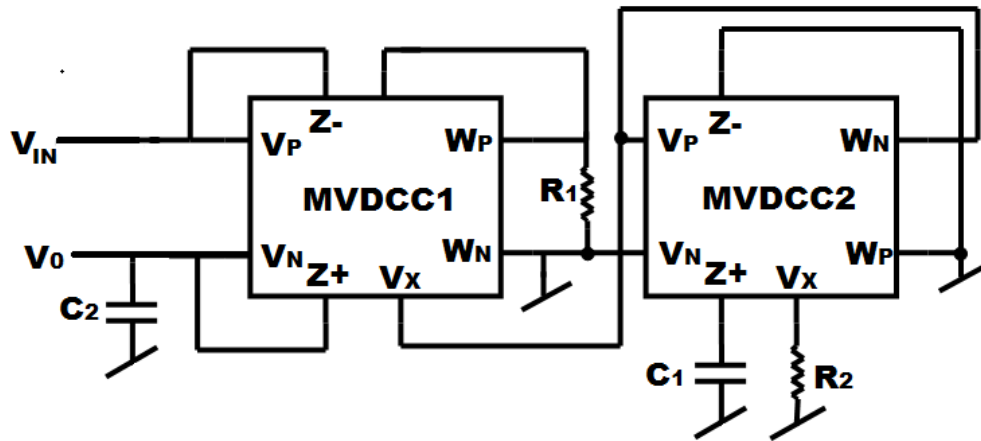


Figure. 11. MC LPF Filter realized by using MVDCC based memristor emulator (given in Fig. 7)

The filter shown in Fig 11 is different from the conventional R-C low pass filter, as in the memristor based filter, the effective resistance offered by memristor depends upon both the input voltage as well as the input frequency.

The expression for cut-off frequency (f_c) and gain G (dB) for the filter of Fig. 11 can be evaluated as;

$$f_c = \frac{G_M}{2\pi C_2} \quad (21)$$

and

$$G(dB) = 10 \log \left(\frac{G_M}{\omega C_2} \right) \quad (22)$$

Where G_M is the memductance of memristor which can be written as;

$$G_M = G_{Mean} \pm \Delta G \quad (23)$$

where from Eq. 13,

$$G_{Mean} = k(-V_{SS} - V_{th}) \quad (24)$$

and

$$\Delta G = V_m k_1 g_{m2} R_1 \frac{1}{\omega R_2 C_1} \cos(\omega t + \phi) \quad (25)$$

8. Simulation Results

For the validation of the reported floating memristor and inverse memristor emulators, PSPICE simulation environment with 0.18um CMOS technology is chosen. The CMOS implemented MVDCC shown in Fig. 6 is used with power supply voltages $V_{DD}=\pm 0.9V$. And the selected W/L ratio of the employed CMOS transistors in MVDCC implementation is given in Table 2.

Table 2. Aspect ratios of MOS transistors in the MVDCC implementation shown in Fig. 6

| Transistors | W/L Ratio(μm) |
|-----------------|----------------------|
| M1-M4 | 3.6/1.8 |
| M5-M6 | 7.2/1.8 |
| M7-M8 | 2.4/1.8 |
| M9-M10, M23-M24 | 3.06/0.72 |
| M11-M12 | 9/0.72 |
| M13-M17 | 14.4/0.72 |
| M18-M22 | 0.72/0.72 |
| M25 | 3.6/1.8 |
| M26 | 3.06/0.72 |

To verify its behaviour, the simulation has been performed for memristor emulator (shown in Fig. 7) at different values of frequency and obtained results have been depicted in Fig. 12 and 14. The operating values of passive elements have been chosen as; $R_1=10K$, $R_2=2.5K$ and $C_1=0.01nF$. The applied sinusoidal voltage has a peak value of $V_{in}=0.1 V$. And also, the values of biasing voltages corresponding to MVDCC1 and MVDCC2 have been selected as; $V_{BS1}=V_{BS2}=0.2V$. Now, it is known that the span of the PHL of an ideal memristor must decrease on increasing the value of applied signal frequency. And the same can be witnessed in the plots presented in Fig. 12 and 13. Now, this contraction of $v-i$ lobes must lead to a shape of a line on the $v-i$ plane passing through the origin, which seems to happen when the frequency is increased further as it is shown in Fig. 13. Now, to investigate the influence of employed passive elements and other quantities such as input voltage and biasing voltage, the excitation signal frequency has been chosen as $F_{in}=100KHz$, biasing voltage is kept at $V_{BS1}=V_{BS2}=0.4V$ and peak input value is chosen as $V_{in}=0.1V$.

Firstly, the effect of the variation of used grounded resistance R_1 has been studied and related simulation results are presented in Fig. 14. It is confirming its resistance tunable nature. On the other hand, when R_2 and capacitor C_1 were chosen as a variable component, it was

observed that variation in the R_2 and C_1 does not result into significant change in memristor. Therefore, the realized memristor is not tunable through passive elements R_2 and C_1 .

In Fig. 15, the feature of electronic controllability is demonstrated. It can be seen from the figure that variation in biasing voltages V_{BS2} , is producing a significant change in the hysteresis behaviour of proposed floating memristor.

Now, the non-volatility property has been checked through simulation. This has been confirmed through subjecting the proposed emulator to a periodic pulse input having on time $T_{ON}=0.1ns$, time-period, $T_{period}=0.5ns$ and the peak value of $V_{on}=10mv$. The simulations have been performed for both types of connections of memductor namely decremental and incremental type. The corresponding simulations results have been provided in Fig. 16 and 17 respectively, which illustrates the response of memristor current with time. In the plots, the change of memductance is described through the current response, which can be seen as the staircase shape curve plotted over the current pulses. It can be observed from both the plots that for each succeeding applied pulse the height of the generated current pulses found to be decreased and increased (depending upon the case), which follows from the decremental and incremental nature of the employed connection. Next, we have plotted the response of instantaneous memristance over time subjected to sinusoidal excitation. The graph, shown in Fig. 18 has been plotted for $F_{in}=100KHz$. During a single period of the input signal, the behaviour of R_{in} can be observed through the PHL presented in Fig. 12 for 100KHz. The discontinuity at the middle may be because, at this instant the VI contour passes through the origin where the instantaneous resistance cannot be defined.

Now, the transient response of voltage and current of memristor have been presented. The current response given in Fig. 20 for the sinusoidal input is presented in Fig. 19. Also, the frequency response plot of the MC low-pass filter based on proposed emulator given in Fig. 11 has been shown in Fig.21 for different values of external capacitance C_4 . The frequency response has been plotted for the parameter values as; $C_1=0.01nF$, $R_1=1.5K$, $R_2=1.5K$ and biasing voltage as $V_{BS1}=0.4V$, $V_{BS}=0.4V$.

Furthermore, the transient characteristics of the proposed inverse memristor emulator have also been explored. For the simulation of the inverse memristor emulator presented in Fig. 8, the value of employed passive elements, grounded resistance and capacitance have been taken as $R_1=1.5K$ and $C_1=10nf$ respectively. The biasing voltage of MVDCC is chosen as $V_{BS2}=0.4V$ (of second stage) and the peak value of applied input is selected as $V_p=0.16V$. As described in the theory section that area enclosed under the lobes of inverse memristor expands with the increase in operating signal frequency. This frequency dependence can be validated through PHL presented in Fig. 22, 23 and 24. It is verified from the three plots that area enclosed under the lobes increases on raising the operating frequency value. Now, selecting the operating frequency of the proposed inverse memristor emulator as $F_{in}=10KHz$ and keeping all other parameters constant, the rest of the simulation results are presented. The influence of resistance R_3 is studied and derived plots are depicted in Fig. 25. The effect can be clearly observed that the higher value of R_3 gives rise to an expansion in the area of PHL. Further, the change in the transient VI characteristics is observed for the variation of biasing voltage V_{BS2} . The corresponding VI curves, shown in Fig. 26, illustrate the effect of biasing voltage on inverse memristor behaviour. Although the effect is not considerable, as second stage of the MVDCC has little effect of applied bias voltage as it is a current conveyor stage.

Furthermore, the working of commercial IC-based implementations of presented emulators given in Fig. 9 and 10 has been validated. Here, we have used the SPICE model of the ICs provided by the Texas-Instruments, which provides the output, in a close match with the physical ICs as per the claim of the manufacturer.

To simulate the memristor emulator based on LM13700 and AD844 given in Fig. 9, the power supply voltage $V_{CC,EE}$ is chosen $\pm 12V$ and passive elements are taken as; chosen as $R_1=112K$, $R_2=100K$, $R_3=30K$, $R_4=40K$ and $C_1=0.01nF$. And also, the maximum value of applied sinusoidal input is chosen as $V_m=0.5V$. The three plots are given in Fig. 27 illustrate the frequency related characteristics of the PHL of the memristor. As it can be noticed, that at 25 KHz, the area enclosed by lobe is larger than the area of $v-i$ curve, obtained at 50 KHz. And finally, the size of the lobes become smallest as the frequency is increased up to 75 KHz as shown in Fig. 27.

Now, the operation of the inverse memristor emulator given in Fig. 10 can be verified similarly. The circuit is based on LM13700 IC and an AD844 ICs and uses three passive elements. For this simulation purpose of the emulator, the circuit parameters of implemented configuration are taken as; $V_{CC,EE}=\pm 12V$, $R_1=112K$, $R_2=100K$ and $C_2=1nF$. And the pure sinusoidal signal is chosen with a peak value of $V_m=0.5V$. The transient $v-i$ characteristics of the inverse memristor are plotted in Fig.28, 29 and 30. These three $v-i$ curves are plotted for increasing value of frequency. And it can be witnessed that increasing frequency value giving rise to an increase in the area lobes. It is confirming the described property of an inverse memristor.

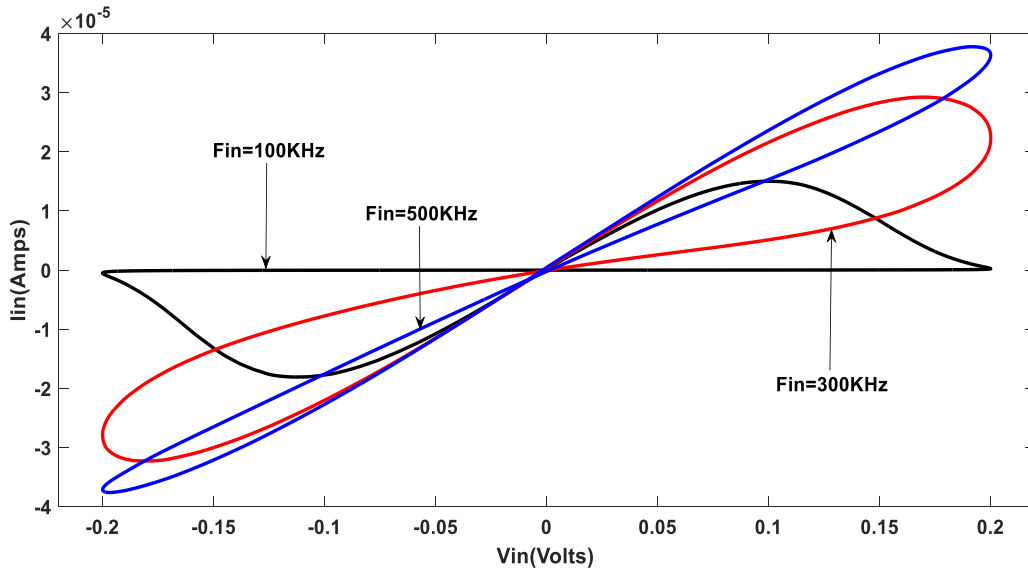


Figure. 12. PHLs with large lobe area at same operating frequencies for different set of parameters

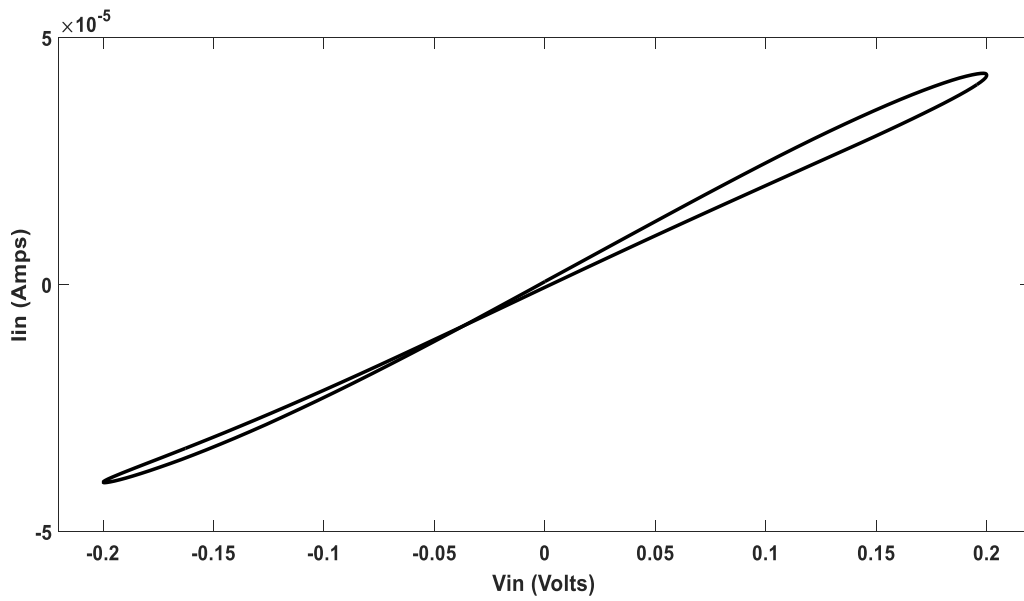


Figure 13. Memristor behaviour at 1MHz for changed values of parameters

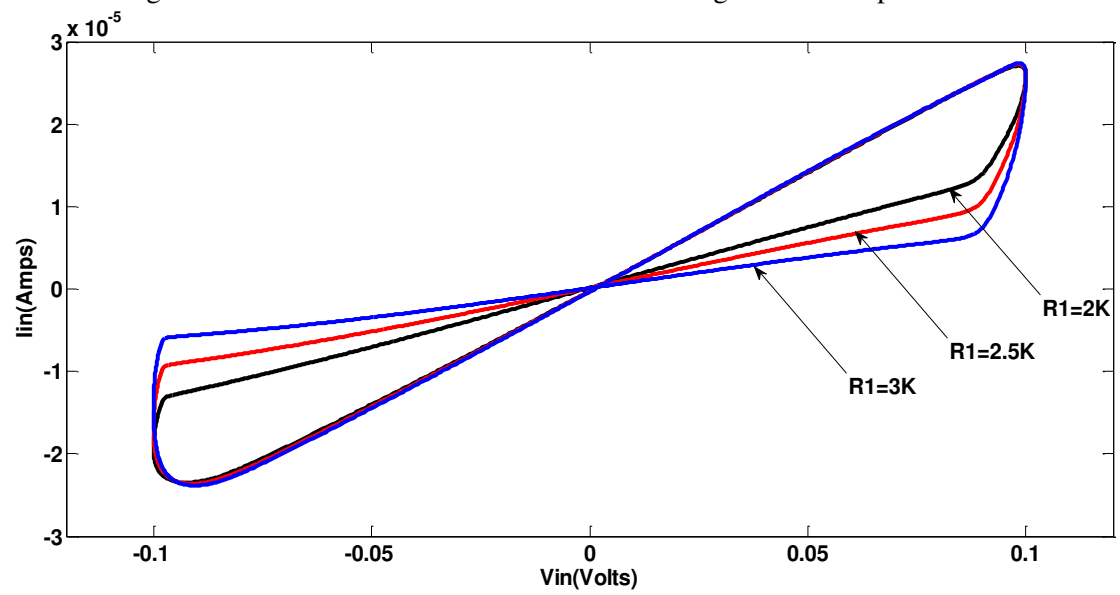


Figure. 14. PHLs generated for different values of resistance R1

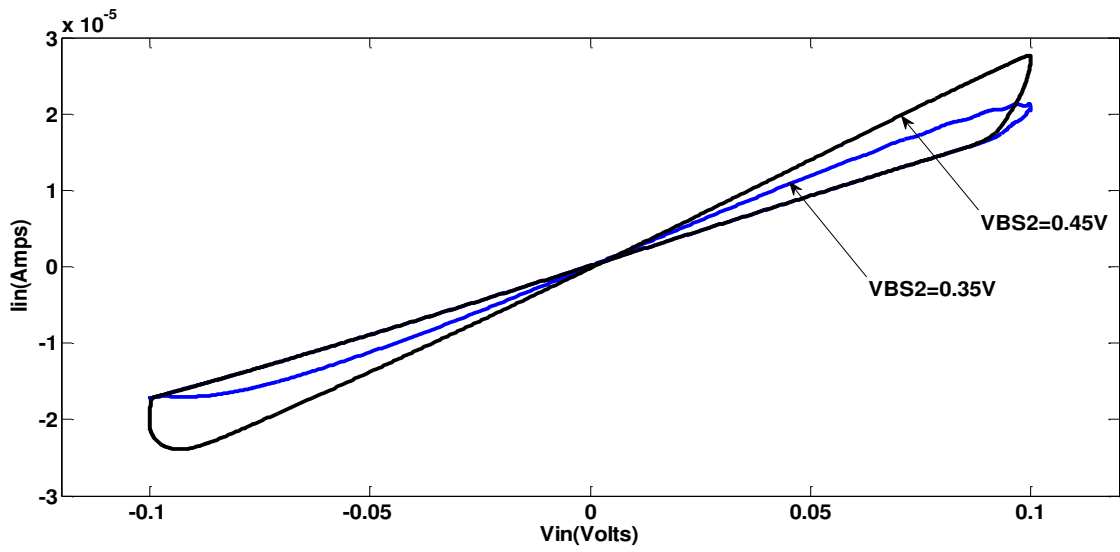


Figure. 15. Electronically tunable hysteresis behaviour for various biasing voltage V_{BS2}

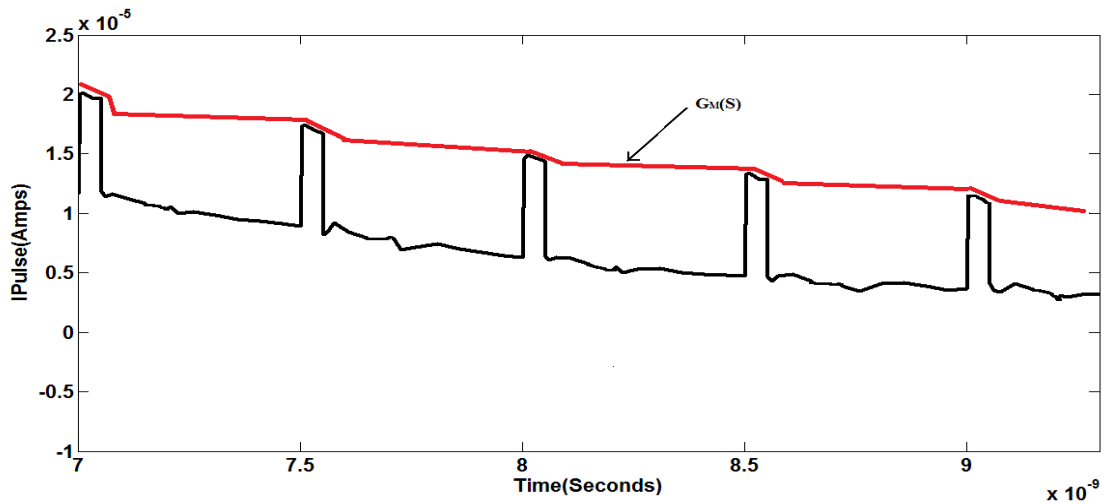


Figure. 16. Response of generated decremental memductance current for pulse input excitation and corresponding memductance behaviour

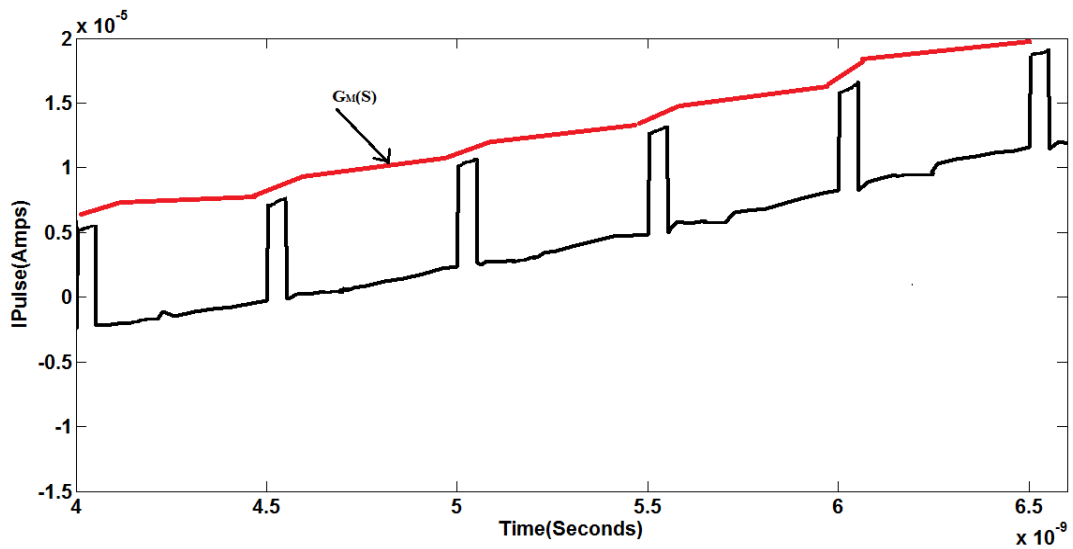


Figure. 17. Plot showing the current response of incremental configuration for pulse input voltage and non-volatile nature of memductance $G_M(S)$

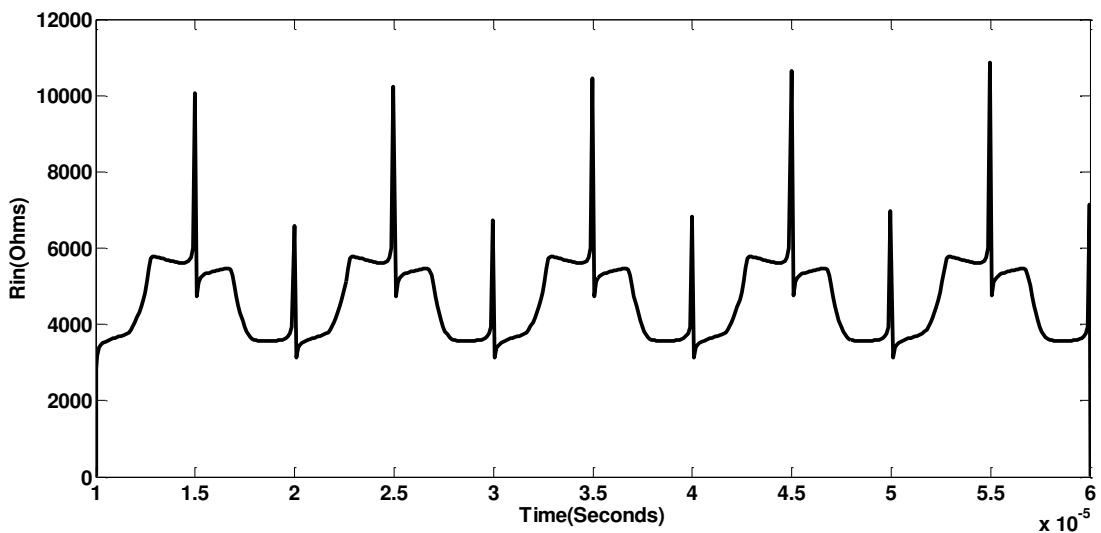


Figure. 18. Plot showing memristance variation with respect to time at $F_{in}=100\text{KHz}$

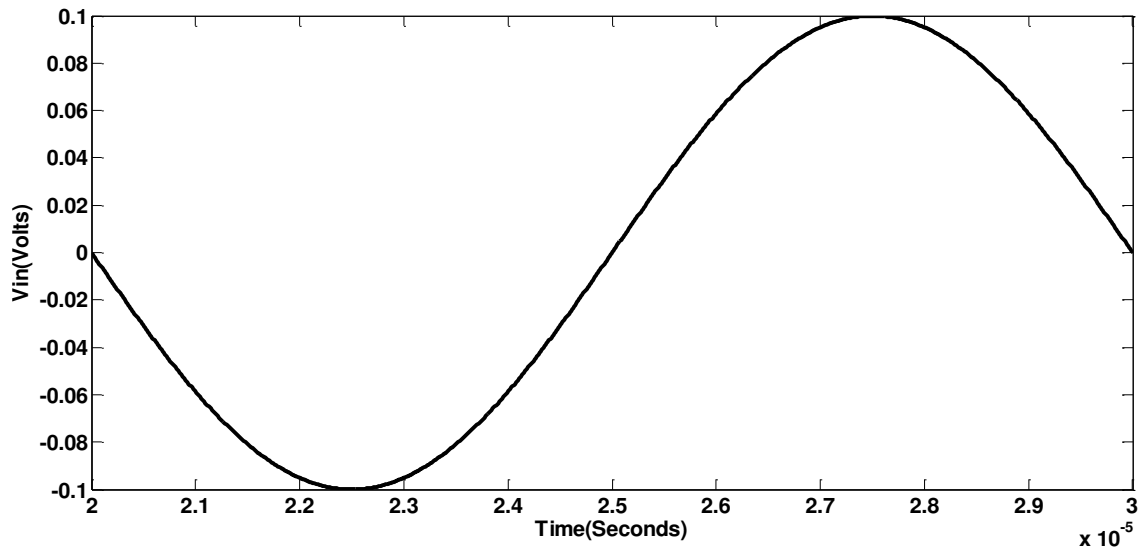


Figure. 19. Sinusoidal excitation of operating frequency $F_{in}=100\text{KHz}$

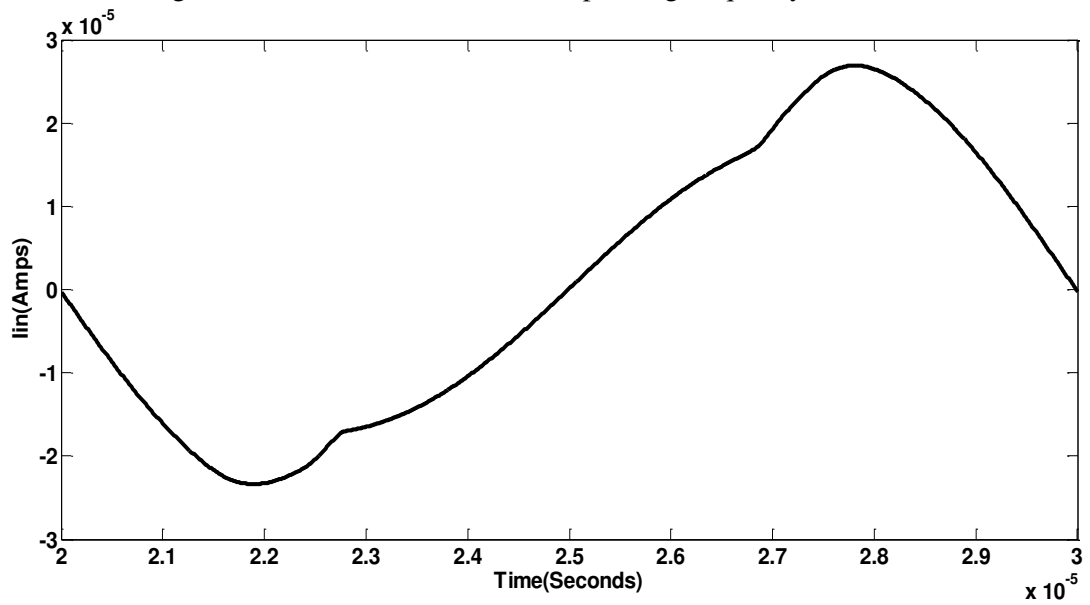


Figure. 20. Behaviour of generated memristor current for sinusoidal excitation depicted in Figure. 23

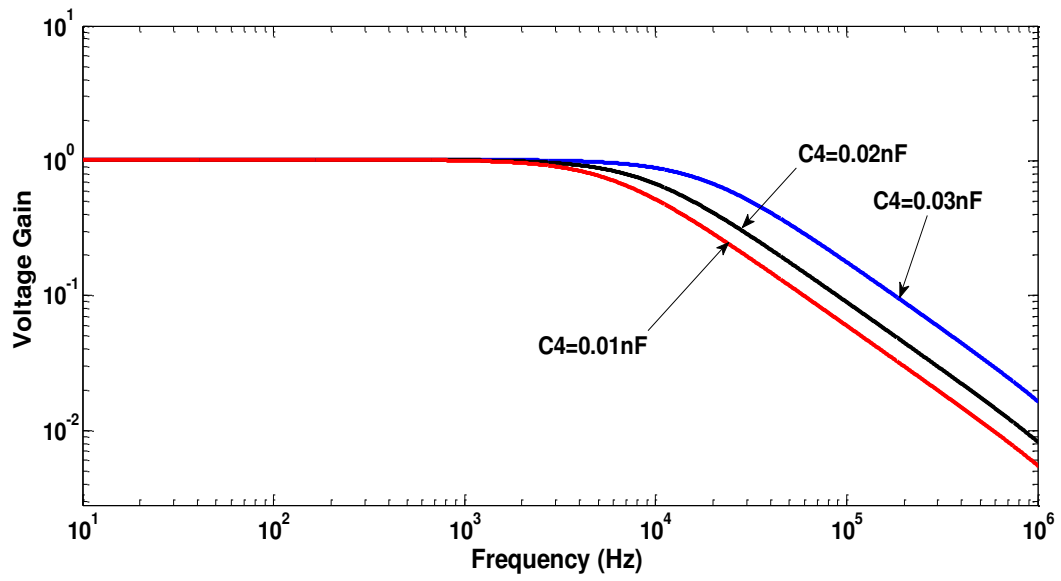


Figure. 21. Frequency response of LPF shown in Fig. 11 for different values of capacitances

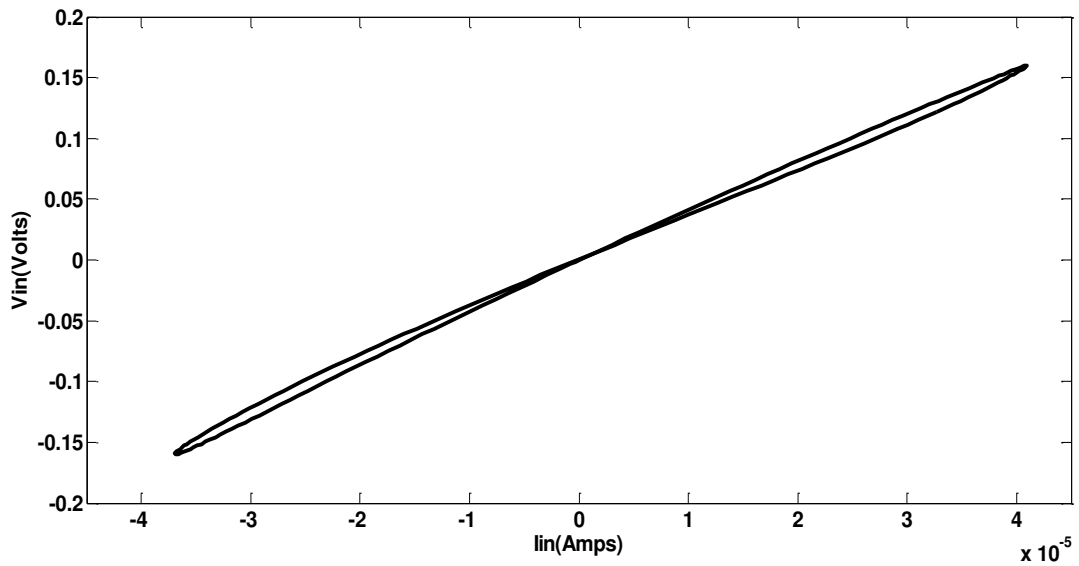


Figure. 22. $v-i$ loop of presented MVDCC based inverse memristor emulator at $F_{in}=5\text{K}$

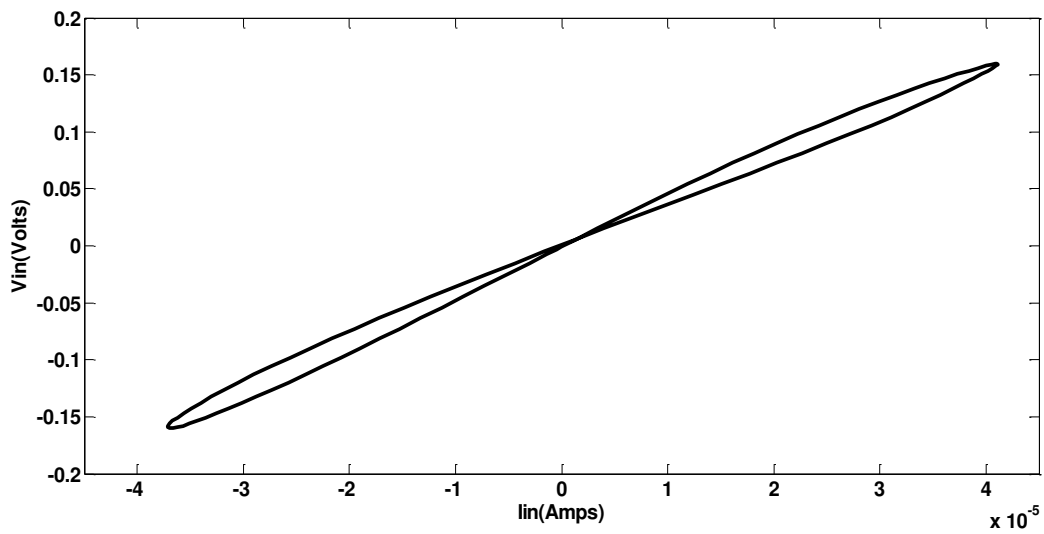


Figure. 23. Transient $v-i$ characteristics at operating frequency $F_{in}=10\text{K}$

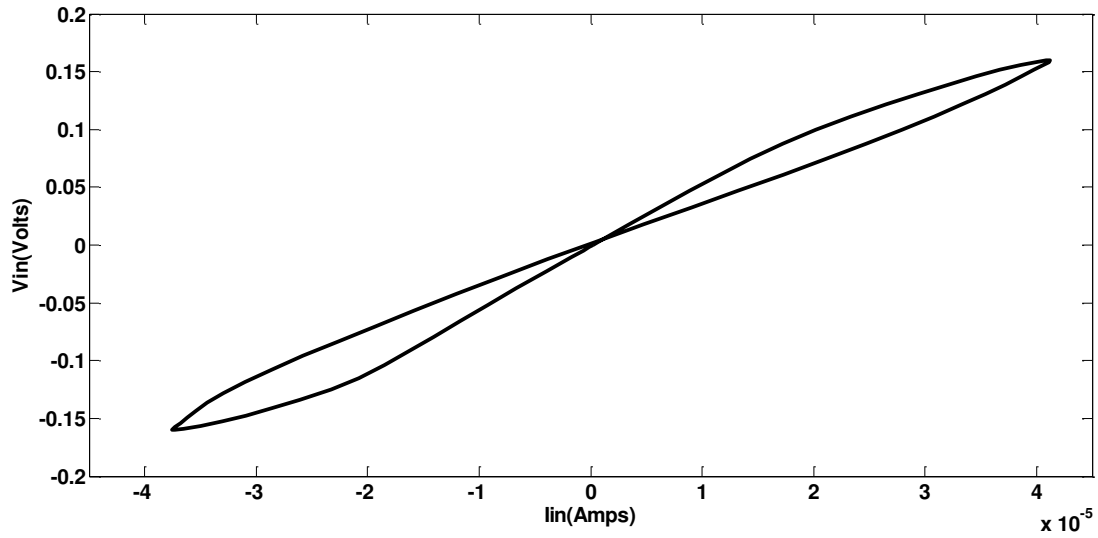


Figure. 24. v - i loop of developed inverse memristor emulator at $F_{in}=15K$

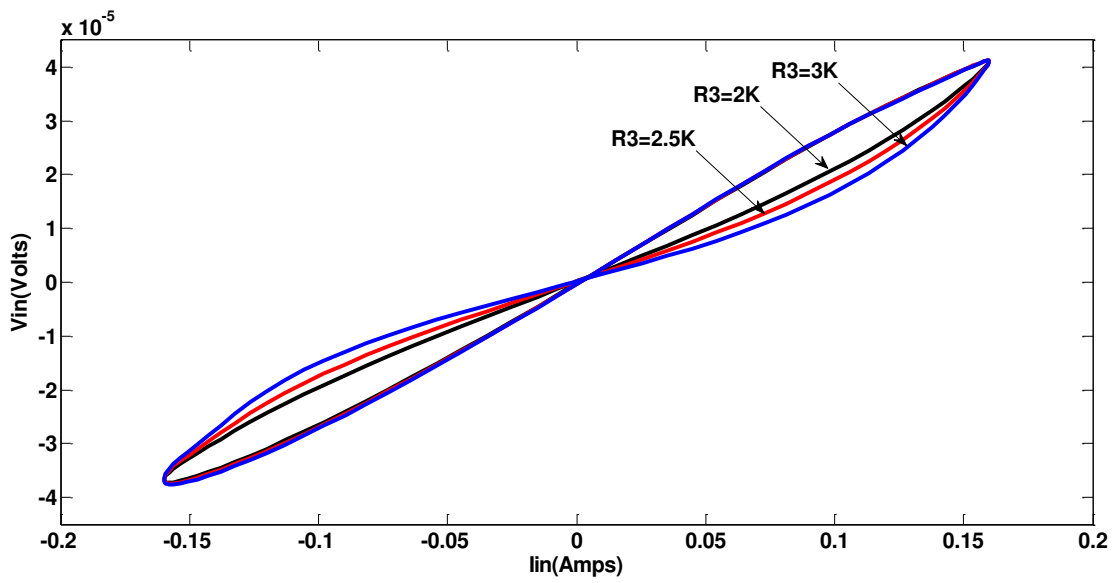


Figure 25. Influence of employed grounded resistance R_3 on the PHL of inverse memristor

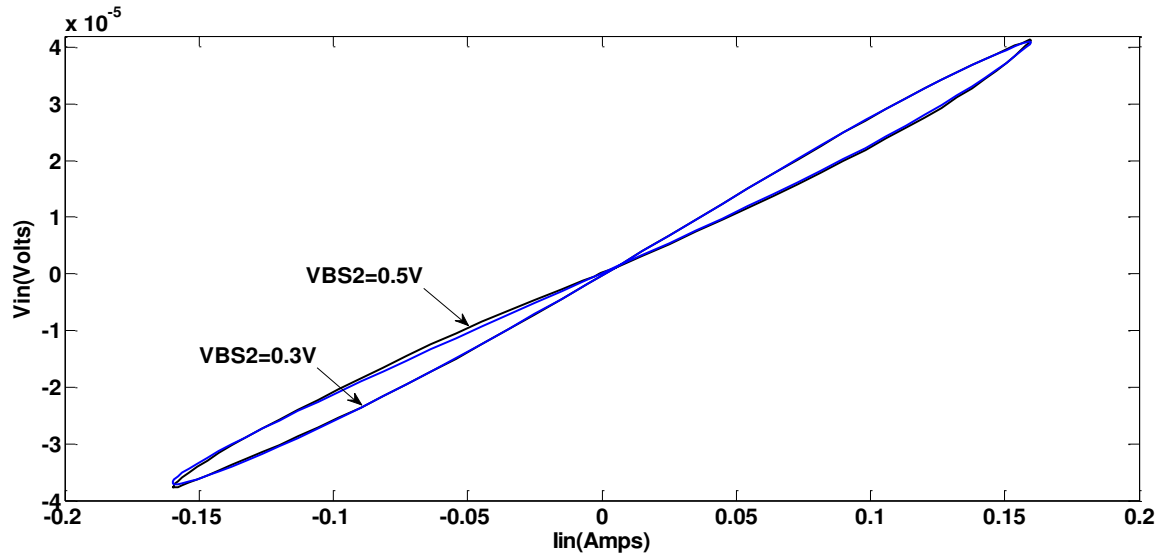


Figure. 26. Plot showing the effect of biasing voltage V_{BS2} of second stage on the $v-i$ loop of inverse memristor

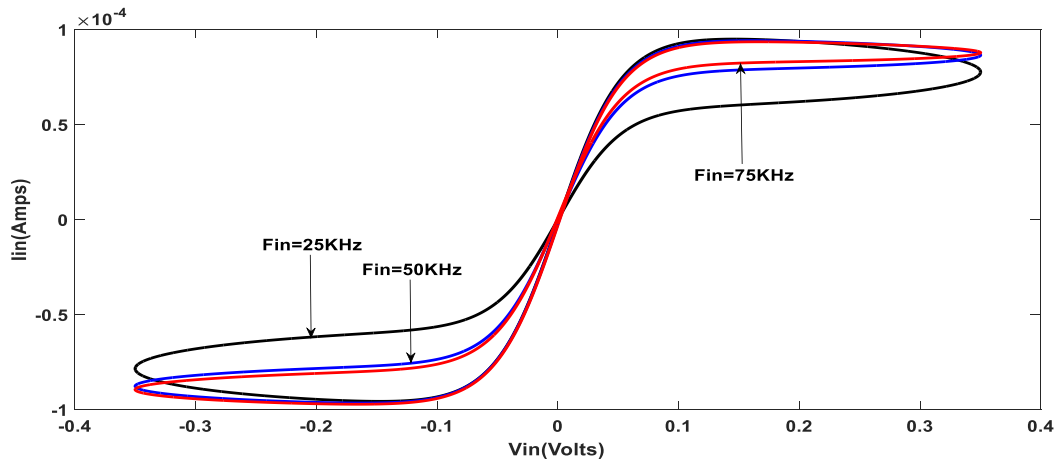


Figure. 27. Behaviour of emulator circuit (shown in Fig. 9) based on LM13700 and AD844 at $V_m=0.35\text{ V}$

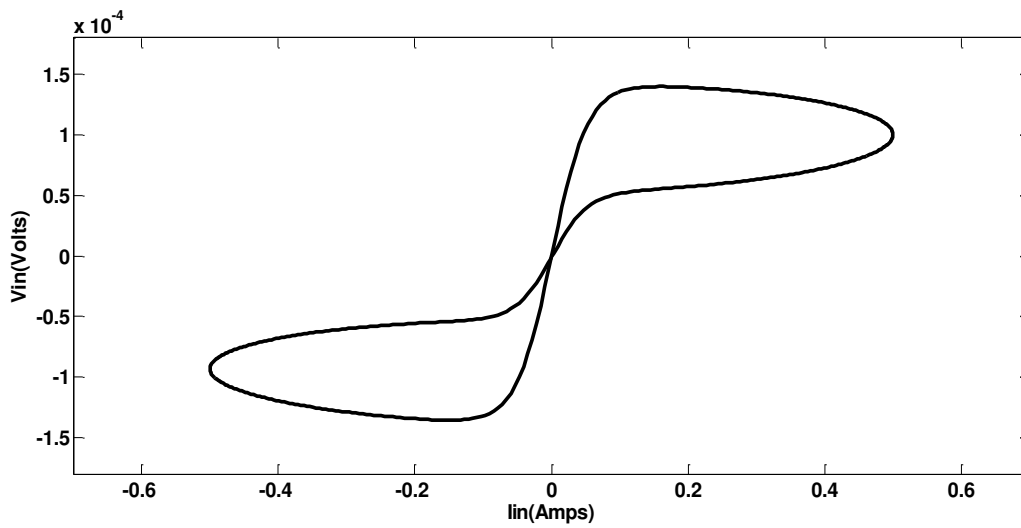


Figure. 28. $v-i$ loop obtained for the commercial IC-based implementation of the MVDCC based inverse memristor (presented in Fig. 10) at operating frequency $F_{in}=20\text{K}$

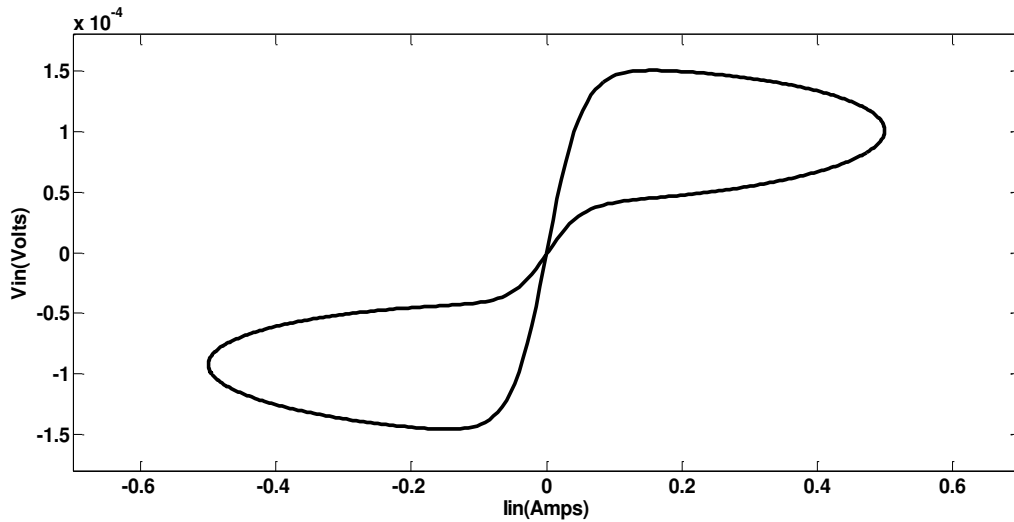


Figure. 29. Transient $v-i$ response behaviour generated at $F_{in}=25K$

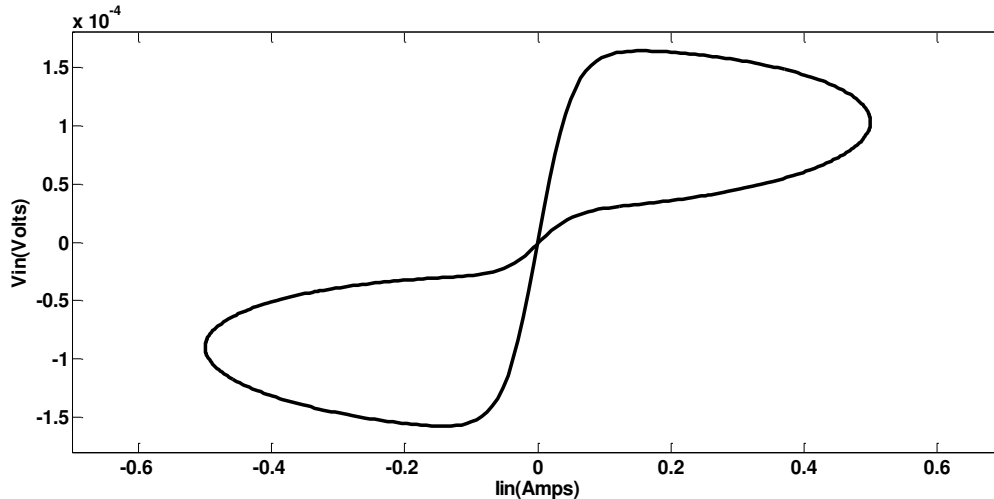


Figure 30. Increased span of $v-i$ lobe area at operating frequency $F_{in}=30KHz$

9. Conclusion

The research work was dedicated to the realization of floating emulator configurations of an ideal and a non-ideal memristor based on the MVDCC active element, which is a slightly modified version of popular active element VDCC. The reported floating memristor emulator consists of two MVDCCs and three grounded passive elements including single capacitance and two resistances. The other presented emulator configuration which realizes a non-ideal memristor is designed using single MVDCC and two grounded passive elements. Both the presented emulator enjoys electronic tunability along with the passive element tunability. The sought after feature of both the reported circuits is no use of any external voltage multiplier circuit/IC which verify the compactness and on-chip realization suitability. This article also describes the utility of inverse memristor for controlling ideal memristive behaviour. For verification of the realized behaviour of proposed emulators, these circuits are simulated using the PSPICE environment using 0.18 μ m technology and all results have been discussed. The given floating memristor and inverse memristor emulators have also been implemented using commercially available ICs; LM13700 and AD844.

Declarations

1. Funding

Not Applicable

2. Conflicts of Interest

Not Applicable

3. Availability of data and material

Data sharing not applicable to this article as no datasets were generated or analysed during the current study.

4. Code availability

Not Applicable

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