Power Estimation of QPSK and BPSK Modulation Systems for FPGAs based on IP Modeling for Wireless Applications

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ABSTRACT

FPGA market has expanded due to its adoption in mobile phones and wearable devices. The communication IP blocks in Field Programmable Gate Array (FPGAs) has made it possible to realize different communication systems. However, in spite of their high performance, FPGAs suffers from high power consumption due to their complex architecture as compared to their ASIC counterpart. This has made power estimation as an important design metric. The existing commercial tools provide the option to estimate the power, but at the cost of longer estimation time as the designs have to follow the complete design cycle. Moreover, literature, mostly focuses on power estimation of individual blocks and power estimation of the complete system is still in infancy stage. Therefore, in this work, Quadrature Phase Shift Keying (QPSK) and Binary Phase Shift Keying (BPSK) modulation systems have been designed that are used in various wireless and satellite communication applications. Further, a new identity is proposed that could evaluate the power of whole system. The QPSK and BPSK systems have been designed via embedded IP and user-defined IP cores. A power estimation model of diverse blocks of QPSK and BPSK modulation systems have been developed based on a supervised machine learning technique using MATLAB R2016b and models are validated against commercial tool. Finally, the power of complete QPSK and BPSK modulation system is estimated using the proposed identity and is also validated for accuracy with reference to Vivado 2014.2 tool targeted to the Zynq family device and state of the art work. It has been seen from the results that the proposed identity outperforms in power estimation of complete systems as compared to existing identities available in literature and is providing aligned results with reference to the commercial tool.

Keywords— QPSK, BPSK, Embedded IPs, Power, FPGA, RTL.

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1. INTRODUCTION

The inclusion of communication based firm Intellectual Property (IP) cores in FPGAs has given the opportunity to the designers to use them for designing telecommunication applications. The global market of FPGAs is expected to reach USD 25 billion by 2023. Application Specific Integrated Circuits (ASICs) are the popular choice of designers, but cannot be altered after manufacturing. However, FPGAs has the ability to be reprogrammed after their deployment. Nowadays, FPGAs are the first choice due to their compact design turnaround time, high operating speed and less Non-Recurring Engineering (NRE) cost. But the major drawback with FPGAs is that they consume more power in comparison with ASICs. Thus, power and performance has become imperative design metrical for FPGAs [1]. Also, power estimation with accuracy at primary design phase is a challenge for electronic design engineers.

The power of each element of a chip can be measured separately either through a low-level tool or through methodologies based on hardware measurement. Few low-level commercial tools are available like Xpower, Vivado from Xilinx and Power Play from Altera. But through these tools, power estimation is time taking process as the design has to undergo an entire design cycle. Therefore, models are required that could estimate the power at primary design phase. At RTL level things are technology sovereign, which provides freedom to the designer to some extent. Also, the simulation run time at this level is less. So, designing of a complete system for power estimation at this level can be a virtuous choice. Numerous models have been established in the literature for power estimation of individual blocks, but very few literatures are available for power estimation of different applications designed using IP cores [2], [17].

QPSK and BPSK find application in various wireless standards, for example Global System for Mobile Communication (GSM), Code- Division Multiple Access (CDMA), cable modem, satellite etc. Therefore, in this paper, QPSK and BPSK modulation systems have been designed using IP cores. The estimated power of each module of the modulation systems obtained from curve-fitting and regression technique has been used for estimating power using proposed identity. The power values obtained using proposed identity has been authenticated contrary to the power values obtained using the commercial tool and available techniques in the literature.

The paper is systematized as follows: the literature survey of the related FPGAs based power estimation methods is deliberated in segment 2. Emphasis on projected methodology is laid in segment 3. Focus on IP power is in segment 4. Characterization of systems is given in segment 5. Regression based model for different blocks is being discussed in segment 6. Power estimation

using proposed identity is discussed in segment 7. Finally, comparison with existing identity and conclusion is given in segment 8 and 9 respectively.

2. LITERATURE SURVEY

Currently, the main aim is power saving owing to enlarged computation and architectural intricacy. Elleouet et al. have projected a method to estimate the power of a system containing N number of IP. In their work, algorithmic and architectural parameters have been considered for analysis. But they have not focused on interconnection power that may be the prime factor leading to large errors for intricate designs [2]. A similar concept has been reported in Lorandel et al. paper. They have presented a power estimation method for wireless communication systems. They carried the analysis on system C. The maximum error obtained for a particular application is 5.11%. In their work, the component's time activity has been considered as a source of error. Also, the emphasis has not been rested on interconnection power. Thus, in proposed work emphasis has been laid on interconnection power [3]. Durrani et al. have presented a macro-modeling procedure to evaluate the power of an IP. The proposed technique estimates the power for digital circuits at the architectural level based on the statistical information of inputs and outputs [4]. Jevtic et al. have proposed a methodology based on on-board measurement to separate static power, logic power, clock power and power consumed by global interconnects for FPGAs devices [5]. Deng et al. have presented a model based on curve-fitting and regression technique to accurately estimate area, time and power of FPGAs based implementations of IP cores. The IP cores-based designs will greatly enhance the hardware development efficiency [6]. Verma et al. have projected a power model by modifying the Deng model. They have proposed the model for embedded multiplier targeted to SPARTAN 3 FPGAs. Their model is also based on curve fitting and regression technique. Their proposed model is very similar to the power model proposed by Lorandel but they have carried out analysis for embedded multiplier block only [7]. Verma et al. have proposed an improved power estimation model created using curve- fitting and regression technique, i.e., FPEV_tool for normal and power efficient digital circuits [8]. Najm et al. have presented a statistical simulation technique that could measure the switching activity of individual nodes in combinational logic circuits. [9]. Nasser et al. have presented a new power estimation tactic. The proposed approach is based on the disintegration of digital circuits into basic operators [10].

To summarize, various methods and modeling procedures have been projected in literature. It has been analyzed from the literature surveys that Elleouet et al. and Lorandel et al. provide solution for power estimation of the complete system. However, both of them have not worked on interconnection power which becomes a crucial parameter after interconnecting different blocks. Also, they have worked on higher abstraction level. But, accurate measurement of power is possible only at low-level with the knowledge of the capacitances of chip. At higher abstraction level power estimation would not be accurate as most of the information related to low-level is missing. So, there is requirement of improved identity that could estimate the power of a complete system at RTL level.

3. PROPOSED METHODOLOGY

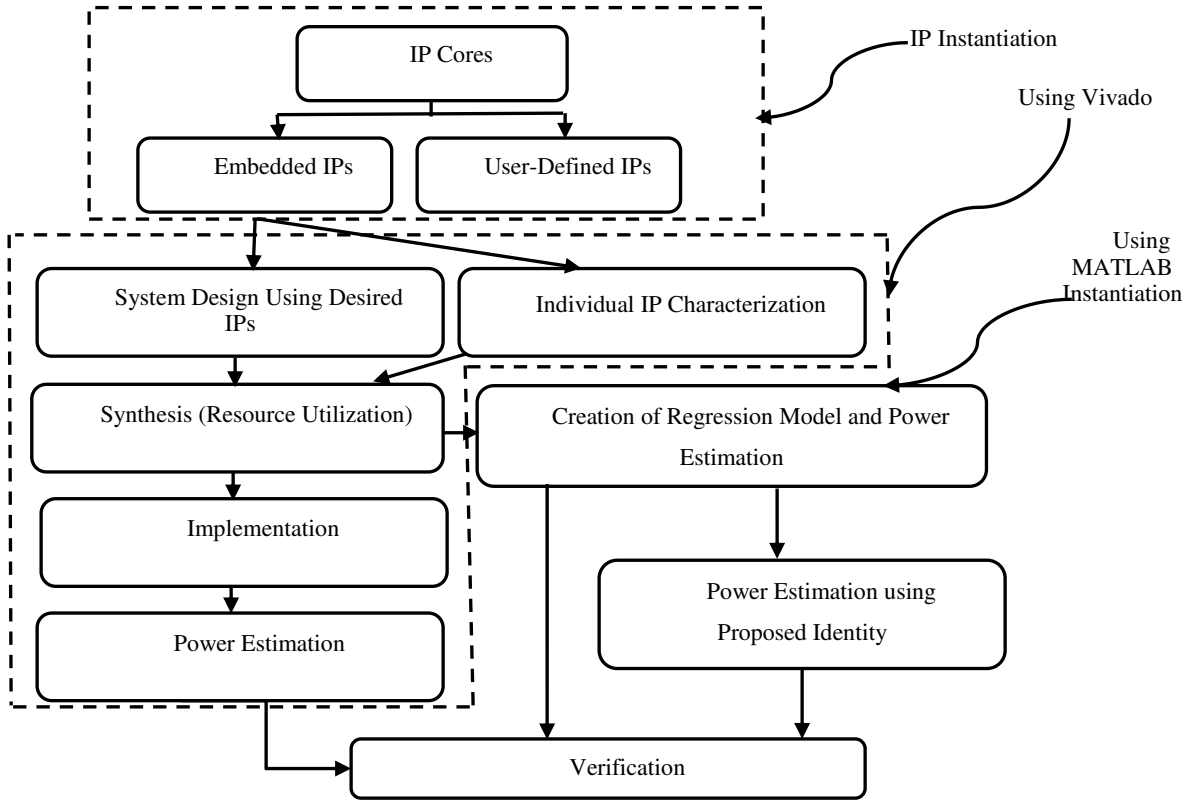

Fig. 1. Power estimation flow.

QPSK and BPSK modulation systems have been designed using embedded IP and user-defined IP. User-defined IP has been incorporated in the vendor library using Verilog Hardware Descriptive Language (HDL). Individual IP cores are characterized for model creation and power estimation based on the resource utilization obtained after synthesis as shown in fig.1.

Power values obtained through regression-based models are authenticated for accuracy using the commercial tool. Finally, communication systems are designed and implemented using dedicated

IP blocks for power estimation. The power values obtained from the proposed identity have been tested for accuracy against the power values obtained using the commercial tool.

4. POWER MODELING OF AN IP

Each IP that has been used for implementing QPSK and BPSK modulation systems are analyzed for different Input and Output (I/O) configurations at 125 MHz frequency [15], [2], [3]. The power of an IP is given by (1).

$$\text{Total power} = \text{Dynamic power} + \text{Static power} \quad (1)$$

For a particular FPGA device static power is fixed. In this work, static power is 120 mW. But dynamic power is instantaneous and can be given by (2).

$$\text{Dynamic power} = \alpha \text{ x } f_{clk} \text{ x } C_L \text{ x} V_{DD}{}^2 \quad (2)$$

Every designer has its own timing requirement for a particular design and also supply voltage V_{DD} is fixed in most cases. C_L is the total capacitance. So, it's only the switching activity α that can be directly controlled by the designers [11]. The control over α is an almost impossible task when designing using IP blocks because, Vivado tool works on vector-less algorithms to provide the value of α at different nodes of the circuits under consideration. Hence, in FPGAs, Dynamic power can be given by (3). Parameters and their denotation used in this work are given in Table 1.

$$\text{Dynamic power} = \text{Signalpower} + \text{Logicpower} + \text{I/Opower} + \text{Clockpower} + \text{Memorypower} + \text{DSPpower} \quad (3)$$

Table 1 Parameters used and their denotation

Parameters used	Denotation
out_pin	Total figure of output pins
lut	Total figure of Look-Up Table (LUTs) (logic slice)
ff	Total figure of Flip-Flops (FF)
in_pin	Total figure of input pins
DSP48	Total figure of DSP blocks
Clockpower	Average power consumed by clock network including buffer and routing resources
Logicpower	Average power consumed by all CLBs including LUTs and FFs
Signalpower	Is the interconnects average power
DSPpower	Average power disbursed by DSP blocks
Outputpower	Average power spent by the output pins
Inputpower	Average power spent by the input pins

5. CHARACTERIZATION OF SYSTEMS

In this work, QPSK and BPSK modulation systems have been designed for analyzing the feasibility of the proposed identity. QPSK is a digital modulation method where two information bits are modulated at a time.

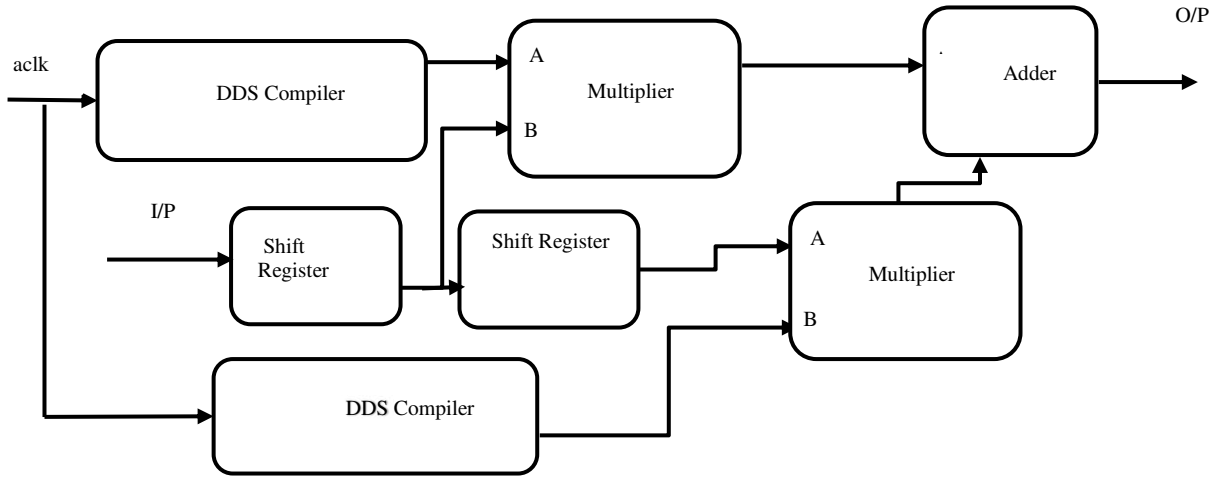

Fig. 2 Block diagram of QPSK.

The complete system is designed for power estimation using IP modeling approach. QPSK has been implemented using SIPO register, multiplier, adder and Direct Digital Synthesizer (DDS) as shown in fig. 2. DDS has been configured for generating sine and cosine signals. In BPSK modulation system, 0's and 1's of a binary information epitomizes two different phase state in the carrier signal [12], [14]. BPSK has been implemented using DDS compiler, RAM based shift register and a multiplexer (MUX) as shown in fig. 3.

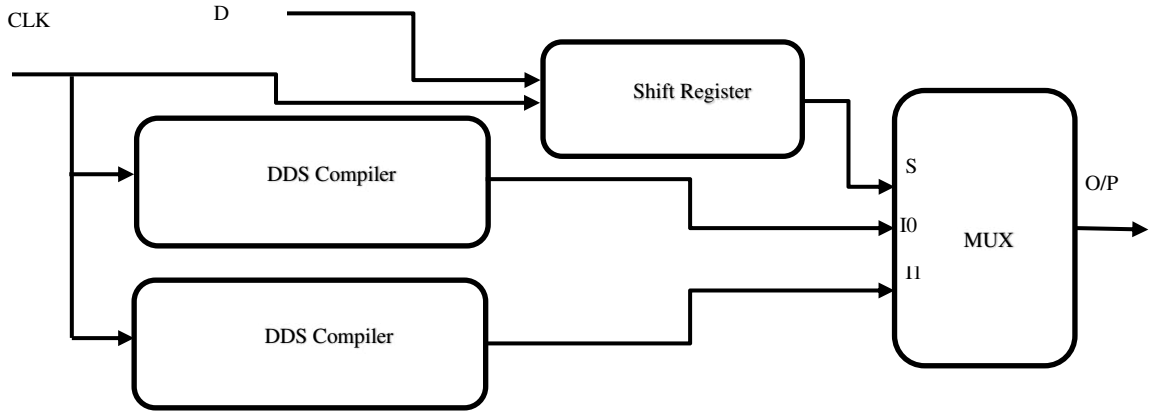

Fig.3 Block diagram of BPSK.

6. REGRESSION MODEL FOR MODULES OF QPSK AND BPSK MODULATION SYSTEMS

Regression model has been created for different IP cores that are used in designing of QPSK and BPSK modulation systems**.** The power of individual IP cores has been estimated using curve fitting and regression model. Models have been created using training data sets and have been tested for accuracy using testing data sets.

6.1 REGRESSION MODEL FOR RAM-BASED SHIFT REGISTER

Curve-fitting and regression-based model for Shift register IP has been created by modifying and synthesizing the IP for diverse I/O configurations. Model is created based on the resource utilization data. The dynamic power equations obtained are given in (4) to (8) [13], [16].

$$\text{Inputpower} = -1.339\text{e} - 8 \text{ x } (\exp(-0.503 \text{ x in\_pin})) + 0.1 \quad (4)$$

$$\text{Outputpower} = 0.3041 \text{ x } (\text{out\_pin}) - 0.1217 \quad (5)$$

$$\text{Clockpower} = 1.054 - 0.045\text{x ff} + 0.0329 \text{ x lut} + 0.00167 \text{ x ff x ff} - 0.001243 \text{ x ff x lut} + 0.000208 \text{ x lut x lut} \quad (6)$$

$$\text{Signalpower} = 1.171 + 0.6631 \text{ x } \sin(0.1835 \text{ x pi x ff x lut}) - 1.171 \text{ x } \exp(-(10.37 \text{ x lut})^2) \quad (7)$$

$$\text{Logicpower} = 0.1 - 4.043\text{e-}09 \text{ x } \sin(0.03615 \text{ x pi x ff x lut}) - 9.641\text{e} - 09 \text{ x } \exp(-(0.1373 \text{ x lut})^2) \quad (8)$$

The comparison result of training and testing data sets is given in Table 2. The estimated power attained from regression model has been authenticated contrary to the power obtained from commercial tool using (9). Similar procedure has been adopted for validating all the IP cores used in the designs.

$$\text{Error (\%)} = \left|\left(\frac{\text{Estimated power} - \text{Reference power}}{\text{Reference power}}\right)\right| \text{ x } 100 \quad (9)$$

Where, *Estimated power* is the power gained from the projected model and *Reference power* is the power gained from the commercial tool.

Table 2 Comparison result of shift register for training and testing data sets

Shift register IP configurations	Power values from commercial tool (mW)	Power values from regression-based model (mW)	% Error
Training data			
1	121	121.39	0.32
4	122	122.98	0.81
8	123	123.90	0.73
16	126	127.28	1.02
32	134	133.25	0.56
40	136	136.66	0.48
64	146	144.95	0.72
68	148	147.09	0.62
76	150	149.92	0.05
90	155	153.96	0.67
Testing data			
10	124	125.32	1.06
20	128	128.29	0.22
30	133	133.63	0.47
84	154	151.29	0.48

6.2 REGRESSION MODEL FOR DDS COMPILER

Curve-fitting and regression-based model for DDS compiler IP has been created by modifying and synthesizing the IP for diverse output width. Model is created based on the resource utilization data. The dynamic power equations obtained are given in (10) to (15). The comparison result of training and testing data sets is given in Table 3.

$$\text{Inputpower} = 0.1 \tag{10}$$

$$\text{Outputpower} = 1.183 \text{ x out\_pin} - 3.769 \tag{11}$$

$$\text{Logicpower} = 0.1 \tag{12}$$

$$\text{BRAMpower} = 2.657 \text{ x BRAM} - 0.1762 \tag{13}$$

$$\text{Signalpower} = -2.388 + 0.1161 \text{ x ff} - 0.1528 \text{ x lut} - 0.00069 \text{ x ff x ff} + 0.001175 \text{ x ff x lut} \tag{14}$$

$$\text{Clockpower} = 1.439 - 0.0248 \text{ x ff} + 0.0109 \text{x lut} + 0.0003328 \text{ x ff x ff} - 0.0003805 \text{ x ff x lut} \tag{15}$$

Table 3 Comparison result of DDS compiler for training and testing data sets

DDS compiler IP configurations	Power values from commercial tool (mW)	Power values from regression-based model (mW)	% Error
Training data			
3	123	126.71	3.02
8	129	129.09	0.07
12	137	138.43	1.05
16	161	158.11	1.80
22	177	175.95	0.59
24	182	178.90	1.70
26	189	191.34	1.24
Testing data			
5	125	126.77	1.42
14	143	141.84	0.81
18	169	170.00	0.59
20	173	172.87	0.07

6.3 REGRESSION MODEL FOR MUX

Curve-fitting and regression-based model for MUX IP has been created by modifying and synthesizing the IP for diverse I/O configurations. Model is created based on the resource utilization data. The dynamic power equations obtained are given in (16) to (20). The comparison result of training and testing data sets is given in Table 4.

$$\text{Inputpower} = 0.7938 \text{ x } \exp(-0.986 \text{ x in\_pin}) + 0.1 \quad (16)$$

$$\text{Outputpower} = 0.4274 \text{ x out\_pin} - 0.129 \quad (17)$$

$$\text{Clockpower} = 1.429 - 1.178\text{e}15 \text{ x ff} + 1.178\text{e}15 \text{ x lut} \quad (18)$$

$$\text{Logicpower} = 0.1 + 0.1566 \text{ x ff} - 0.1566 \text{ x lut} \quad (19)$$

$$\text{Signalpower} = 1.714 + 5.241\text{e}14 \text{ x ff} - 5.241\text{e}14 \text{ x lut} \quad (20)$$

Table 4 Comparison result of MUX block for training and testing data sets

MUX IP configurations	Power values from commercial tool (mW)	Power values from regression-based model (mW)	% Error
Training data			
8	124	126.99	2.41

16	128	128.91	0.71
24	132	132.33	0.25
32	137	135.75	0.91
36	139	135.46	2.55
44	143	138.88	2.88
48	145	140.59	3.04
Testing data			
4	123	124.53	1.24
12	126	129.20	2.54
28	135	134.04	0.71
40	141	137.17	2.72

6.4 REGRESSION MODEL FOR MULTIPLIER

Embedded multiplier IP has been customized for performance using mult based construction approach. The model is framed based on curve fitting and regression techniques to obtain the dynamic power equations as given in (21) to (25). Estimated power values of multiplier IP for diverse configurations can be referred from [15].

$$\text{Inputpower} = 0.1 \tag{21}$$

$$\text{Outputpower} = 1.171 \text{ x out\_pin} - 2.18 \tag{22}$$

$$\text{DSPpower} = 3.372 - 5.57 \text{ x } \cos(\text{DSP48 x } 0.3927) + 2.671 \text{ x } \sin(\text{DSP48 x } 0.3927) + 2.04 \text{ x } \cos(2 \text{ x DSP48 x } 0.3927) + 0.965 \text{ x } \sin(2 \text{ x DSP48 x } 0.3927) \tag{23}$$

$$\text{Clockpower} = 0.6464 - 0.5 \text{ x } \cos(\text{ff x} 0.0462) + 1.207 \text{ x } \sin(\text{ff x } 0.0462) + 0.85 \text{ x } \cos(2 \text{ x ff x } 0.0462) - 0.146\text{x } \sin((2 \text{ x ff x } 0.0462) \tag{24}$$

$$\text{Signalpower} = 2.446 \text{ x } e^{(0.0103 \text{ x ff})} - 1.646 \text{ x } e^{(-1.191 \text{ x ff})} \tag{25}$$

6.5 REGRESSION MODEL FOR ADDER

Curve-fitting and regression-based model for adder IP has been created by modifying and synthesizing the IP for diverse I/O configurations. Model is created based on the resource utilization data. The dynamic power equations obtained are given in (26) to (30). Estimated power values of adder IP for various configurations can be referred from [15].

$$\text{Outputpower} = 0.8744 \text{ x } (\text{out\_pin}) - 0.2083 \tag{26}$$

$$\text{Clockpower} = 1 - 0.0147 \text{ x lut} + 0.0147 \text{ x ff} \quad (27)$$

$$\text{Signalpower} = 1.167 + 2.039\text{e}14 \text{ x ff} - 2.039\text{e}14 \text{ x lut} \quad (28)$$

$$\text{Inputpower} = 0.1 \quad (29)$$

$$\text{Logicpower} = 0.1 \quad (30)$$

7. PROPOSED POWER ESTIMATION IDENTITY FOR COMPLETE SYSTEM BASED ON IP MODELING

In a system consisting of different interconnected blocks, the major power exhausting activity occurs at the output stage. This indicates that the impact of output power of intermediate stages and the input stage on the total power would be negligible in comparison with the output power of output stage. So, it would be logical to take the output power of output stage in to consideration. With this approach, assuming that a system consists of Input stage IP, intermediate stage IP and output stage IP as shown in fig. 4, the identity for estimating the power of a system that consists of N number of IP can be given by (31).

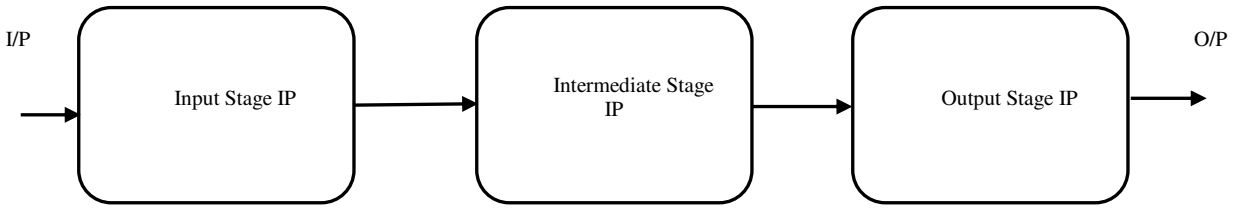

Fig. 4 Block diagram representation of a system.

$$\text{Power}_{\text{System}} = \sum \text{Power}_{(\text{Dynamic of each IP})} - \sum \text{Power}_{(\text{Interconnection Power})} + \text{Power}_{(\text{FPGA Configuration Plan})} \quad (31)$$

Where, interconnection power is the output power of intermediate IPs and input IP in a system.

7.1 POWER ESTIMATION OF QPSK MODULATION SYSTEM

Expanding the proposed identity with reference to the QPSK modulation system, the power equation can be written as (32).

$$\text{Power}_{(\text{QPSK system})} = \sum \text{Power}_{\text{dynamic}_{\text{multipliers}}} + \sum \text{Power}_{\text{dynamic}_{\text{adders}}} + \sum \text{Power}_{\text{dynamic}_{\text{DDS}}} +$$

$$\sum \text{Power}_{\text{dynamic}_{\text{shift register}}} - \sum \text{Power}_{\text{output}_{\text{muliplier}}} - \sum \text{Power}_{\text{output}_{\text{DDS}}} - \sum \text{Power}_{\text{output}_{\text{shift register}}} + \text{Power}_{(\text{FPGA Configuration Plan})} \quad (32)$$

The dynamic power and output power of single IP estimated through regression model used in QPSK system design is given in Table 5.

Table 5 Dynamic power and output power of QPSK system blocks

QPSK system modules	Dynamic power (mW)	Output power (mW)
Multiplier	17.79	16.55
Shift register	3.90	2.31
DDS Compiler	9.09	5.69
Adder	15.78	--

In QPSK modulation system, the output stage IP is one adder IP, Input stage IP are two DDS complier and two shift registers IP and intermediate stage IP is two Multiplier IP. Thus, the power of the QPSK system as per proposed identity is given by (33).

$$\text{Power}_{(\text{QPSK System})} = 17.79\text{x}2 + 1\text{x}15.78 + 9.09\text{x}2 + 3.90\text{x}2 - (2 \text{ x } 5.69 + 2\text{x } 2.31 + 2 \text{ x } 16.55) + 120 = \mathbf{148.24\ mW} \quad (33)$$

The total power of QPSK system estimated using Vivado tool is 147mW, while, the power estimated using proposed identity is 148.24 mW. The percentage error calculated using (9) is 0.84%, which indicates that the proposed identity is producing result that is aligned with the commercial tool.

7.2 POWER ESTIMATION OF BPSK MODULATION SYSTEM

Expanding the proposed identity with reference to the BPSK modulation system, the power equation can be written as (34).

$$\text{Power}_{(\text{BPSK system})} = \sum \text{Power}_{\text{dynamic}_{\text{MUX}}} + \sum \text{Power}_{\text{dynamic}_{\text{DDS}}} + \sum \text{Power}_{\text{dynamic}_{\text{shift register}}} - \sum \text{Power}_{\text{output}_{\text{DDS}}} - \sum \text{Power}_{\text{output}_{\text{shift register}}} + \text{Power}_{(\text{FPGA Configuration Plan})} \quad (34)$$

The dynamic power and output power of single IP estimated through regression model used in BPSK system design is given in Table 6.

Table 6 Dynamic power and output power of BPSK system blocks

BPSK system modules	Dynamic power (mW)	Output power (mW)
Shift Register	3.90	2.31
DDS Compiler	9.09	5.69
MUX	6.99	--

BPSK system consists of one MUX IP as an output IP and one shift register and two DDS compiler IP as an input IP. Thus, power of BPSK system as per proposed identity can be given by (35).

$$Power_{(BPSK\ system)} = 1\text{x}3.90 + 2\text{x}9.09 + 6.99 - (2\ \text{x}5.69 + 2.31) + 120$$

$$= \mathbf{135.38mW} \tag{35}$$

The total power of BPSK system estimated using Vivado tool is 131mW, while, the power estimated using proposed identity is 135.38mW. The percentage error calculated using (9) is 3.34%, which indicates that the proposed identity is producing result that is aligned with the commercial tool.

8. COMPARISON WITH STATE OF ART

The proposed identity has been compared with the existing identity proposed by Elleouet et al. as it is more relevant in context with identity proposed in this paper. Lorandel et al. have also proposed an identity for power estimation of wireless communication system. Though their algorithm is motivated by David Elleouet et al. but it is specific for wireless communication system. In their work, the total power is the summation of data transmission power and power consumed by the circuits that are in Single-Input Single-Output (SISO) configurations. They have also not considered the interconnection power. In this work, the comparison is performed for QPSK and BPSK modulation systems as given in Table7. It is evident from the percentage error analysis that the proposed identity is more accurate in comparison with the existing identity [2]. It is also evident from the result obtained that the power values obtained are aligned with reference to the commercial

tool. Further, errors can be reduced by re-creating a more accurate model of individual IP or by using other machine learning approaches.

Table 7 Comparison with existing work

System taken	Power estimated using commercial tool (mW)	Power estimated using David Elleouet et al. identity (mW)	%Error	Power estimated using proposed identity (mW)	%Error
QPSK	147	197.34	34.24	148.24	0.84
BPSK	131	149.07	13.79	135.38	3.34

9. CONCLUSION

In this work, QPSK and BPSK modulation systems have been considered for power estimation using proposed identity. The power values estimated using proposed identity is validated for accuracy against power values obtained using the commercial tool. It has been analyzed from the power values obtained that the proposed identity outperforms in comparison with existing identity. The percentage error obtained using proposed identity for QPSK and BPSK modulation system is 0.84% and 3.34%, respectively. Whereas, the percentage error obtained using existing identity for QPSK and BPSK modulation systems is 34.24% and 13.79%, respectively indicating much deviation from the power values obtained using the commercial tool. Thus, it can be concluded that the proposed identity is producing accurate results based on the resource utilization data. This will not only help designers to design power efficient systems but will also improve the design turnaround time. In future, the proposed identity can be applied for power estimation of other systems designed using IP modeling approach.

DECLARATIONS

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Availability of data and material: The authors declare that no data or material is taken illegally. However, authors have referred data from their own work.

Code availability: All the analysis has been carried out using standard Xilinx Tool.

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Figures

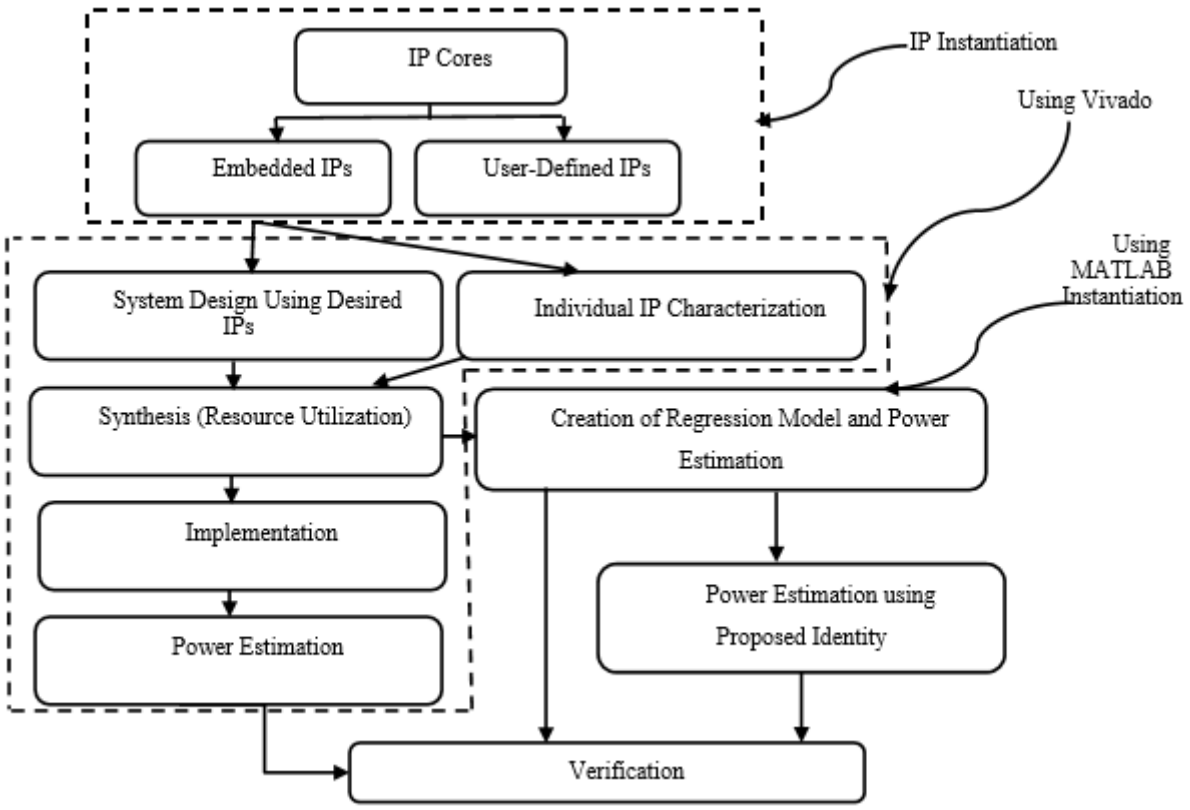

Figure 1

Power estimation flow.

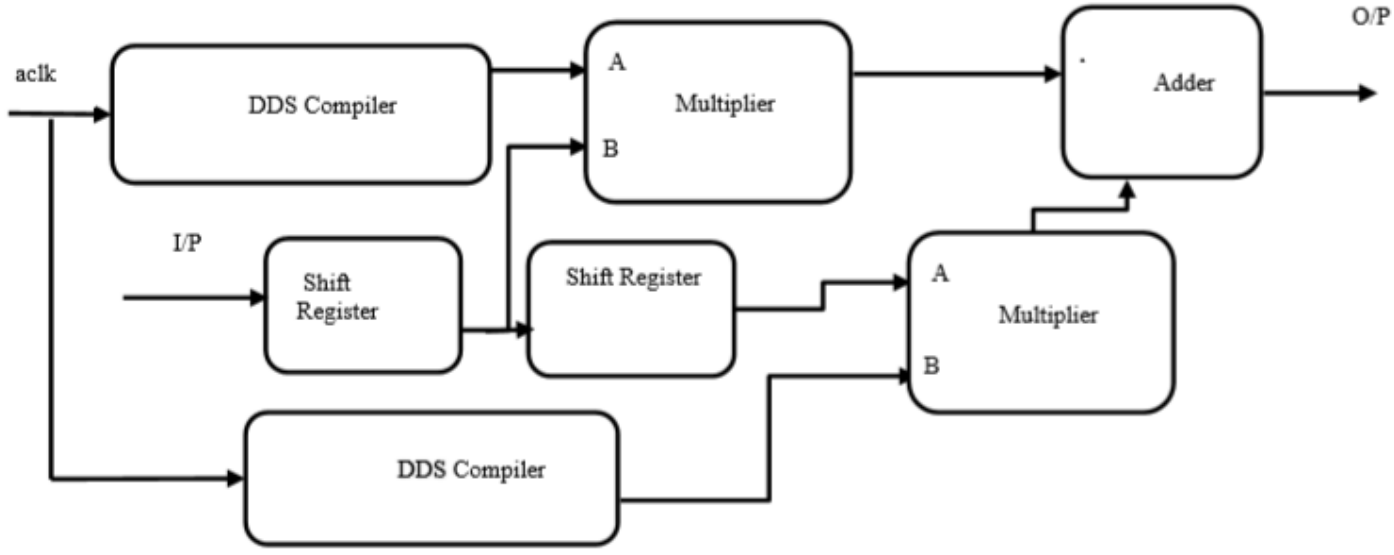

Figure 2

Block diagram of QPSK.

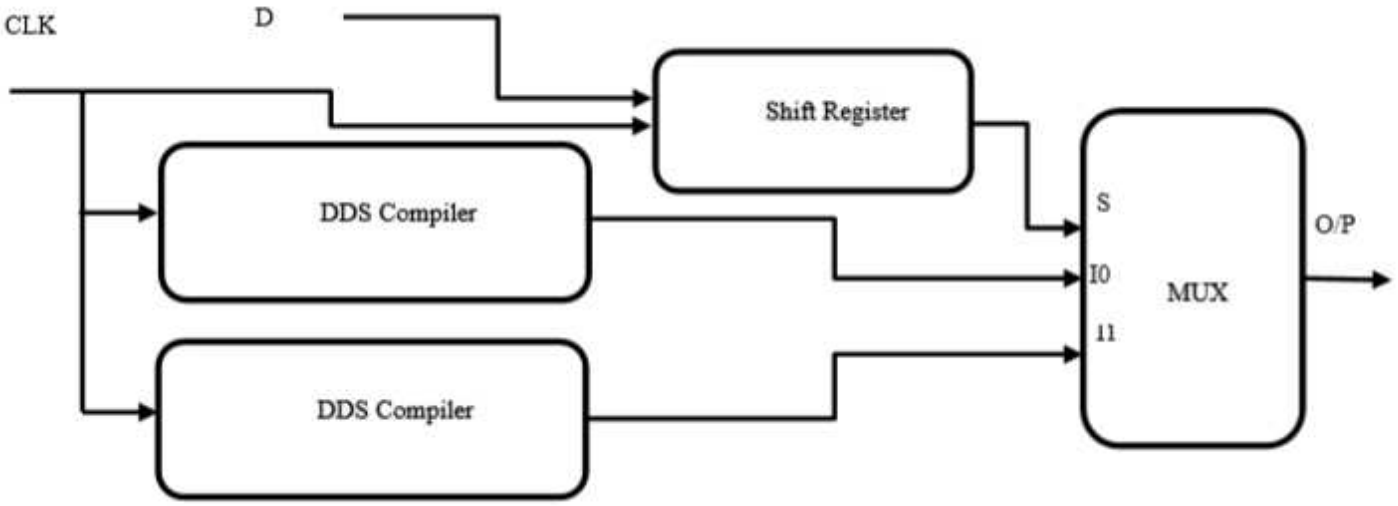

Figure 3

Block diagram of BPSK.

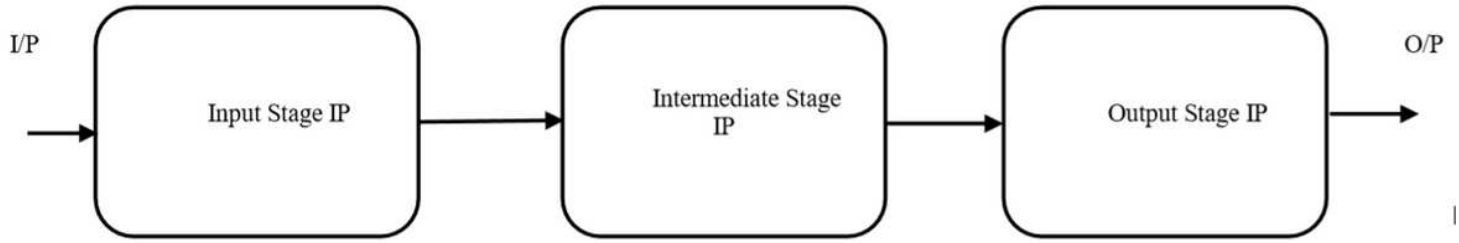

Figure 4

Block diagram representation of a system.