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Analysis of Eddy Effect for Cu and CNT Bundle based Through-Silicon Vias: Impact on Crosstalk and Power

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Abstract
The performance of a three dimensional integrated circuit primarily depends on the filler material used in through silicon via (TSV). The mostly used filler material Cu is primarily facing severe reliability issues due to the skin effect and electromugration related problems at high frequencies. Therefore, in recent, single- and multi-walled carbon nanotubes (SWCNT and MWCNT) have been emerged as suitable filler materials in TSV. Additionally, at high frequencies, an electrmagetic force primarly induces to an eddy current that adversely affects the overall performance of a TSV. This paper for the first time demonstrates the impact of eddy current on Cu, bundled SWCNT and MWCNT based TSVs. An accurate *RLGC* circuit model is proposed by considering the eddy effect at the depletion layer and the silicon substrate region. The equivalent circuit parameters are modelled at 7 nm technology using a three line driver-via-load setup. Using the proposed setup, crosstalk and power disspation are analyzed with and without considering the eddy effect. Irrespective of TSV heights, the MWCNT bundle demonstrates substantially lower crosstalk delay, peak noise and power dissipation in comparison to the Cu and SWCNT bundle based TSVs.

Keywords Crosstalk-induced delay · Peak noise · Power dissipation · Eddy effect · Skin effect · Single-Walled CNT (SWCNT) · Multi-Walled CNT (MWCNT) · Circuit level approach

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1 Introduction

In the recent past, several researchers have contributed in designing Three Dimensional (3D) integrated circuits (ICs) as an alternative solution to conventional 2D planar ICs, wherein IC layers are stacked vertically to integrate more devices on a single chip ensuring improved performance [1-3]. This process, referred to as 3D stacking, primarily results in higher transistor density, lower power dissipation, enhanced speed, and reduced footprint area. For interconnection purposes in 3D IC, Through Silicon Via (TSV) is mainly used that provides higher density and bandwidth, low latency, and provides homogeneous and heterogeneous integration [4]. The performance of 3D IC is primarily dependent on the type of filler material used in TSV [5]. Mostly, copper (Cu) is used as filler material in the TSV due to its higher conductive nature and is comparatively compatible in via last TSV fabrication process. In addition to this, Cu provides good thermal cycling performance, lesser stress, void-free filling, conductivity, and higher current density than tungsten and polymer [6]. However, challenges due to fabrication limitations in accomplishing Physical Vapour Deposition (PVD) and Seed Layer Deposition are observed in Cu-based TSVs. Therefore, researchers are compelled to find an alternative solution to replace the Cu TSVs. Carbon Nanotubes (CNTs) have emerged as the most promising filler material as an alternative choice to Cu. The CNTs are hollow cylindrical-shaped

structures made up of concentrically rolled-up graphene sheets at a specific angle [7]. Two types of CNTs auch as single- (SWCNT) and multi-walled CNT (MWCNT) are generally preferred as filler materials. Negligible electromigration, thermal stability, unique electrical and mechanical properties provide CNT an edge over other materials to be considered suitable as TSV filler [8]. Thus compared to Cu TSV, impressive results can be observed in CNT-based TSV.

At high frequencies, eddy resistance primarily plays a key role for modelling of a TSV using Cu and CNT as filler materials. As per Faraday's law of induction, the magnitude of induced electromotive force (EMF) is directly proportional to the rate of change of magnetic flux [9]. Thus induced EMF can work on the other conducting material of the TSV, and an eddy current will generate in it. According to the Lenz's law, the eddy current opposes the change of magnetic field that is the main reason behind its circulatory nature [10]. Thus eddy resistance comes into the existence in the silicon substrate, neighboring TSVs, and depletion regions due to the flow of eddy current. In general, most of the state-of-the art experimental evidences [11-20] describes an equivalent *RLGC* model of the cylindrical-shaped TSV without considering the eddy effect at high frequencies. Previously, Khalil *et al.* [11] demonstrated an analytical model of Cu-based TSV that depends on its physical parameters. The researchers studied the propagation delay of the TSV by using a transmission line model and electromagnetic field solver using both structural and analytical simulation by neglecting the impact of high-frequency eddy current. Afterward, Xu *et al.* [12] presented a comparative study of propagation delay of TSV with different filler materials like Cu, SWCNT, and MWCNT bundle. In the proposed circuit model, the authors have considered eddy resistance in the silicon substrate. However, the impact of the eddy effect in the depletion layer and neighboring TSVs were ignored. Later, Kim *et al.* [13] presented a compact ac model of the TSV including the via bump, redistribution layers, and skin effect. On the other hand, their frequency-based measurement techniques alongwith several other physical parameters such as inter-metal dielectric (IMD) layer, bump, and underfilled layer were considered for the analysis. The analysis was based on an eye diagram that demonstrates signal amplitude for different frequencies using the method described in [14]. However, the impact of the eddy effect is ignored in the TSV modeling in the case of high frequencies. Researchers in [15] proposed a comprehensive model of SWCNT bundle-based TSV to represent a driver-via-load (DVL) setup that presents significant improvement in delay and power performance with an increase in aspect ratio, although it was ignored in high-frequency analysis. Subsequently, Qian *et al.* [16] proposed a lumped crosstalk noise model to capture TSV to TSV coupling noise in CNT-based 3D IC but neglected the impact of eddy resistance at the higher frequency. Later, Su *et al.* [17] proposed an equivalent model of MWCNT based TSV using temperature effects that considered the eddy resistance due to the flow of eddy current in the substrate but neglected the eddy resistance impact due to depletion region and TSV material. Lu *et al.* [18] demonstrated a *pi* equivalent electrical model of the Cu-based cylindrical TSV with consideration of eddy current and proximity effect at high frequencies. However, the authors restricted their research related to the impact of the eddy effect only for the *S* parameter that shows the power loss of the TSV. Later, Liao *et al.* [19] demonstrated the crosstalk-induced delay considering the proximity effect in a shielded pair of the TSV. The proposed model provides a good agreement with the analytical calculations and 3D full-wave simulation. Although a comprehensive analysis has been performed for transmission coefficient and high-frequency impedance considering TSV design parameters but the impact of the eddy effect is restricted only to the silicon substrate. In recent, the researchers in [20] have demonstrated the crosstalk induced delay and power dissipation for cylindrical, tapered, square, and annular shaped TSVs considering the skin effect at high frequency. The authors proposed an electrical equivalent model of metal-insulator-semiconductor (MIS) and metal-semiconductor (MES) based on different TSV shapes to analyze the power delay product (PDP). The analysis is majorly focused on the TSV shapes and at high frequencies. However, the impact of several design parameters such as mutual inductance, eddy resistance, and depletion capacitance were ignored. Therefore, the state-of-the-art research [11-20] fails on some fronts to present a comprehensive analysis of eddy current for a pair of TSV at high frequencies, and hence a detailed investigation is required to apostrophize the eddy resistance of TSVs by considering all the physical parameters.

This research work for the first time demonstrates the electrical modeling of the TSV considering the eddy effect at high frequencies. Whenever high-frequency alternating current passes through the TSV, it causes the varying electromagnetic field that generates an induced EMF in the other conducting layers such as depletion region, silicon substrate, and the neighboring TSVs. Due to the induced EMF, a circulatory current known as eddy current primarily flows in it. Thus, an eddy resistance comes to an existance due to the flow of eddy current at high frequencies. Hence, all these phenomena are normally known as the eddy effect. In order to demonstrate this effect, a closed-form expression of the eddy resistance is derived for the depletion region, silicon substrate, and neighboring TSVs. In addition, Metal Oxide Semiconductor (MOS) effect is also considered during the *RLGC* modeling of

the TSV. Furthermore, the liner and the depletion layers are used to provide isolation to the TSV from the silicon substrate. Similarly, Inter Metal Dielectric (IMD) and underfilled layers are used to isolate the bump from the silicon substrate and to prevent coupling between the bumps, respectively. This paper analyzes the crosstalk and power performance using a three line parallel DVL, wherein the via line is modelled with Cu, SWCNT, and MWCNT bundles as filler materials. The model primarily considers the impact of eddy effect at 7 nm technology [21]. The main reason behind choosing a 7 nm technology node is that it provides higher device density, improved power-saving, and better performance. A unique 20 distributed *pi* type network is used for the electrical circuit model. Due to the performance accuracy, the *pi* type distributed network is considered instead of *L*- and *T*-type networks [22-23].

The paper is organized in the following sections: Section 1 sheds light on the recent state-of-art research scenario and briefs the modeling of cylindrical-shaped TSV taking into account the impact of eddy resistance. Section 2 introduces the electrical equivalent model of Cu, SWCNT, and MWCNT (number of shells n = 10) bundle-based TSV with and without consideration of eddy resistance. A detailed analytical expression is derived to model the eddy resistance in the silicon substrate, depletion region, and neighboring TSVs. Based on the proposed model, Section 3 demonstrates a comprehensive study of the impact of eddy resistance in the crosstalk noise, delay, and power dissipation concerning different heights and frequencies. Finally, Section 4 briefly concludes this work with a summary.

2 TSV Model and Eddy Resistance

This section demonstrates a cylindrical-shaped TSV structure and their physical parameters using different filler materials such as Cu, SWCNT and MWCNT bundle. Furthermore, a closed-form expression of eddy resistance is derived for the depletion region, silicon substrate, and in the neighboring TSVs. Consequently, a novel equivalent electrical modeling of cylindrical TSV is proposed with consideration of the eddy resistance.

2.1 TSV Structure and Physical Parameters

This subsection gives a detailed insight of the TSV structure and quantitative values of several parameters that will eventually be used in the modeling of equivalent *RLGC* model. Figures 1(a) and 1(b) shows the physical configuration and top cross-sectional view of cylindrical TSV, respectively. The TSV is surrounded by an insulating layer such as liner (usually SiO_2) and depletion layers to provide the DC isolation and prevent leakage between TSV and the substrate. Usually, copper is used as a filler material in TSV and the bump. A cylindrical-shaped pillar bump is used to provide a contact to the TSVs with a different functional block of the dies. In general, an IMD and underfilled layer is used to isolate the bump from the substrate and reduce the cross-coupling between the bumps, respectively. Lossy silicon material is considered as a substrate, whereas the depletion region consists of the lossless silicon to reduce the leakage. Silica-filled anhydride resin polymers are used in the underfilled layer to prevent coupling between the bumps.

The physical parameters of the cylindrical TSV is designed at 7 nm technology [24] as shown in Fig. 1. Under the proposed TSV model, the via pitch *i.e.* center-to-center distance between adjacent TSVs (p_{via}) is considered as 23 nm. TSV pitch (p_{via}) should be equal to or greater than twice the TSV diameter (d_{tsv}) to avoid the misalignment [25]. Based on this concept, the diameter (d_{tsv}) is approximated as 10.5 nm. The height (h_{tsv}) of TSV is taken in the range of 30-120 nms. Considering an aspect ratio of 2.4, the height (h_{bump}) and diameter (d_{bump}) of the bump are approximated as 3.71 nm and 22.26 nm, respectively. The thickness of oxide liner (t_{liner}) and depletion width (t_{dep}) are approximated as 1.05 nm and 1.65 nm, respectively [12]. The height of the IMD layer (h_{IMD}) is 1.05 nm. The number of CNT bundles in a TSV is calculated using the cross-sectional area of TSV and diameter of CNTs in a bundle.

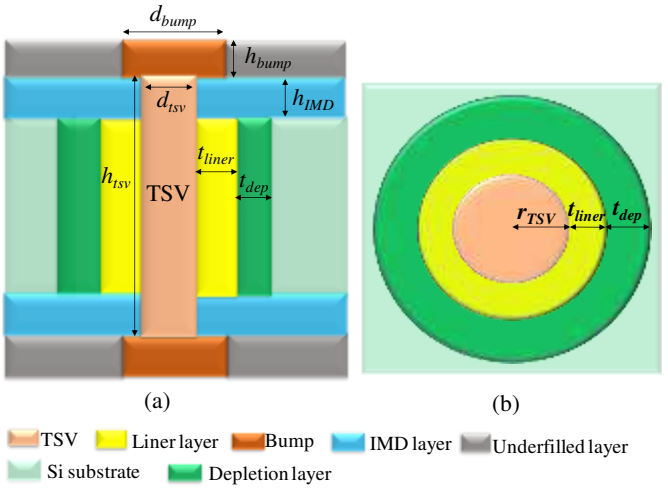

Fig. 1 Structure of a cylindrical-shaped TSV (C-TSV)**: (a)** Side-view and **(b)** Top cross-sectional view of C-TSV.

2.2 Cu based TSV Model

This subsection demonstrates the Cu-based TSV modeling with consideration of the eddy effect in the silicon substrate, depletion region, and neighboring TSVs. Firstly, a closed-form expression of eddy resistance in the silicon substrate is derived by using the physical dimension of the TSV as shown in Fig. 1. The equivalent *RLGC* circuit model of the 3-line TSV at high frequency is presented in Fig. 2. Whenever a high-frequency current passes through the TSVs, it generates a

varying magnetic field. Thus, magnetic vector potential $\vec{A}$ is calculated by using the Maxwell equation [26-27] as

$$\nabla^2\vec{A} = j\omega\mu_{Si}\sigma_{Si,eff}\vec{A} \quad (1)$$

where $\sigma_{Si,eff} = \sigma_{Si}+j\omega\mu\varepsilon_{si}$ is the effective conductivity of the silicon substrate and ω is the angular frequency. Assuming the magnetic vector potential has only z directional component and it varies in radial direction r of the TSV, the variation in the ϕ and z will be zero in the cylindrical coordinate system. Therefore, $\partial A_z/\partial z = 0$, $\partial A_z/\partial \phi = 0$. In this way, the simplified Eqn. (1) can be expressed as

$$\frac{\partial^2}{\partial r^2}A_z(r)+\frac{1}{r}\frac{\partial}{\partial r}A_z(r)+k_s^2A_z(r)=0 \quad (2)$$

where $k_s = (-j\omega\mu_{Si}\sigma_{Si,eff})^{1/2}$. Using the solution of the Bessel function, Eqn. (2) can be simplified as

$$A_z^{sub}(r) = c_1H_0^{(1)}(k_sr)+c_2H_0^{(2)}(k_sr),\ a_1 \le r \le b_1 \quad (3)$$

where c_1 and c_2 are the arbitrary constant, $a_1=r_{TSV}+t_{liner}+t_{dep}$ and $b_1=[p_{via}-(r_{TSV}+t_{liner}+t_{dep})]$. It is assumed that the total current I is passing through the TSV. Hence, the Ampere's law can be used to obtain the magnetic vector potential in the depletion and insulating layers as

$$A_z^{ins}(r) = -\frac{\mu I}{2\pi}\ln(r)+c_3 \quad (4)$$

where $r_{TSV} \le r \le a_1$ or $b_1 \le r \le (p_{via}-r_{TSV})$

Applying the boundary condition in the TSV as Eqn. (5) to (8) as

$$A_z^{ins}(r)|_{(r=a_1)} = A_z^{sub}(r)|_{(r=a_1)} \quad (5)$$

$$\frac{\partial}{\partial r}A_z^{ins}(r)|_{(r=a_1)} = \frac{\partial}{\partial r}A_z^{sub}(r)|_{(r=a_1)} \quad (6)$$

$$A_z^{ins}(r)|_{(r=b_1)} = A_z^{sub}(r)|_{(r=b_1)} \quad (7)$$

$$\frac{\partial}{\partial r}A_z^{ins}(r)|_{(r=b_1)} = \frac{\partial}{\partial r}A_z^{sub}(r)|_{(r=b_1)} \quad (8)$$

Now, c_1 and c_2 can be obtained after solving the above expressions as

$$c_1 = \frac{\mu_0\mu_{r,Si}I}{2\pi k_s}\times\frac{m^2(a_1,b_1)}{u} \quad (9)$$

$$c_2 = \frac{\mu_0\mu_{r,Si}I}{2\pi k_s}\times\frac{m^1(b_1,a_1)}{u} \quad (10)$$

where $u = \{H_1^1(k_sa_1)\times H_1^2(k_sb_1)\}-\{H_1^1(k_sb_1)\times H_1^2(k_sa_1)\}$ (11)

and $m^p(r_1,r_2) = \frac{1}{r_1}H_1^{(p)}(k_sr_2)-\frac{1}{r_2}H_1^{(p)}(k_sr_1)$ (12)

Electric current density in the substrate is $J_z^{sub}(r)$ that can be derived from Eqn. (3), (9), and (10) as

$$J_z^{sub}(r) = -j\omega\mu_{Si}\sigma_{Si,eff}\times A_z^{sub}(r), a_1 \le r \le b_1 \quad (13)$$

Hence, the eddy resistance in the substrate (r'_{e_sub}) can be obtained by using Eqn. (13) and that can be expressed in per unit height (*p.u.h.*) as

$$r'_{e\_sub} = \frac{1}{\sigma_{Si,eff}I}\left[J_z^{sub}(b_1)-J_z^{sub}(a_1)\right] \quad (14)$$

where $h = h_{tsv}-2\times h_{IMD}$ for the calculation of eddy resistance over the total height. In the same way, eddy resistance in the depletion region (r'_{e_dep}) and neighboring TSVs (r'_{e_sub}) can be obtained using the limits of the radius and material as $(r_{TSV}+t_{liner}) \le r \le (r_{TSV}+t_{liner}+t_{dep})$ and $(r_{TSV}+t_{liner}+t_{dep}) \le r \le [p_{via}+(r_{TSV}+t_{liner}+t_{dep})]$, respectively. The conductivity of depleted silicon region $\sigma_{Si,dep}=1.56\times10^{-3}$ [S/m] and for silicon substrate $\sigma_{Si}=100$ [S/m] is considered for this work.

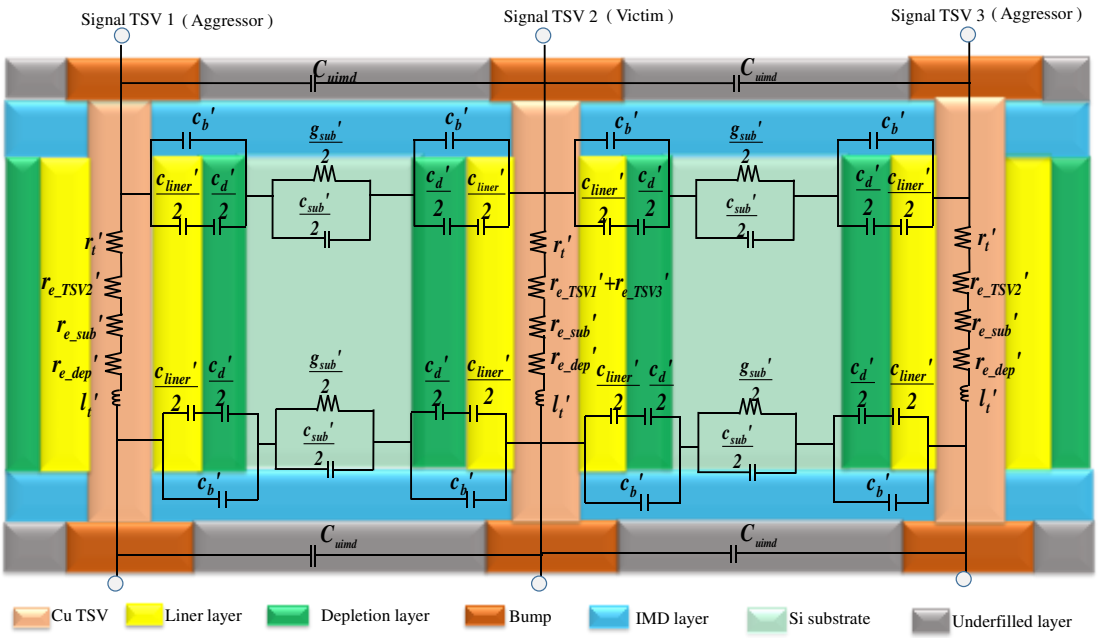

Fig. 2 An equivalent *RLGC* circuit model of the Cu based C-TSV considering eddy effect

As shown in the Fig. 2, rest of the other parasitic parameters of the TSV can be obtained by using the TSV physical dimensions. First of all, the total capacitance (C_{uimd}) is a parallel combination of underfilled (C_{uf}) and IMD capacitances (C_{imd}). The C_{uf} exists between the bump pairs due to the presence of underfilled layer that is made of silica-filled anhydride resin polymer. However, C_{imd} exhibits between the TSV pairs due to the presence of IMD layer [28]. The C_{uf} and C_{imd} can be modeled as parallel-wire capacitance [13].

$$C_{imd} = \frac{\pi \times \varepsilon_{IMD} \times h_{IMD}}{\cosh^{-1}\left(\frac{\mathrm{p_{via}}}{\mathrm{d_{tsv}}}\right)} \tag{15}$$

$$C_{uf} = \frac{\pi \times \varepsilon_{uf} \times h_{bump}}{\cosh^{-1}\left(\frac{p_{via}}{d_{bump}}\right)} \tag{16}$$

$$C_{uimd} = C_{uf} + C_{imd} \tag{17}$$

A silicon substrate capacitance (c'_{sub}) is formed between the TSVs due to the presence of conductive silicon substrate. The c'_{sub} can be derived using the parallel-wire capacitance model [29] in *p.u.h.* as

$$c'_{sub} = \left\{ \frac{2\pi \times \varepsilon_{si} \times h}{\cosh^{-1}\left(\frac{p_{via}^2}{2\left(r_{tsv} + t_{liner} + t_{dep}\right)^2} - 1\right)} \right\} \tag{18}$$

where height is considered as $h = h_{tsv}–2\times h_{IMD}$. In addition to this, substrate conductance g'_{sub} exists between the TSV pairs due to the presence of lossy characteristics of the silicon substrate. The g'_{sub} can be obtained by using a relationship between the c'_{sub} and g'_{sub} as discussed in [13]. Liner capacitance c'_{liner} exists between the TSV and depletion layer due to the presence of the oxide layer [13]. In addition to this, depletion capacitance c'_d formed between the TSVs surrounded by the oxide layer and the Si substrate in the presence of the depletion layer [29]. The c'_{liner} and c'_d in *p.u.h.* can be derived by applying the coaxial-wire capacitance model.

Bump capacitance c'_b exists between the silicon substrate and the bump due to the presence of IMD layer. Bump capacitance can be expressed in *p.u.h.* by using the parallel plate capacitor model [13] as

$$C'_b = \varepsilon_{IMD} \times \pi \frac{\left[\left(\frac{d_{bump}}{2}\right)^2 - \left(\frac{d_{tsv}}{2} + t_{liner} + t_{dep}\right)^2\right]}{h_{imd}} \tag{19}$$

Apart from this, the total resistance of the circuit r'_t in Fig. 2 is a series combination of the TSV resistance r'_{tsv} and the bump resistance r'_b.

$$r'_t = r'_{tsv} + r'_b \tag{20}$$

where r'_{tsv} and r'_b are obtained using the dc and ac components of the resistance in terms of *p.u.h.* Here, ac component of the resistance primarily considers the skin effect of the TSV [13]. On the other hand, the total inductance l'_t is a series combination of bump inductance l'_b and TSV inductance l'_{tsv} [13]. Inductance forms due to the magnetic field that is produced by current passing through TSV.

2.3 CNT based TSV Model

This subsection presents the equivalent electrical model with the parasitic calculation techniques for SWCNT bundle, followed by MWCNT bundle based TSVs. The modeling of via parasitic primarily depends on the number of conducting channels in each SWCNT present in a bundle. The total number of SWCNTs (N_{CNT}) in a bundle is calculated using the radius of each SWCNT (r_{CNT}), the radius of TSV (r_{via}), and the Vander Waals distance ($\delta \approx 0.34$) between the adjacent SWCNTs. The N_{CNT} can be represented as

$$N_{CNT} = \frac{2\pi r_{via}^2}{\sqrt{3}\,(2r_{CNT}+\delta)^2} \tag{21}$$

The number of conducting channels in MWCNT is a function of the shell diameter [30]. All the SWCNTs in a bundle act as either metallic or semiconductor based on their chirality whereas MWCNTs are always metallic. For metallic SWCNT in a bundle, the average number of conducting channels for a particular diameter of SWCNT is as follows

$$N_i(D_i) \approx \begin{cases} k_1 T D_i + k_2, & D_i > d_t/T \\ \frac{2}{3} & D_i \le d_t/T \end{cases} \tag{22}$$

where D_i represents the diameter of the *i*th shell of MWCNT (or SWCNT) and k_1 *and* k_2 possess a value of $2.04 \times 10^{-4}\ nm^{-1}$ and 0.425, respectively. The quantitative value of d_t is determined from the thermal energy of electrons and the gap between the two sub-bands that is equivalent to 1300 nm.k at T=300K. For D_i > 4.3 nm, the average number of conducting channels is proportional to its shell diameter. Therefore, the total number of conducting channels in a bundle can be calculated by taking the summation of conducting channel of each SWCNT as

$$N_{channel} = \sum_{i=1}^{n} N_i \tag{23}$$

The conduction mechanism of CNT is ballistic due to the long mean free path (*mfp)* in the range of micrometers. The diameter following *mfp* can be expressed as:

$$\lambda_{mfp,i} = \frac{1000}{\left(\frac{T}{T_i}\right)-2} \tag{24}$$

Thus, the total number of conducting channels can be expressed as

$$N_{Total} = N_{channel} \times N_{CNT}. \quad (25)$$

The electrical equivalent *RLGC* model of CNT bundle-based TSV considers the eddy resistance as shown in Fig. 3. Each CNT in a bundle comprises of broadly three types of resistances: (1) scattering resistance (r'_{bundle}) that occurs due to higher nanotube length exceeding *mfps* of the electron, (2) quantum resistance (R_q) due to the quantum confinement of electron and depends on the $N_{channel}$ of each SWCNT/ MWCNT in a bundle, and (3) imperfect metal-nanotube contact resistance (R_{mc}) with the approximated value of 3.2 kΩ arising due to the fabrication process [30-33]. Thus, the equivalent scattering and quantum resistances can be expressed as

$$R_{fix} = \frac{R_q}{N_{Total}} + R_{mc}, \text{ where } R_q = \frac{h}{2e^2} \approx 12.9\ \text{k}\Omega \quad (26)$$

$$r'_{bundle} = \frac{(\sum_{i=1}^{n}(R_q/2N_i\,\lambda_{mfp,i})^{-1})^{-1}}{N_{CNT}} \quad (27)$$

where h and e represents the plank's constant and electronic charge, respectively.

The equivalent *RLGC* model of CNT bundle comprises of two types of capacitances: (1) quantum capacitance (c'_{q_bundle}) that arises due to finite electronic states in a quantum wire and (2) electrostatic capacitance (c'_{E_bundle}) that is due to the potential difference between the CNT bundle and the ground plane. The c'_{q_bundle} and c'_{E_bundle} in *p.u.h.* can be expressed as

$$c'_{q\_bundle} = c'_q \times 2\,N_{Total} \quad \text{where} \quad c'_q = \frac{2e^2}{hv_f}, \quad (28)$$

$$c'_{E\_bundle} = \frac{2\pi\varepsilon_o\varepsilon_r}{cosh^{-1}[\frac{d_{CNT}^{out}+h_{tsv}}{d_{CNT}^{out}}]} \quad (29)$$

where d_{CNT}^{out} and v_f represents the outer shell diameter of SWCNT/MWCNT and the Fermi velocity ($\approx 8 \times 10^5 m/s$), respectively. Similrly, the equivalent bundle inductance (l'_{Bundle}) of TSV is a combination of two types of inductances: (1) kinetic inductance (l'_k) is associated with the kinetic energy of the electrons in each conducting channel of CNT and (2) magnetic inductance (l'_m) is due to the induced magnetic field by the current flowing through the nanotube [33]. Thus, l'_{Bundle} can be primarily expressed as

$$l'_{Bundle} = \frac{l'_k}{2\,N_{Total}} + l'_m \quad (30)$$

$$\text{where } l'_k = \frac{h}{2e^2 v_f}, \text{ and } l'_m = \frac{\mu}{2\pi}\ln\left(\frac{y}{d_{CNT}^{out}}\right). \quad (31)$$

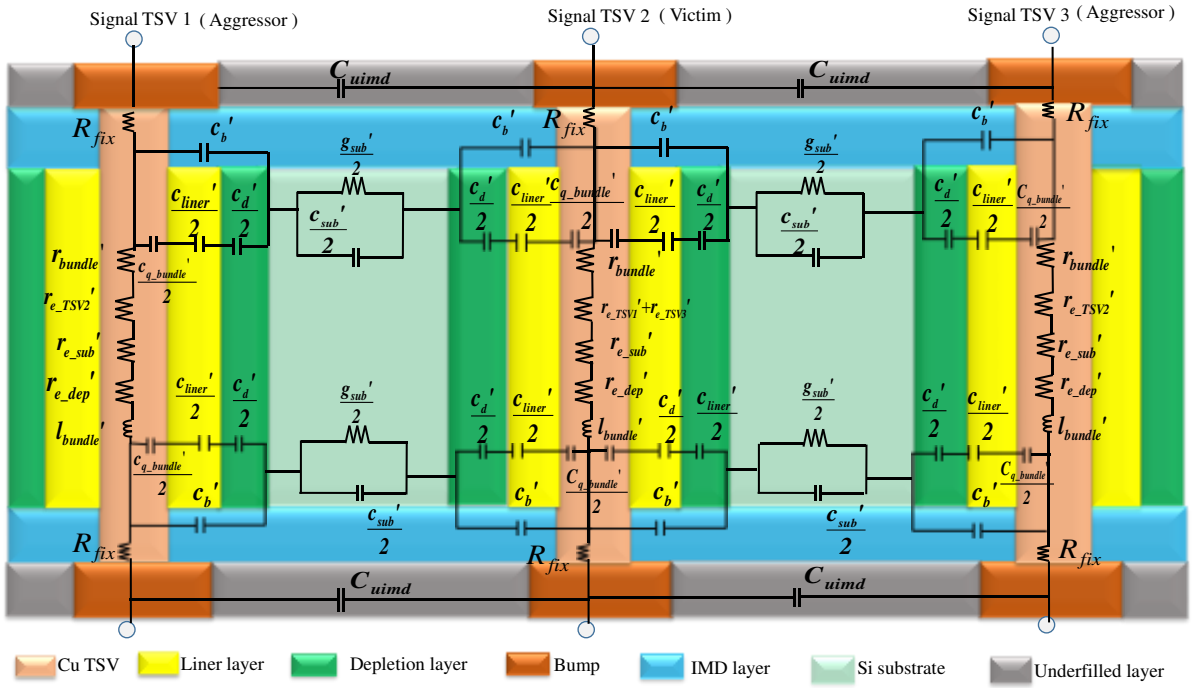

Fig. 3 An equivalent *RLGC* circuit model of the CNT based C-TSV considering eddy effect

TABLE 1:Parasitic values of Cu, SWCNT, and MWCNT bundle based C-TSV for different TSV heights and frequencies.

TSV Height (in μm)	Parasitic Parameter	Parasitic values of Cylindrical shape TSV for different frequencies (in GHz) at								
		Cu based TSV			SWCNTbundle based TSV			MWCNT bundle based TSV		
		f = 20	f =200	f =500	f = 20	f =200	f =500	f = 20	f =200	f =500
30	R_{eq}(Ω)	6.0545	6.0546	6.0554	4.1835	4.1835	4.1835	1.8138	1.8138	1.8138
	R_{e_tsv}(μΩ)	0.1341	0.1351	0.1364	0.1110	0.1122	0.1185	0.1110	0.1122	0.1185
	R_{e_dep}(kΩ)	4.1485	4.1485	4.1485	4.1485	4.1485	4.1485	4.1485	4.1485	4.1485
	L_{eq} (fH)	4.7010	4.7010	4.7010	2600	2600	2600	9570	9570	9570
	C_{eq}(aF)	18.3451	18.3451	18.3451	17.8475	17.8475	17.8475	17.4488	17.8475	17.4488
	C_{uimd}(aF)	2.8915	2.8915	2.8915	2.8915	2.8915	2.8915	2.8915	2.8915	2.8915
	C_{sub} (aF)	10.1150	10.1150	10.1150	1.0115	1.0115	1.0115	1.0115	1.0115	1.0115
	G_{sub} (μS)	9.6004	9.6004	9.6004	9.6004	9.6004	9.6004	9.6004	9.6004	9.6004
60	R_{eq}(Ω)	11.9543	11.9545	11.9559	8.3725	8.3725	8.3725	3.6331	3.6331	3.6331
	R_{e_tsv}(μΩ)	0.2681	0.2702	0.2728	0.2219	0.22435	0.23696	0.2219	0.2244	0.2370
	R_{e_dep}(kΩ)	8.6093	8.6093	8.6093	8.6093	8.6093	8.6093	8.6093	8.6093	8.6093
	L_{eq} (fH)	9.1326	9.1326	9.1326	5100	5100	5100	19140	19140	19140
	C_{eq}(aF)	31.1581	31.1581	31.1581	30.0742	30.0742	30.0742	29.2358	29.2358	29.2358
	C_{uimd}(aF)	2.8915	2.8915	2.8915	2.8915	2.8915	2.8915	2.8915	2.8915	2.8915
	C_{sub} (aF)	20.9920	20.9920	20.9920	2.0992	2.0992	2.0992	2.0992	2.0992	2.0992
	G_{sub} (μS)	19.9230	19.9230	19.9230	19.923	19.923	19.923	19.923	19.923	19.923
90	R_{eq}(Ω)	17.8542	17.8546	17.8566	12.5616	12.5616	12.5616	5.4525	5.4525	5.4525
	R_{e_tsv}(μΩ)	0.4023	0.4053	0.4092	0.3328	0.3365	0.3555	0.3328	0.3365	0.3555
	R_{e_dep}(kΩ)	13.0700	13.0700	13.0700	13.07	13.07	13.07	13.07	13.07	13.07
	L_{eq} (fH)	13.5640	13.5640	13.5640	7700	7700	7700	28710	28710	28710
	C_{eq}(aF)	43.9697	43.9697	43.9697	42.3106	42.3106	42.3106	41.0191	41.0191	41.0191
	C_{uimd}(aF)	2.8915	2.8915	2.8915	2.8915	2.8915	2.8915	2.8915	2.8915	2.8915
	C_{sub} (aF)	31.8680	31.8680	31.8680	3.1868	3.1868	3.1868	3.1868	3.1868	3.1868
	G_{sub} (μS)	30.2460	30.2460	30.2460	30.246	30.246	30.246	30.246	30.246	30.246
120	R_{eq}(Ω)	23.7541	23.7545	23.7572	16.7506	16.7506	16.7506	7.2718	7.2718	7.2718
	R_{e_tsv}(μΩ)	0.5364	0.5404	0.5455	0.4438	0.4487	0.4739	0.4438	0.4487	0.4739
	R_{e_dep}(kΩ)	17.5310	17.5310	17.5310	17.531	17.531	17.531	17.531	17.531	17.531
	L_{eq} (fH)	17.9960	17.9960	17.9960	10300	10300	10300	38280	38280	38280
	C_{eq}(aF)	56.7836	56.7836	56.7836	54.5698	54.5698	54.5698	52.8041	52.8041	52.8041
	C_{uimd}(aF)	2.8915	2.8915	2.8915	2.8915	2.8915	2.8915	2.8915	2.8915	2.8915
	C_{sub} (aF)	42.7450	42.7450	42.7450	4.2745	4.2745	4.2745	4.2745	4.2745	4.2745
	G_{sub} (μS)	40.5690	40.5690	40.5690	40.569	40.569	40.569	40.569	40.569	40.569

$$R_{eq} = \begin{cases} R_t + R_{eddy\_sub}, & for\ Cu\ based\ TSV \\ R_{bundle} + R_{eddy\_sub}, & for\ CNT\ based\ TSV \end{cases} \quad and \quad C_{eq} = \begin{cases} C_b + \frac{1}{2}\left(\frac{C_{liner} \times C_d}{C_{liner} + C_d}\right), & for\ Cu\ based\ TSV \\ C_b + \frac{1}{2}\left(\frac{C_{q\_bundle} \times C_{liner} \times C_d}{(C_{q\_bundle} \times C_{liner}) + (C_{liner} \times C_d) + (C_{q\_bundle} \times C_d)}\right), & for\ CNT\ based\ TSV \end{cases}$$

$$L_{eq} = \begin{cases} L_t, & for\ Cu\ based\ TSV \\ L_{bundle}, & for\ CNT\ based\ TSV \end{cases}$$

Note: all parasitic values are calculated with consideration of the whole height of the TSV and bump.

The resistances due to eddy current induced by changing electromagnetic field are the same as that of Cu TSV. Equations (1) to (31) are used for the calculation of the parasitic parameters of the copper and CNT bundle-based cylindrical TSVs. Furthermore, the parasitic parameter values with different TSV heights and operating frequencies are summarized in Table 1 for Cu and CNT bundle-based TSVs. It is observed that the quantitative values of the parasitic parameters are lesser for MWCNT bundle compared to the Cu TSV irrespective of via height. As shown in Table 1, the eddy resistance in the neighboring TSV R_{e_tsv} becomes more effective at high frequencies due to the eddy effect and skin effect.

3 Performance Analysis

This section illustrates the impact of eddy current on the

crosstalk induced delay, peak noise and power dissipation using the proposed *RLGC* model of the TSV at 7 nm technology. A 3-line DVL setup (as shown in Fig. 4) is used for circuit-level simulation of the TSV with 20 distributed *pi* networks. Each via line represents the *RLGC* model of the TSV as shown in Fig. 3. The vias are driven by a field effect transistor (FET) instead of CMOS driver at the 7nm technology node. Although a CMOS performs well up to 28 nm technology but below 28 nm technology, CMOS shrinks in such a way that the short channel effect becomes uncontrollable. As a result, the gate is unable to control the leakage path. In the case of FET driver, there is good control of the gate on the leakage path at the lower technology and hence FET is used as a suitable driver. In Fig. 4, each via line is terminated with the load capacitor C_{load} = 200aF. Using the above mentioned setup in Fig. 4, the subsequent sections have analyzed the overall reliability of the TSV in terms of crosstalk induced delay, peak voltage, and power dissipation for different operating frequencies and via heights.

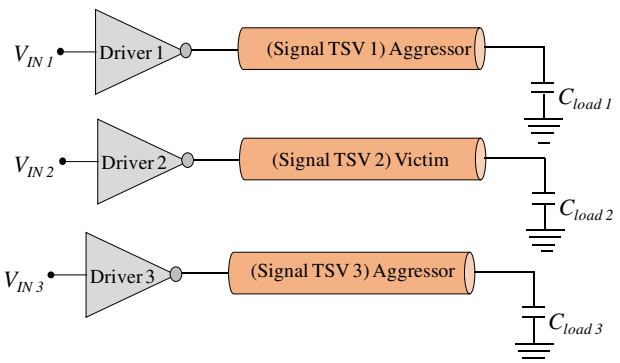

Fig. 4 Driver-Via-Load (DVL) setup for circuit-level simulation

3.1 Crosstalk Delay Analysis

This subsection presents the crosstalk induced delay analysis of cylindrical TSV with consideration of the eddy effect in terms of dynamic crosstalk delay by using the DVL setup as shown in Fig. 4. The transmission line experiences some delay at the same time as the signal passes through it. In this situation, one of the transmission lines can act as an aggressor and the other can act like a victim. Dynamic crosstalk delay phenomena is introduced when all signals provided to the aggressor and victim lines are in the same or the opposite switching state at the same time. However, in the case of out-phase crosstalk delay, all signals are in the opposite switching transition from each other [34]. Furthermore, out-phase crosstalk delay is the worst-case delay due to a higher Miller Capacitive Factor (MCF) between the vias [23]. Hence, this work considers the opposite switching transition state for crosstalk delay calculation such as aggressor line switches from high to low and victim is low to high. Figure 5 shows the crosstalk delay of Cu, SWCNT, and MWCNT bundle based TSVs that are obtained with and without consideration of eddy effect for different via heights and frequencies. From Fig. 5, it is clear that the delay of MWCNT bundle based TSV is considerably lower in comparison to the SWCNT bundle and Cu-based TSVs. The primary reason behind this is that the quantitative values of the coupling capacitance of the MWCNT bundle are lower as compared to other vias. It can also be noticed that the delay with eddy effect is substantially higher than the delay without considering the eddy effect. It is due to the fact that the impact of eddy current is more effective at high frequencies that shows the eddy resistance in neighboring TSV R_{e_tsv} rises with frequencies as observed from Table 1. Additionally, it can be also observed that the crosstalk induced delay increases with the TSV heights and operating frequencies. It is due to the higher values of parasitics that increases for more via height and frequencies as witnessed from Table 1.

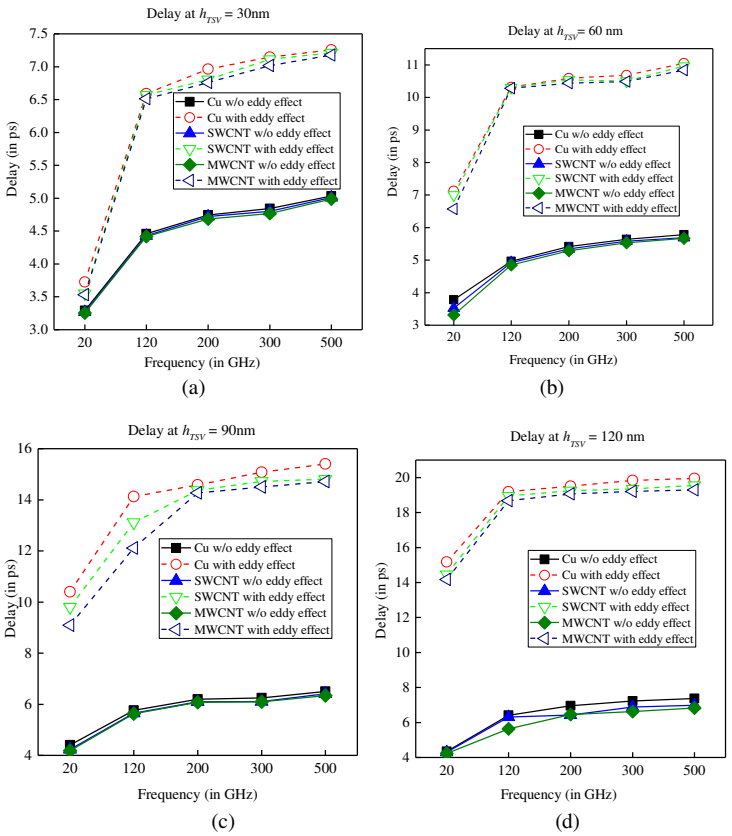

Fig. 5 Crosstalk delay of Cu, SWCNT and MWCNT bundle based TSV at via heights of (a) h_{TSV}=30 µm, (b) h_{TSV}=60 µm, (c) h_{TSV}=90 µm and (d) h_{TSV}=120 µm

Additionally, Fig. 6 presents the rate of change in crosstalk delay for different frequencies *w.r.t.* the delay obtained at 20GHz. This percentage change is obtained for Cu, bundled SWCNT and MWCNT based TSVs with and without

consideration of eddy effect at 120 nm TSV height as shown in Fig. 6 It can be noticed that the percentage change in delay is more for higher frequencies due to a rise in the delay for an increasing frequency. However, the rate of change of crosstalk delay without considering the eddy effect is more server than variation in the delay including the eddy effect. The differences in the percentage of crosstalk delay with and without considering the eddy effect are 21.14%, 31.63%, 35.77%, and 38.35% at 120GHz, 200GHz, 300GHz, and 500GHz frequencies, respectively for Cu based TSV. Similarly, these differences in delay for bundle SWCNT based TSVs are 15.57%, 16.12%, 26.18%, and 27.04% at 120GHz, 200GHz, 300GHz, and 500GHz frequencies, respectively. The differences in delay for bundle MWCNT based TSV are 1.66%, 18.08%, 21.17%, and 25.29% at 120GHz, 200GHz, 300GHz, and 500GHz frequencies, respectively. It can be observed that this difference in the rate of change in delay is improving when moving towards

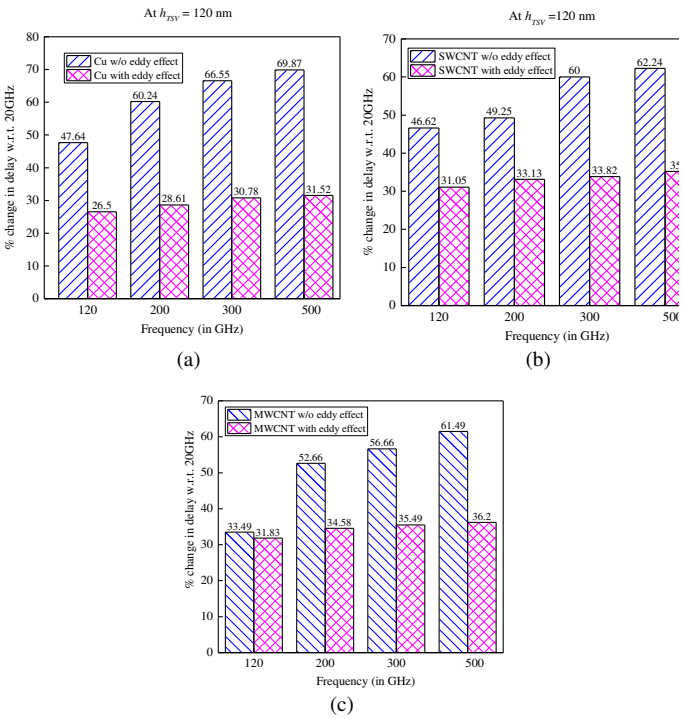

Fig. 6 Percentage change in the crosstalk delay of (a) Cu, (b) SWCNT bundle and (c) MWCNT bundle for different frequencies *w.r.t.* the delay obtained at 20 GHz with and without considering the eddy effect at h_{TSV} = 120 nm.

the MWCNT bundle based TSV. The average percentage change in delay *w.r.t.* eddy effect is 31.73%, 21.23%, and 16.55% for Cu, SWCNT and MWCNT bundle based TSVs, respectively.

3.2 Peak Noise

This sub-section discusses the impact of eddy effect on peak noise of the TSV. Conceptually, noise coupling takes place in the region of substrate whenever a fast signal transition happens within the TSV. This coupling mechanism is similar to the noise coupling taking place into the substrate through source/drain junctions of a transistor. However, due to the greater dielectric area, the dielectric capacitance of a TSV is larger than source/drain junction capacitance. TSV related substrate noise coupling is therefore one of the primary noise injection mechanisms in 3D integrated circuits [35]. Peak noise is observed when the aggressor line is supplied with the in-phase signals and the victim line is grounded. It results in the form of unintentional peaks observed at the victim line which is responsible for faults in digital circuits [36]. Figure 7 demonstrates the peak noise voltage of Cu, SWCNT and MWCNT bundle based TSVs with and without consideration

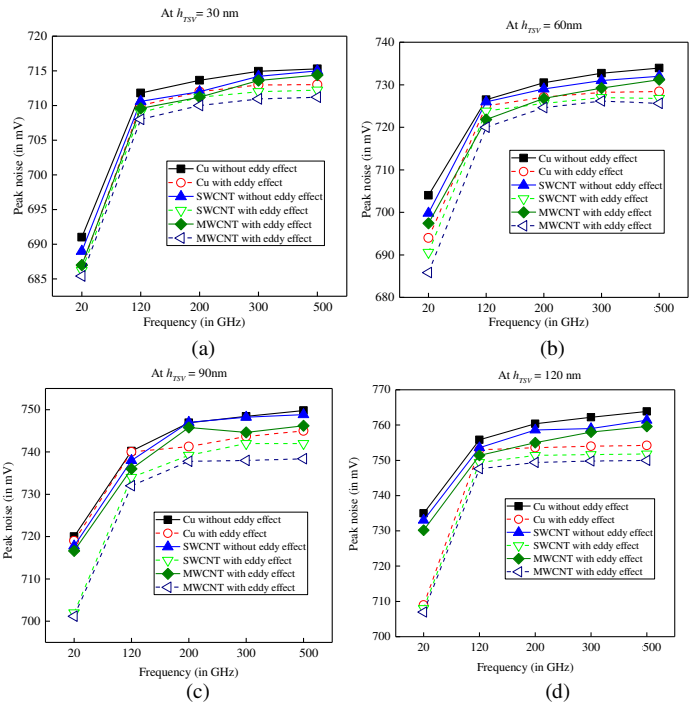

Fig. 7. Peak noise of Cu, SWCNT and MWCNT bundle based TSV at via heights of (a) h_{TSV}=30 µm, (b) h_{TSV}=60 µm, (c) h_{TSV}=90 µm and (d) h_{TSV}=120 µm

of eddy effect for different TSV heights and frequencies. From Fig. 7, it can be observed that the peak noise voltage in MWCNT bundle based TSV is lesser as compared to SWCNT bundle and Cu-based TSVs due to the less coupling factor. It can also be noticed that the peak noise with eddy effect is considerably lower than the peak noise without considering eddy. Additionally, the peak noise is more for higher TSVs and operating frequencies. The reason behind this is the higher parasitic values that increases with the height and frequencies

as witnessed from Table 1.

Additionally, Fig. 8 demonstrates the rate of change in peak noise voltage for different frequencies *w.r.t.* the delay obtained at 20 GHz. This percentage change is calculated for Cu, SWCNT bundle and MWCNT bundle based TSVs with and without consideration of eddy effect at h_{TSV} = 120 nm as shown in Fig. 8. It is observed that the percentage change in noise voltage is considerably higher for more frequencies due to a rise in the noise voltage with an increase in frequencies. However, the rate of change of noise voltage considering the eddy effect is more server than without the eddy. The differences in the percentage of peak noise voltage with and without considering the eddy effect are 3.38%, 2.83%, 2.65%, and 2.45% at 120GHz, 200GHz, 300GHz, and 500GHz frequencies, respectively for Cu based TSV. Similarly,

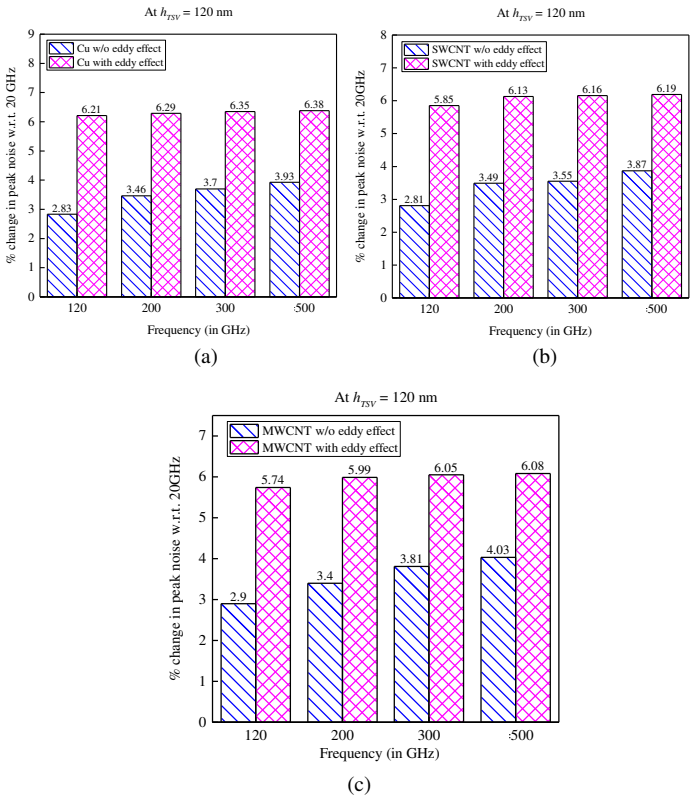

Fig. 8 Percentage change in peak noise of (a) Cu, (b) SWCNT bundle and (c) MWCNT bundle for different frequencies *w.r.t.* the noise obtained at 20 GHz with and without considering the eddy effect at h_{TSV} = 120 nm.

these differences in peak noise voltage for bundled SWCNT-based TSVs are 3.04%, 2.64%, 2.61%, and 2.32% at 120 GHz, 200 GHz, 300 GHz, and 500 GHz frequencies, respectively. The differences in peak noise voltage for bundled MWCNT based TSVs are 2.84%, 2.59%, 2.24%, and 2.05% at 120 GHz, 200 GHz, 300 GHz, and 500 GHz frequencies, respectively. It can be noticed that this difference in the rate of change of noise voltage is improving when moving towards the MWCNT bundle based TSV. The average percentage change in the noise voltage *w.r.t.* eddy effect is 2.83%, 2.65%, and 2.45% for Cu, SWCNT bundle and MWCNT bundle based TSVs, respectively.

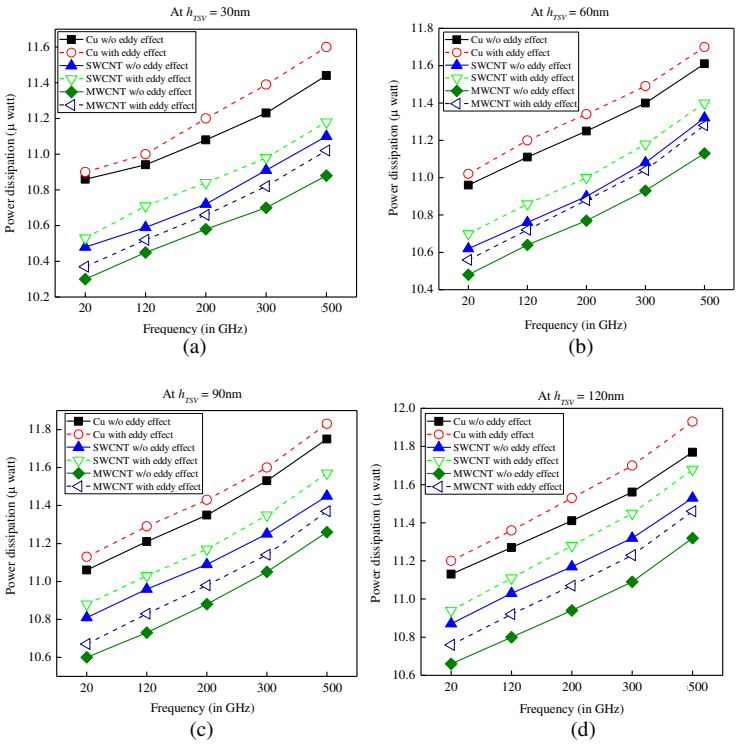

Fig. 9. Power dissipation of Cu, SWCNT and MWCNT bundle based TSV at via heights of (a) h_{TSV}=30 μm, (b) h_{TSV}=60 μm, (c) h_{TSV}=90 μm and (d) h_{TSV}=120 μm

3.3 Power Dissipation Analysis

This sub-section demonstrates the impact of eddy resistance on dynamic power dissipation. The power dissipation is obtained by providing the in-phase signal either from low to high or high to low through the coupled TSVs. Figure 9 shows the power dissipation of Cu, bundled SWCNT and MWCNT based TSVs that are obtained with and without consideration of eddy effect for different TSV heights and frequencies. It has been observed that the bundled MWCNT without eddy resistance dissipates the least power among all filler materials as shown in Fig. 9. Additionally, the power consumption rises for higher TSVs and operating frequencies. The reason behind this is the higher quantitative values of parasitics that increases for higher TSVs and frequencies as witnessed in Table 1.

Furthermore, Fig. 10 presents the rate of change in power dissipation for different frequencies *w.r.t.* the power obtained at 20 GHz at 120 nm TSV height. This percentage change is

calculated for SWCNT and MWCNT bundle based TSVs with and without consideration of the eddy effect that is shown in Fig 10. It can be illustrated that the percentage change in power dissipation is more for an increase in frequencies. However, the rate of change of power dissipation considering the eddy effect is more severe than variation in the power dissipation without the eddy effect. The differences in the percentage of power dissipation with and without considering the eddy effect are 0.17%, 0.43%, 0.6%, and 0.77% at 120 GHz, 200 GHz, 300 GHz, and 500 GHz frequencies, respectively

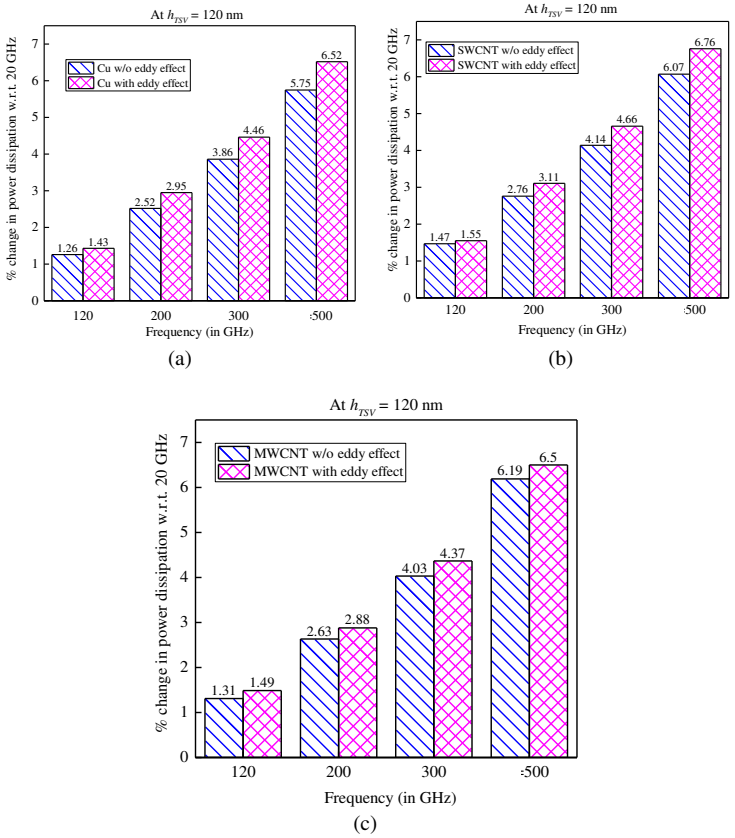

Fig. 10 Percentage change in power dissipation of (a) Cu, (b) SWCNT bundle and (c) MWCNT bundle for different frequencies *w.r.t.* the power obtained at 20 GHz with and without considering the eddy effect at h_{TSV} = 120 nm.

for Cu based TSV. Similarly, these differences in power dissipation for SWCNT bundle based TSVs are 0.08%, 0.35%, 0.52%, and 0.69% at 120 GHz, 200 GHz, 300 GHz, and 500 GHz frequencies, respectively. The differences in power dissipation for MWCNT bundle based TSVs are 0.18%, 0.25%, 0.34%, and 0.31% at 120 GHz, 200 GHz, 300 GHz, and 500 GHz frequencies, respectively. It can be observed that this difference in the rate of change of power dissipation is improving when moving towards the MWCNT bundle based TSV. The average percentage change in power dissipation *w.r.t.* eddy effect is 0.4925%, 0.41%, and 0.27% for Cu, SWCNT, and MWCNT bundle based TSVs, respectively.

4 Conclusion

This paper proposed a novel *pi* type equivalent *RLGC* model of Cu, SWCNT and MWCNT bundle based TSVs considering the eddy effect at high frequencies at 7 nm technology. A closed form expression of eddy resistance is derived for depletion region, substrate and in the neighboring TSV. Further, the performance of the TSV is analyzed in terms of crosstalk delay, peak noise and power dissipation of the TSV with concern of the eddy effect at high frequency. It has been observed that the impact of high frequency eddy current is substantially lower in case of MWCNT bundle based TSV as compared to the Cu and SWCNT bundle. The overall differences are approximately 16.55%, 2.45% and 0.27% in terms of crosstalk delay, noise voltage and power dissipation, respectively.

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Figures

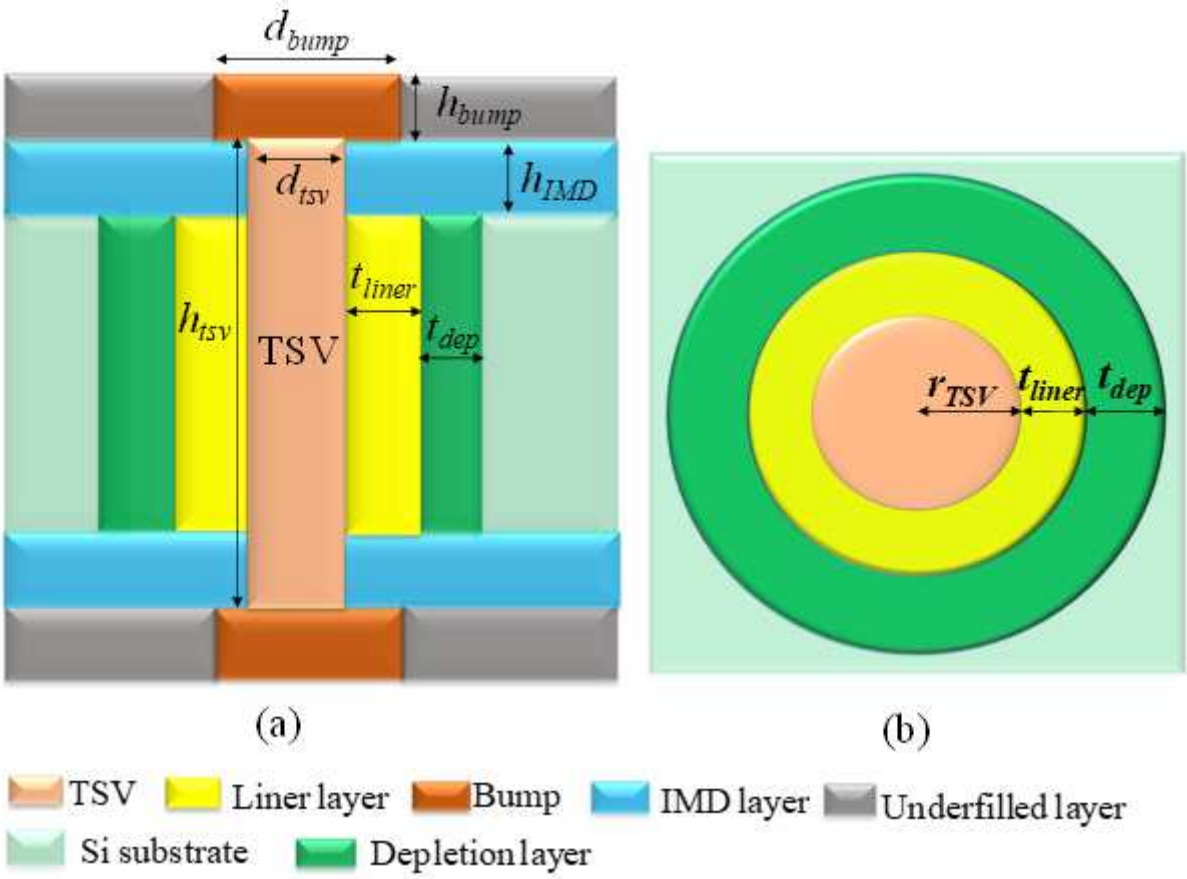

Figure 1

Structure of a cylindrical-shaped TSV (C-TSV): (a) Side-view and (b) Top cross-sectional view of C-TSV.

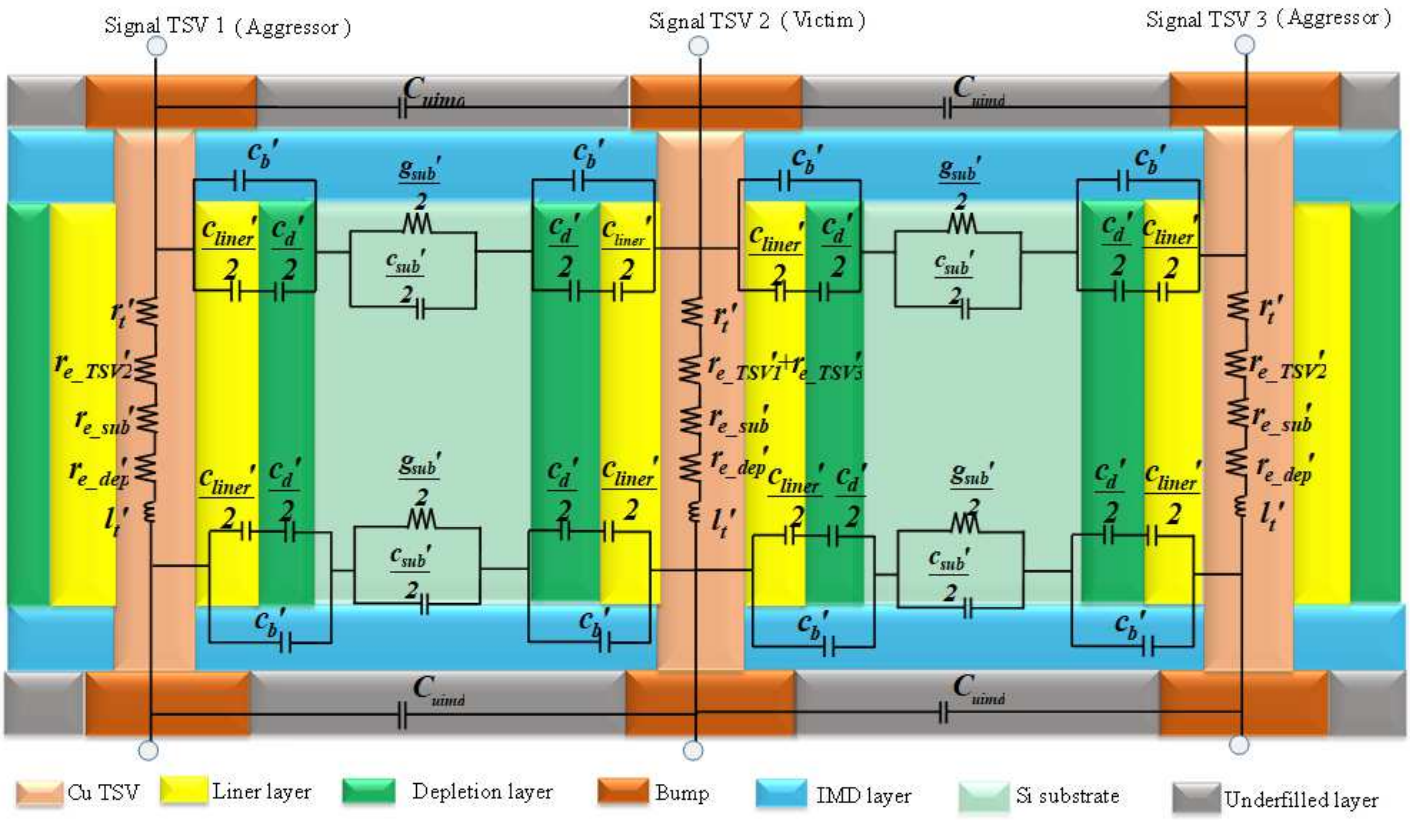

Figure 2

An equivalent RLGC circuit model of the Cu based C-TSV considering eddy effect

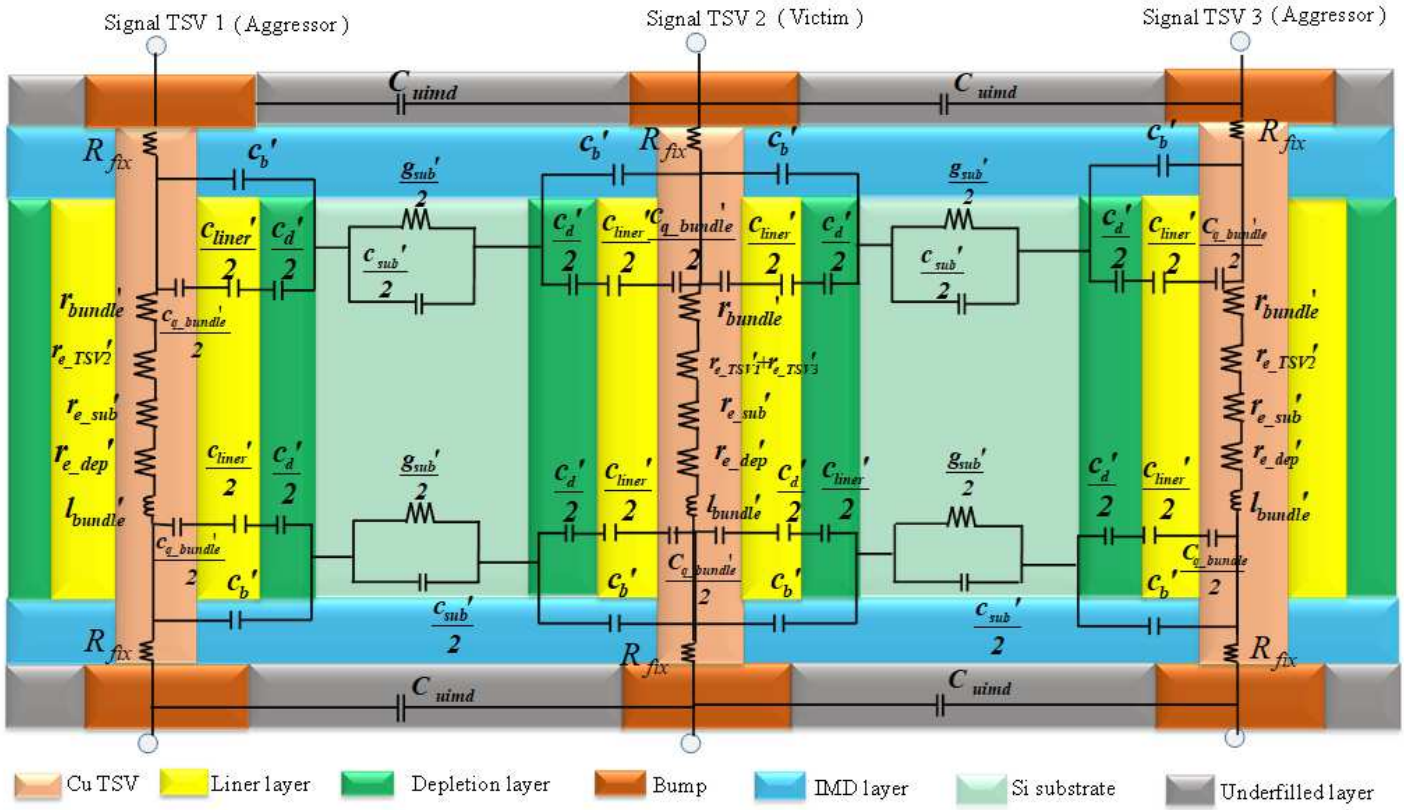

Figure 3

An equivalent RLGC circuit model of the CNT based C-TSV considering eddy effect

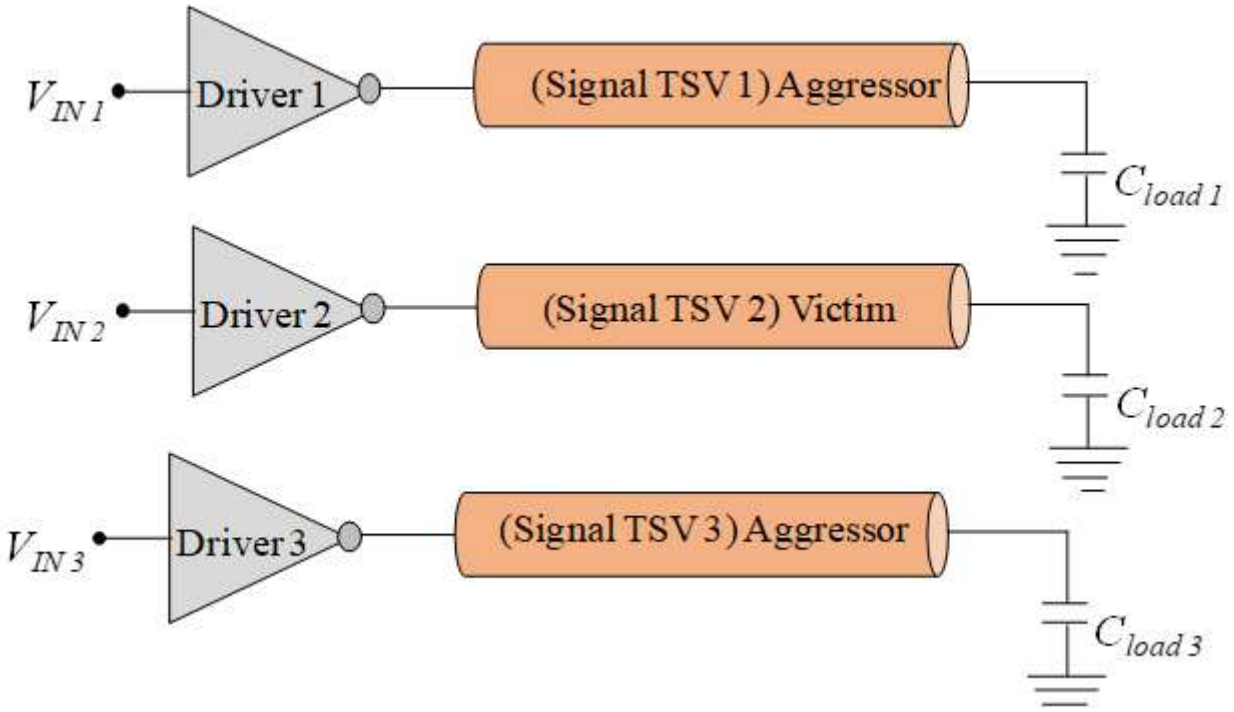

Figure 4

Driver-Via-Load (DVL) setup for circuit-level simulation

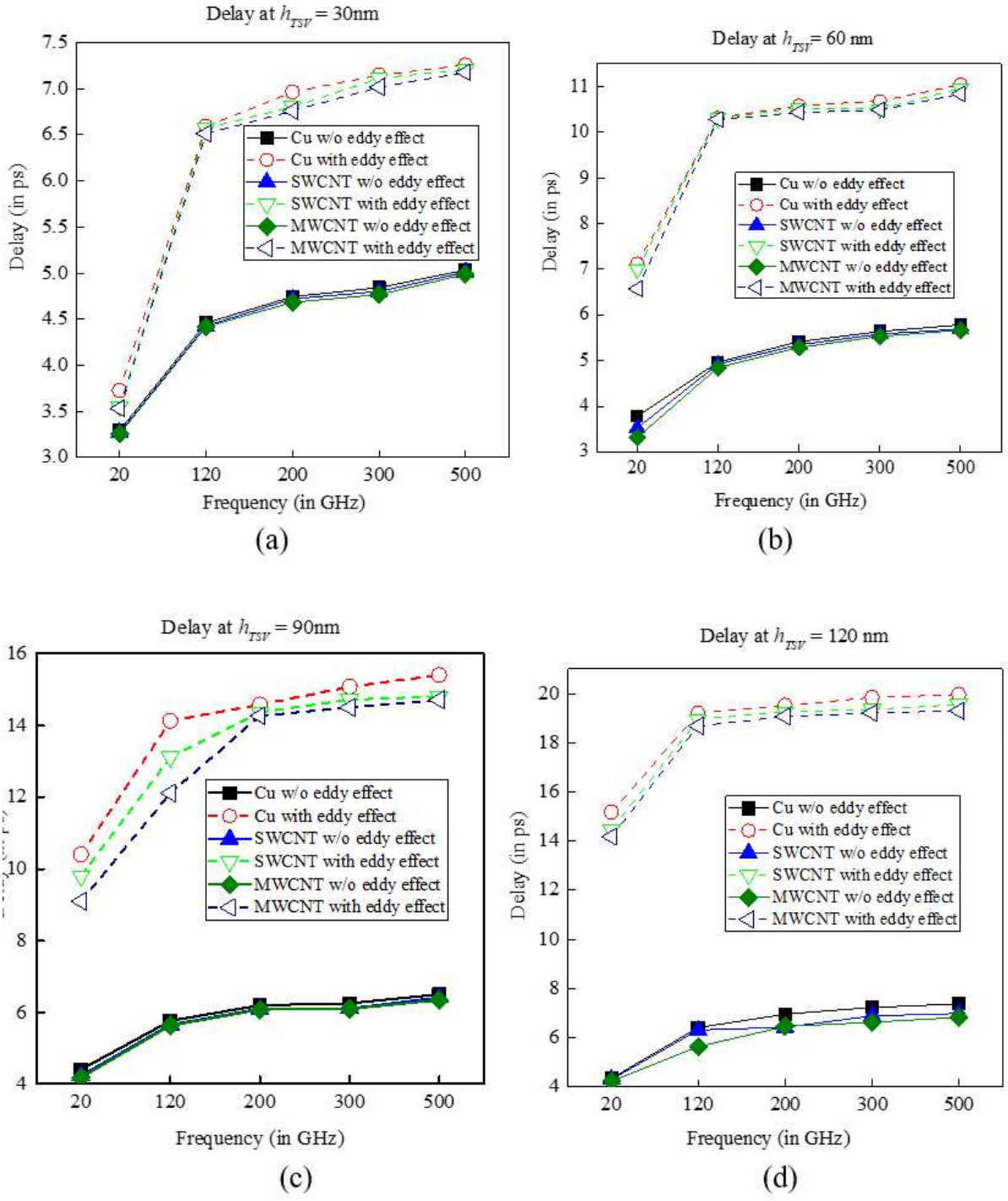

Figure 5

Crosstalk delay of Cu, SWCNT and MWCNT bundle based TSV at via heights of (a) hTSV=30 μm, (b) hTSV=60 μm, (c) hTSV=90 μm and (d) hTSV=120 μm

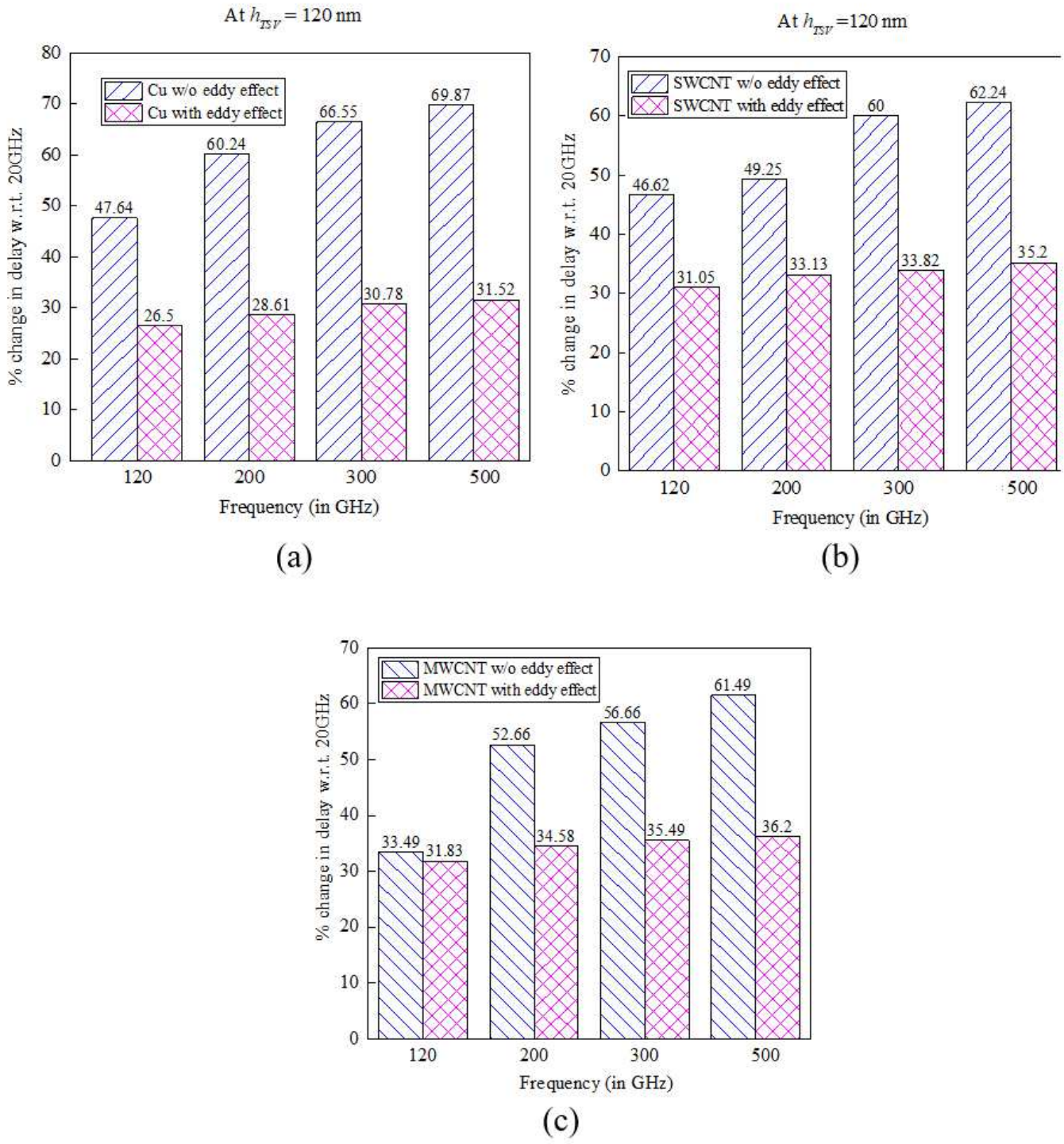

Figure 6

Percentage change in the crosstalk delay of (a) Cu, (b) SWCNT bundle and (c) MWCNT bundle for different frequencies w.r.t. the delay obtained at 20 GHz with and without considering the eddy effect at hTSV = 120 nm.

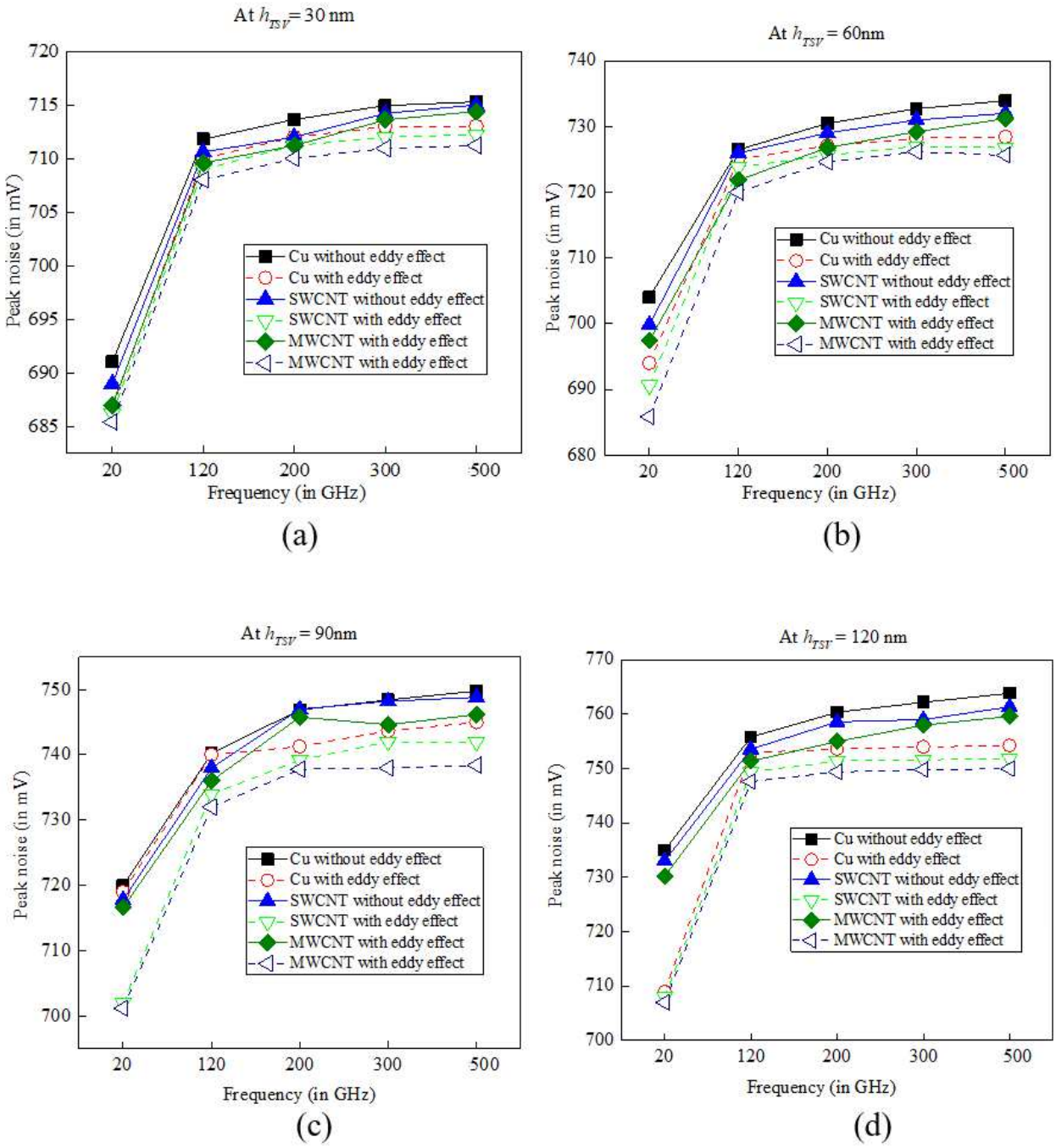

Figure 7

Peak noise of Cu, SWCNT and MWCNT bundle based TSV at via heights of (a) hTSV=30 μm, (b) hTSV=60 μm, (c) hTSV=90 μm and (d) hTSV=120 μm

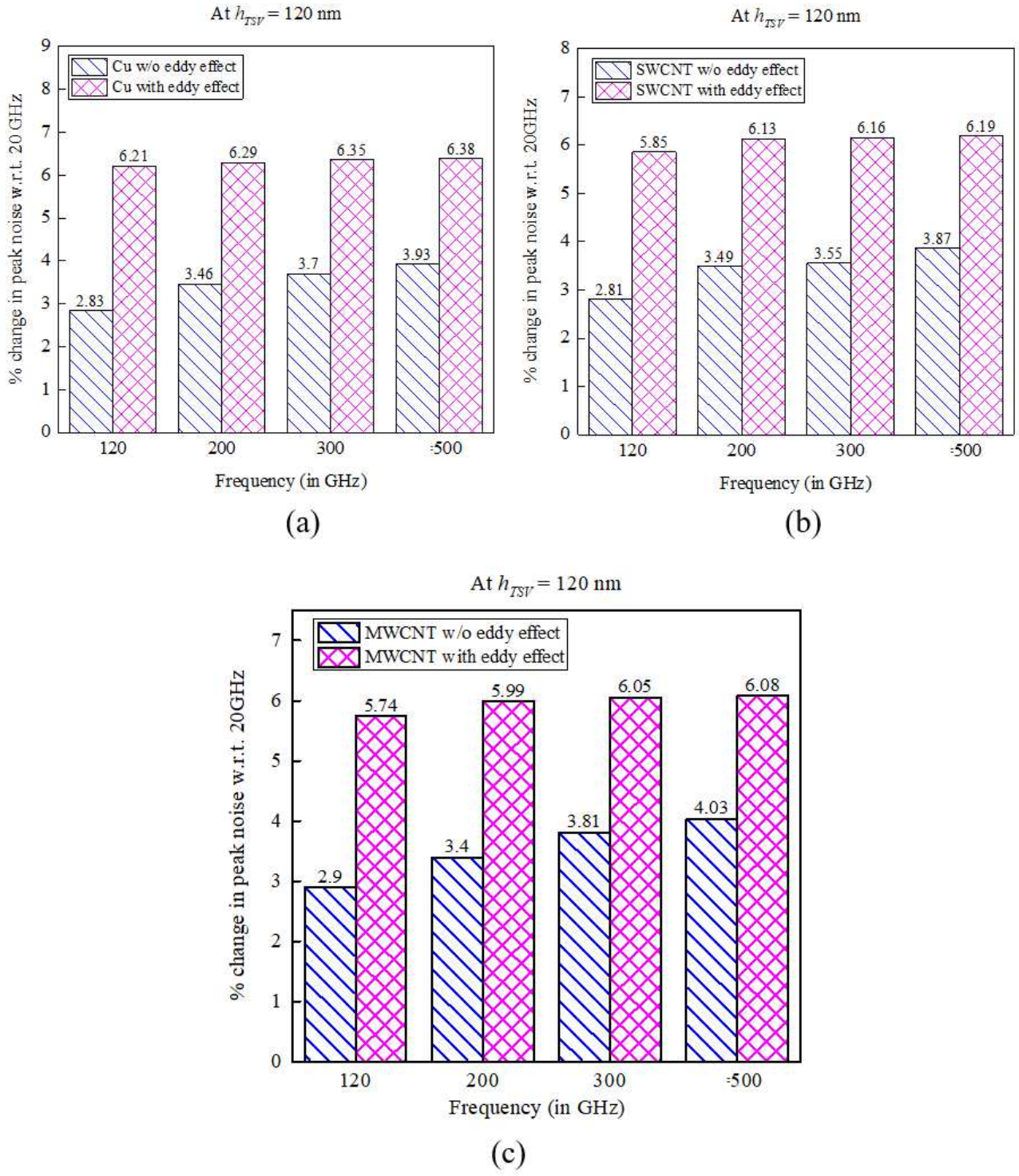

Figure 8

Percentage change in peak noise of (a) Cu, (b) SWCNT bundle and (c) MWCNT bundle for different frequencies w.r.t. the noise obtained at 20 GHz with and without considering the eddy effect at hTSV = 120 nm.

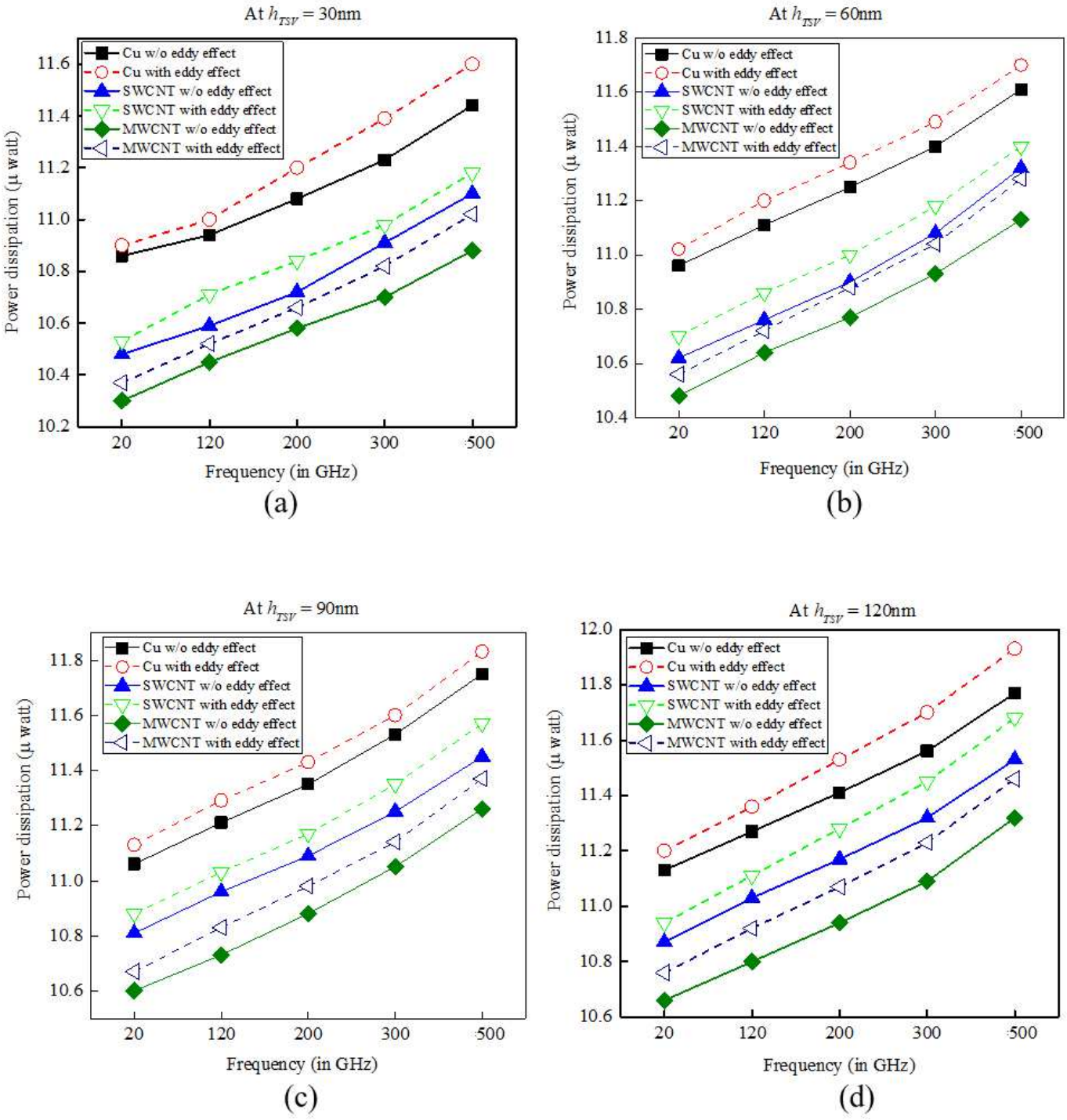

Figure 9

Power dissipation of Cu, SWCNT and MWCNT bundle based TSV at via heights of (a) hTSV=30 μm, (b) hTSV=60 μm, (c) hTSV=90 μm and (d) hTSV=120 μm

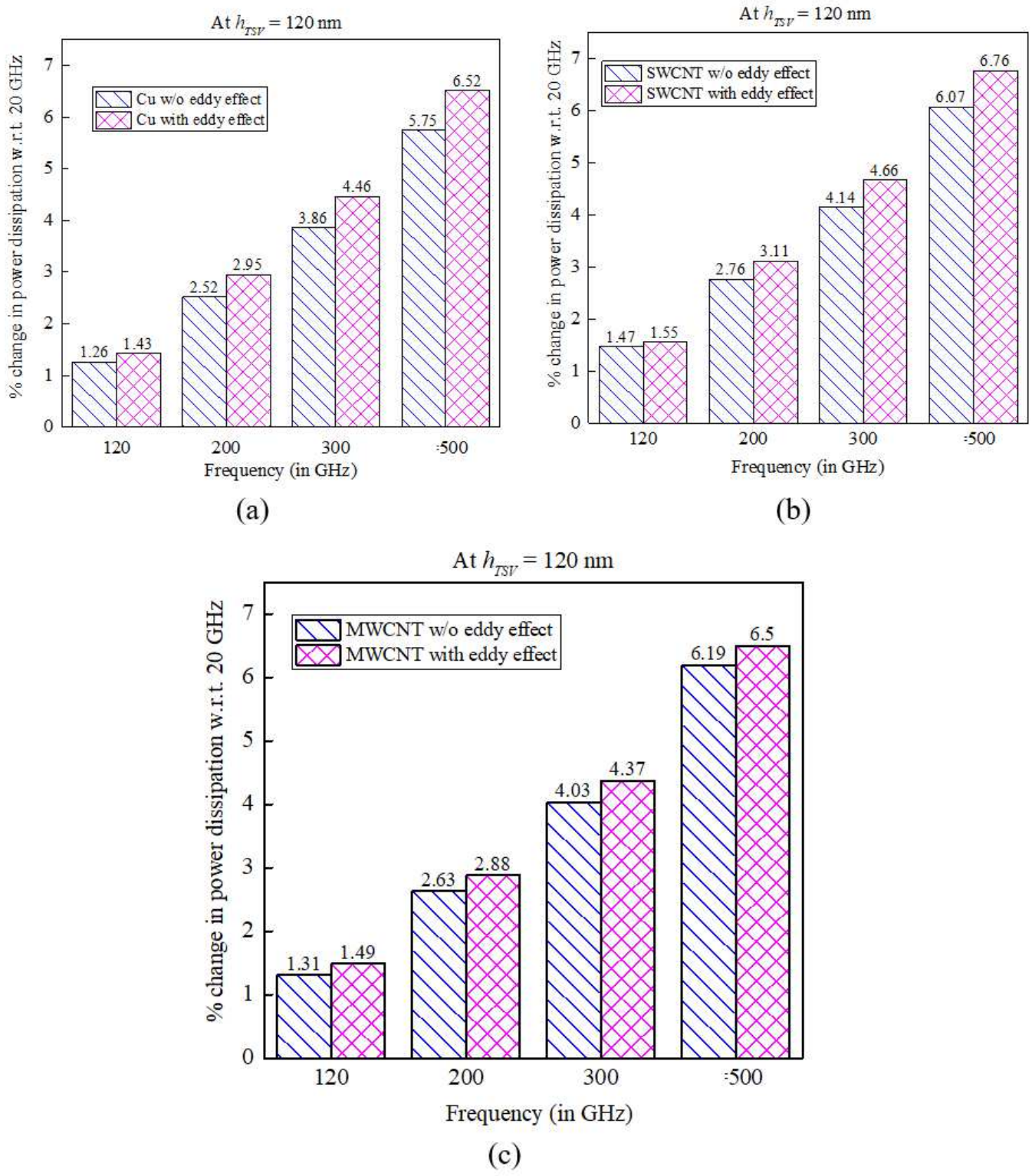

Figure 10

Percentage change in power dissipation of (a) Cu, (b) SWCNT bundle and (c) MWCNT bundle for different frequencies w.r.t. the power obtained at 20 GHz with and without considering the eddy effect at hTSV = 120 nm.