

# Impact of interface trap charges on Junctionless double and triple metal gate High-k Gate All Around Nanowire FET based Alzheimer Biosensor

Rishu Chaujar (✉ [chaujar.rishu@dtu.ac.in](mailto:chaujar.rishu@dtu.ac.in))

Delhi technological University <https://orcid.org/0000-0002-0161-8449>

Mekonnen Getnet Yirak

Delhi Technological University

---

## Research Article

**Keywords:** Interface trap charge, bio-sensor, junctionless-TMG-High-k, gate all around, NWFET, atlas-3D

**Posted Date:** June 9th, 2021

**DOI:** <https://doi.org/10.21203/rs.3.rs-504559/v1>

**License:**   This work is licensed under a Creative Commons Attribution 4.0 International License.

[Read Full License](#)

---

# Impact of interface trap charges on Junctionless double and triple metal gate High-k Gate All Around Nanowire FET based Alzheimer Biosensor

Rishu Chaujar <sup>a,\*</sup> Mekonnen Getnet Yirak <sup>ab</sup>,

<sup>a</sup> Applied Physics Department, Delhi Technological University, Delhi, INDIA

<sup>b</sup> Physics Department, Debre Tabor University, Debre Tabor, Ethiopia

\*Corresponding author email: chaujar.rishu@dtu.ac.in

chaujar.rishu@dtu.ac.in, mekonnengetnet01@gmail.com

## Abstract

In this work, junctionless double and triple metal gate high-k gate all around nanowire field-effect transistor-based APTES biosensor has been developed to study the impact of ITCs on device sensitivity. The analytical results were authenticated using “ATLAS-3D” device simulation tool. Effect of different interface trap charge on the output characteristics of double and triple metal gate high-k gate all around junctionless NWFET biosensor was studied. Output characteristics, like transconductance, output conductance, drain current, threshold voltage, subthreshold voltage and switching ratio, including APTES biomolecule, have been studied in both devices. 184% improvement has been investigated in shifting threshold voltage in a triple metal gate compared to a double metal gate when APTES biomolecule immobilizes on the nanogap cavity region under negative ITCs. Based on this finding, drain off-current ratio and shifting threshold voltage were considered as sensing metrics when APTES biomolecule immobilizes in the nanogap cavity under negative ITCs which is significant for Alzheimer's disease detection. We signifies a negative ITC has a positive impact on our proposed biosensor device compared to positive and neutral ITCs.

**Keywords: - Interface trap charge; bio-sensor; junctionless-TMG-High-k; gate all around; NWFET; atlas-3D**

## 1. INTRODUCTION

Recently, the primary research interest area is biomolecular species detection; detection of these biomolecular species is used for early detection of biological diseases, like Alzheimer's, breast cancer, ovarian cancer (viral diseases), hepatocellular carcinoma (HCC), and other biological diseases. Biological molecules such as RNA, DNA, Uricase, APTES, Streptavidin,  $\text{ChO}_x$ , and Biotin play a vital role in the screening of those diseases[1][2][3]. However, biomolecule detection using a conventional method like surface plasmon resonance, optical measurements, spectrometry, and quartz crystal microbalances are involved multi-stage processes, expensive, time-consuming, and unsuitable for on-line intensive care[4][5][6][7]. To overcome these drawbacks, the new type of FET like, Field-effect transistors (FET) immunosensors[8], Tunnel filed effect transistor[9], and Junctionless FinFET[10] has emerged; because of easy scalability, low power consumption, label-free and high packing density for the detection of biomolecules[1][2].

As the technology grown, FET has been scaled down to increase transistors in a single chip. Bulk metal-oxide field-effect transistors (MOSFETs) performance enhancement has been reached saturation at 20/22nm

complementary metal-oxide-semiconductor generation, forcing Intel's to shift from bulk to multi-gate device structure to continue on the track of Moor's law[11][12]. However, Leakage current, mobility degradation, subthreshold swing, short response time, hot carrier, power consumption, parasitic resistance, and threshold voltage roll-off have been a serious problem when the device shifts to ultra-small scale device dimension[13][14]. Moreover, the transistor faces other significant challenges at ultra-small scale such as electromigration, thermal budget management, 3-D process integration, and dependence of defects along with the oxide interface trap charge due to high electric field[15][16][17]. Gate leakage current limit's device reliability and memory even lower than simple transistor logic under thinner gate oxide, like SiO<sub>2</sub>)[18] [19]. To overcome those device fabrication problems, different approaches like multi-gate device architecture[20] and a dielectric modulating technique (replacing thinner silicon oxide (SiO<sub>2</sub>) gate insulator with high-k dielectric constant material)[21] have been proposed. High-k gate oxide makes thicker equivalent oxide thickness (EOT), and it is used to overcome quantum mechanical tunneling and SCEs under the nanoscale regime of gate oxide thickness[13][22][23]; this can be obtained using eq. (1)[13].

$$EOT = t_{SiO_2} + \left( \frac{K_{SiO_2}}{K_{high-k}} \right) t_{high-k} \quad (1)$$

Where  $t_{SiO_2}$  and  $t_{high-k}$  are the thickness of SiO<sub>2</sub> and HfO<sub>2</sub> dielectric material respectively,  $K_{SiO_2}$  and  $K_{HfO_2}$  are dielectric constants of SiO<sub>2</sub> and HfO<sub>2</sub> oxide material, respectively.

Another problem of CMOS transistor is p-n junction related problem (random dopant fluctuations and an abrupt (unexpected) junction), when channel length and thickness are below 10nm[16][24], which requires expensive fabrication techniques due to diffusion of impurities between p- or n-type drain/source region and n- or p-type body region leads to great difficulty in the fabrication process of small scale devices[25][26]. Dopingless (DL) transistors having uniform doping profiles from source to drain through the channel region are considered significant device architecture for mass production of a microchip in the semiconductor industry. They will have a solution for an abrupt junction problem [24][27]. Dopingless transistor has various advantages over CMOS transistors, including reducing SCEs and accessible for the fabrication process[28]. Therefore, one of the most promising candidate architectures for CMOS fabrication technology is dopingless (DL) MOSFET because it is cost-effective, easy to fabricate, and low power consumption[29]. The impact of fringing capacitance from the polysilicon gate can be controlled using dissimilar gate (multigate)/different gate electrodes with different work-function[30].

Additionally, the ultrathin channel material favors doping less or lightly doped to eradicate threshold-voltage fluctuation due to the variation of dopant atoms and mobility degradation due to depletion charges fluctuation[31]. Nevertheless, in nanoscale MOSFETs, induced hot-carrier, resulting from impact ionization in the channel near the drain junction, becomes a significant reliability concern. In general, hot carriers are injected into the gate oxide due to the high drain electric field, which gives rise to localized interface states and oxide charges near the drain junction and degrades the electrical characteristic parameters [32].

In this paper, effect of interface trap charges (ITCs) on the electrical output characteristics of triple metal gate high-k gate all around junctionless NWFET based Alzheimer biosensor has been proposed using atlas-3D device simulation tool to study the effect of ITCs on device performance; considering trap charges near the insulator/semiconductor interface as shown in **Fig 1**. Including APTES biomolecule on output characteristics of n-type double and triple metal gate JL-GS-GAA-NWFET, has been analyzed under room

temperature. The outcome of localized/interface trap charge on the device output physical characteristics, such as output resistance, threshold voltage variation, transconductance, early voltage, intrinsic voltage gain, output conductance, device efficiency, and surface potential, has been extensively studied.

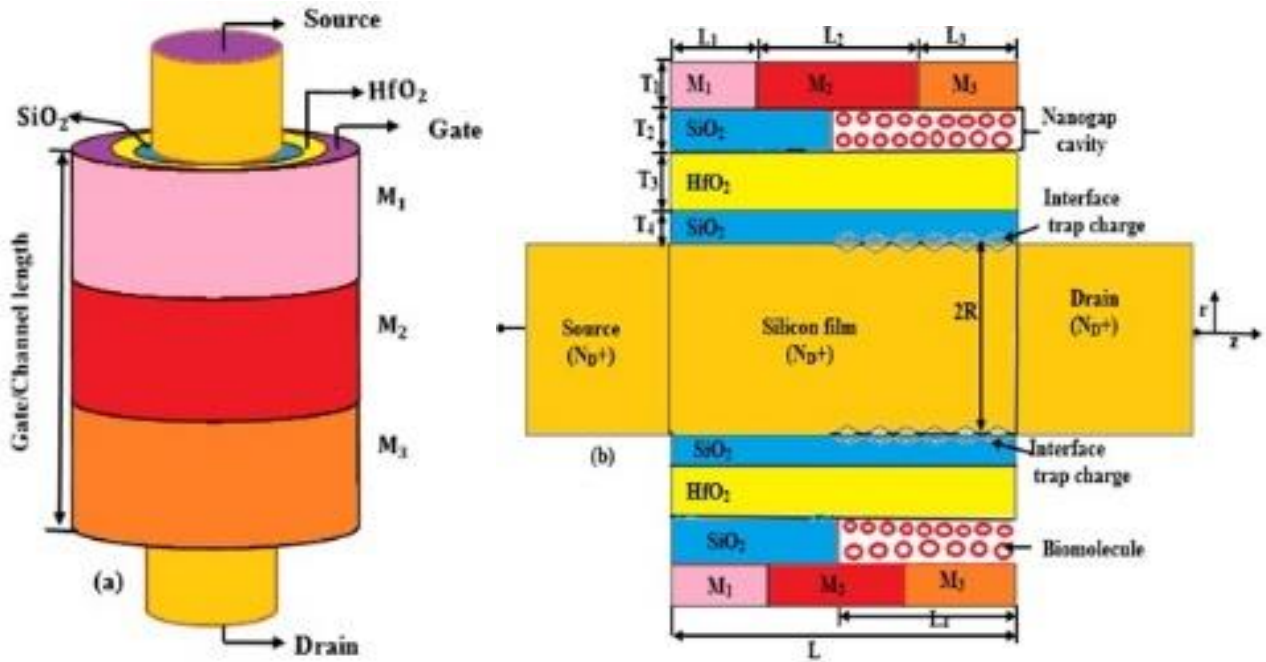
## 1.2 DEVICE SIMULATION AND STRUCTURE

Device structure for n-type junctionless high-k triple metal gate all around NWFET based biosensor with ITCs have been illustrated in **Fig 1(b)**. Here,  $L_1$  (6nm),  $L_2$  (8nm),  $L_3$  (6nm) are the lengths of  $M_1$ ,  $M_2$ , and  $M_3$  respectively and  $L_4$  (10nm), are length of the nanogap cavity and silicon dioxide ( $\text{SiO}_2$ ), etching near to drain and source end, and  $L$  (20 nm) channel length.  $T_1$ ,  $T_2$ ,  $T_3$  and  $T_4$  are the thickness of metal gate, hafnium oxide, nanogap cavity, and interface ( $\text{SiO}_2$ ) oxide, respectively, and  $2R$  is the diameter of the channel. A ( $T_4 = 0.3\text{nm}$ ) thickness of  $\text{SiO}_2$  interface layer is considered between hafnium oxide and silicon film to create a compatible region between hafnium oxide and silicon film for carrier mobility[33]. The three gate materials denoted by  $M_1$ ,  $M_2$  and  $M_3$  have different work-function given by  $\Phi_{M1} = 4.86$ ,  $\Phi_{M2} = 4.96$  and  $\Phi_{M3} = 4.50$ , respectively. The intermediate work-function ( $\Phi_{M1}$ ) near to the source is used to control electron saturation velocity and doping fluctuation, the highest work function ( $\Phi_{M2}$ ) between source end and drain end is used to control potential profile along the channel, which intern reduce drain induced barrier lowering (DIBL) and lower work-function near to drain ( $\Phi_{M3}$ ) is used for screening effects and controls high drain electric field fluctuation due to  $V_{DS}$ [34][35]. The nanogap cavity region used as a detecting site in which the target biomolecules (APTES,  $\epsilon = 3.57$ ) and (air=  $\epsilon = 1.0$ ) are assumed to be uniformly immobilized in this region by introducing their dielectric constant[36]. Different types of ITCs (positive and negative) given by ( $N_f = \pm 5 \times 10^{16} \text{cm}^{-2}$ ) and also without interface (Neutral) charge ( $N_f = 0$ ) are simulated interchangeably to examine the ITCs impact of the proposed device performance.

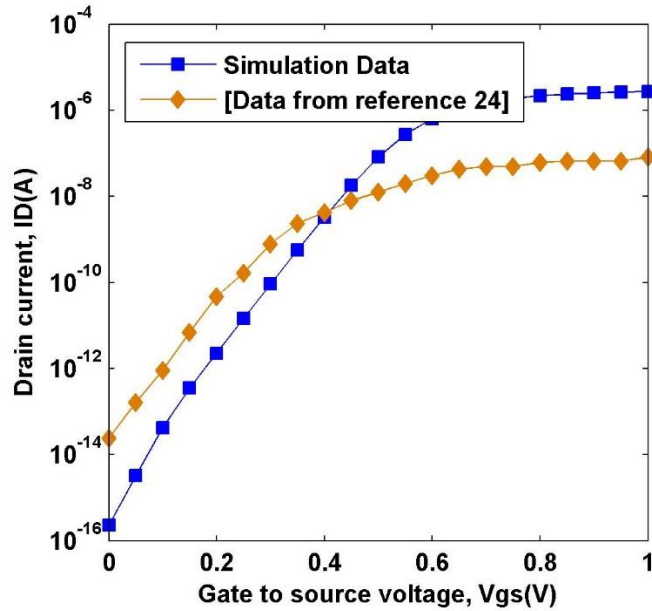
Parameters	DG-GAA-JL-NWFET		TG-GAA-JL-NWFET		
Length of the channel (nm)	20		20		
Hafnium Oxide thickness (nm)	$\text{HfO}_2 = 1.5$ & $\text{SiO}_2 = 0.3$		$\text{HfO}_2 = 1.5$ & $\text{SiO}_2 = 0.3$		
Oxide thickness near to the source (nm)	$\text{SiO}_2 = 1$		$\text{SiO}_2 = 1$		
Oxide length near to the source (nm)	$\text{SiO}_2 = 10$		$\text{SiO}_2 = 10$		
Nanogap cavity length near to drain (nm)	10		10		
Drain/Source thickness (nm)	10		10		
Source/Drain length (nm)	10		10		
Nanogap cavity thickness (nm)	1		1		
The diameter of silicon (nm)	10		10		
Interface trap charges (ITCs)	$\pm 5 \times 10^{12} \text{cm}^{-2}$		$\pm 5 \times 10^{12} \text{cm}^{-2}$		
Source/Drain & Channel Doping ( $N_{D+}$ )	$10^{19} \text{cm}^{-3}$		$10^{19} \text{cm}^{-3}$		
Oxide Dielectric constant	$\text{SiO}_2 = 3.9$ & $\text{HfO}_2 = 25.0$		$\text{SiO}_2 = 3.9$ & $\text{HfO}_2 = 25.0$		
Gate Work functions (eV)	4.50	4.86	4.86	4.96	4.50

**Table I:-** Proposed device structural parameters.

Several simulations have been carried out using the atlas-3D device simulator to describe the proposed device's electrical properties based on these device descriptions. Here different models are applied, such as (CONMOB) concentration-dependent mobility [37] model, to study doping versus mobility distribution along with bandgap narrowing (BGN) model. Shockley–Read–Hall (SRH) model and Boltz-man transport equation account for minority carriers[38][39]. (CCSMOB) Carrier-carrier scattering mobility model used to study carrier mobility and concentration. CVT models are also considered to study perpendicular and parallel field-dependent carrier mobility and mobility roll-off [38][40]. Carrier transport equations have been solved using Newton’s and Gummel’s numerical methods. Quantum mechanical models have not been invoked in this simulation because the silicon film radius is greater than 4nm[10]. The impression of interface trap charge on device performance has been studied by considering uniformly distributed interface trap charge ( $N_f = \pm 5 \times 10^{12} \text{cm}^{-2}$ ) at the Si–SiO<sub>2</sub> interface, as illustrated in **Fig 1(b)**. The reason is that interface trap charge near the drain side is vulnerable to high drain electric field for under short channel device[31]; this high electric field induces hot carriers and leads to rising localized charge at the Si–SiO<sub>2</sub> interface and will create permanent damage to the device performance[41].



**Fig 1. (a)** 3D schematic diagram and **(b)** 2D cross-sectional interpretation with nanogap cavity for n-type triple metal gate high-k gate AA-JL-NWFET.



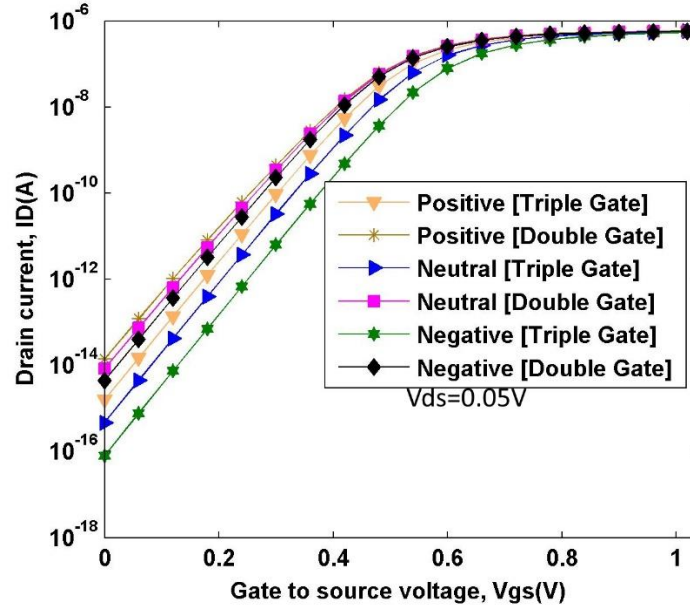
**Fig 2.** Calibration of simulation results compared with data from reference [24] for n-type triple metal gate high-k gate AA-JL-NWFET without ITCs and nanogap cavity region at ( $V_{DS} = 0.05V$ ).

### 1.3 RESULTS AND DISCUSSION

The output characteristics of double and triple metal gate junctionless high-k gate all around NWFET-based Alzheimer Biosensor have been examined incorporating interface trap charges.

#### a) Effect of ITCs on drain current

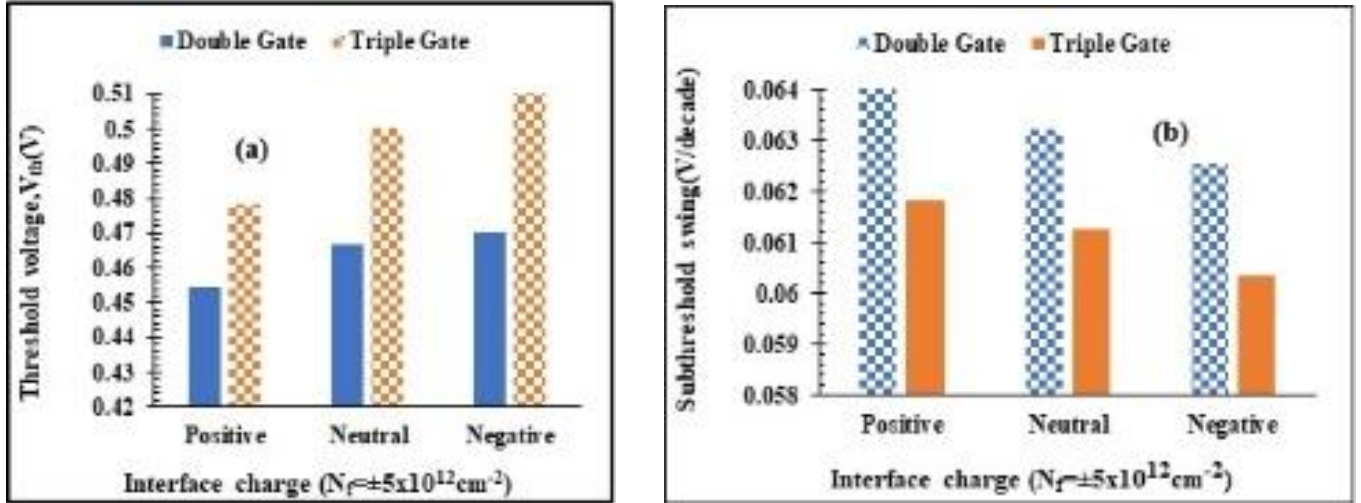
**Fig 3.** Illustrates the simulated results of  $I_D$ - $V_G$  transfer characteristics on log scale at  $V_D = 0.05V$  with interface trap charge of double and triple metal gate. The triple metal gate has a lower leakage current compared to a double metal gate. The reason is that the intermediate work-function ( $\Phi_1$ ) near to the source region is used to control electron saturation velocity and hot carrier effects through the channel. Highest work-function ( $\Phi_2$ ) lowers drain-induced barrier lowering and parasitic resistance, thereby increases gate controllability[15]. Since ITCs rise at  $S - SiO_2$  interface, it will accept an electron for an acceptor-type ITC, and it acts as a fixed negative interface trap charge. Likewise, the donor type interface trap acts as a positive localized charge. These interface traps can be transferred into equivalent interface fixed charge led to band bending under the gate. Greater change in flat band voltage under the damaged region affects electron mobility in the channel[41]. **Fig 3.** Illustrates lower leakage current for negative interface charge and higher leakage current for positive interface charge in both devices; this is because negative ITC mainly reduces DIBL and hot carrier effects in contrary increases mobility carries in the channel. For triple metal gate,  $I_{OFF}$  results of positive and negative interface trap charges are  $1.5 \times 10^{-15}A$  and  $7.97 \times 10^{-17}A$  respectively at  $V_{GS} = 0$  and  $V_{DS} = 0.05V$ .



**Fig 3.** Effect of interface trap charge on  $I_D-V_G$  for n-type double and triple metal gate high-k gate AA-JL-NWFET without cavity region.

**b) Effect of ITCs on subthreshold swing and threshold voltage ( $V_{th}$ )**

**Fig 4.** Illustrates simulated results of (a) threshold voltage ( $V_{th}$ ) (b) subthreshold swing at  $V_{gs} = 1.0V$  and  $V_{DS} = 0.05V$  with ITCs for double and triple metal gate. A lower subthreshold slope has been observed under the triple metal gate compared to the double metal gate. The work-function ( $\Phi_1$ ) near to the source region is used to control carrier injection through the channel and the highest work-function the ( $\Phi_2$ ) develops a barrier potential used to reduce reverse current from the drain through the channel, thereby increasing mobility carriers [15]. Lowest work-function of the metal gate ( $\Phi_3$ ) drain side reduces hot-carriers induced due to high electric field. Variation in threshold voltage is due to different localized/interface trap charges, which introduces a step potential profile in the channel due to the high electric field near the drain side; will rise gate and substrate current; this creates damage in the oxide interface near the drain junction. The metal gate work-function ( $\Phi_3$ ) lowers the peak electric field at the drain side and raises the average electric field near the gate to enhance device performance[41]. It is clear that **Fig 4.** Demonstrates a negative interface trap charge increase threshold voltage while decreasing under positive ITC due to induced hot carriers in the case of positive ITC; negative ITC increases carrier concentration on the channel for n-type channel CMOS device reduces leakage current and subthreshold swing[42]. Also, the fixed localized charge at the interface cause band bending under the gate, leading to changes in flat band voltage in the damaged region led to a change threshold voltage[43]. Higher degradation of SS in the triple metal gate for negative ITCs is investigated due to higher electron mobility and threshold voltage compared to positive interface trap charge; this enhances gate electrostatic control[44], as shown in **Fig 4.(b)** compared to a double metal gate transistor.



**Fig 4.** Variation of (a)  $V_{th}$  and (b) subthreshold swing, with ITCs for n-type double and triple metal gate AA-JL-NWFET without nanogap cavity at ( $V_{DS} = 0.05V$  and  $V_{GS} = 1.0V$ ).

### c) Effect of interface charge on device sensitivity ( $V_{th}$ and $S_{I_{OFF}}$ )

The threshold voltage is an essential characteristic of NW-MOSFET biosensor used as the sensing parameter to detect the device's sensitivity when the biomolecule interacts with the device. The detection mechanism of biomolecule species is carried out by introducing APTES (biomolecule) dielectric constant in the nanogap cavity. **Fig 5.** (a) demonstrates the effect of APTES biomolecule on shifting threshold voltage ( $\Delta V_{th}$ ) and (b) drain off-current ratio for n-type double and triple metal gate JL-high-k-GAA-NWFET with ITCs. Shifting threshold voltage ( $V_{th}$ ) of MOSFET device is obtained using **eq. (2)**[45].

$$\Delta V_{th} = |V_{th}(\epsilon_{APTES} = 3.57) - V_{th}(\epsilon_{air} = 1)| \quad (2)$$

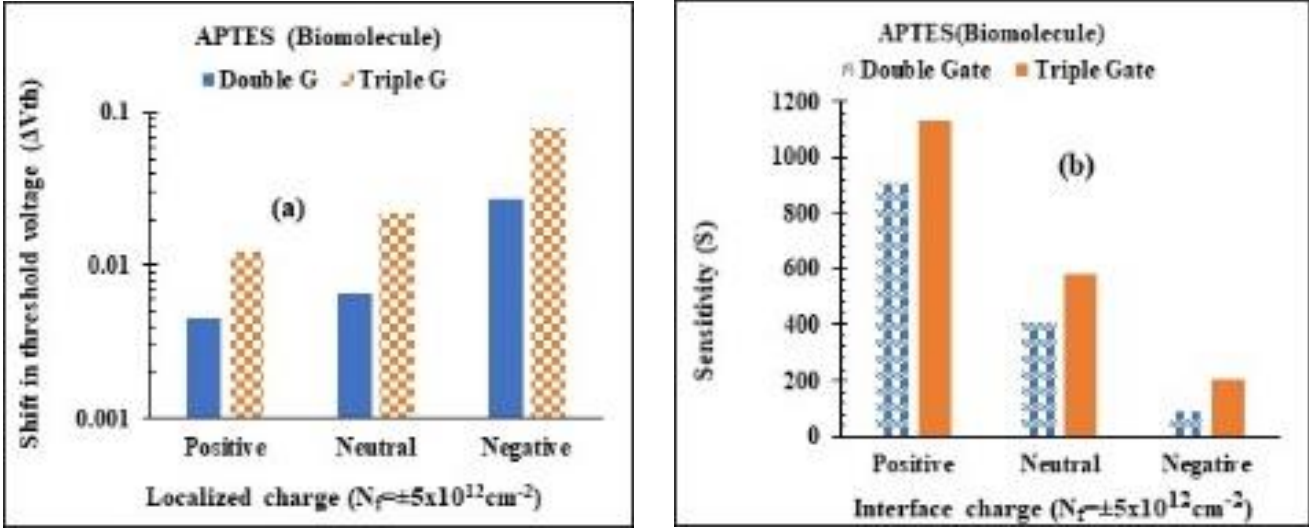
Where ( $\epsilon_{APTES} = 3.57$ ) represents APTES biomolecule dielectric constant and ( $\epsilon_{air} = 1$ ) is air dielectric constant placed in the nanogap cavity region.

**Figure 5(a).** Demonstrates higher threshold voltage shifting for negative interface charge in both devices because negative ITC increases mobility carrier throughout the channel and reduce threshold voltage roll-off. This is because negative ITC is mainly used to improve mobility carriers and stabilize high electric fields near the drain for the n-type channel. For a positive ITCs, the device exposed to short channel effects led to threshold voltage decay. In addition to the interface trap charge, biomolecule (APTES) affects device sensitivity (shifting threshold voltage), as illustrated in **Fig 5(a)**.

**Fig 5(b).** Shows drain off-current ratio ( $S_{I_{off}}$ ) is decrease for negative interface charge due to lower variation of leakage current. The result shows that higher drain off-current ratio for positive and neutral compared to negative ITC; because of, hot-carriers induced by localized charge and high drain electric field near drain side in the presence of positive and neutral ITCs increase leakage current than negative ITCs; also, drain induced barrier lowering effects experienced by positive and neutral ITCs. At negative ITCs, with and without biomolecule,  $I_{OFF}$  ratio is lower than positive ITCs due to less induced hot-carriers and average electric field experienced by negative interface charge. Sensitivity ( $S_{I_{off}}$ ) or drain-off current ratio is given by **eq. (3)**.



$$S_{I_{off}} = \frac{I_{off}(\text{with biomolecule Species})}{I_{off}(\text{without biomolecule Species})} \Big|_{\text{at } V_{gs} = 0} \quad (3)$$

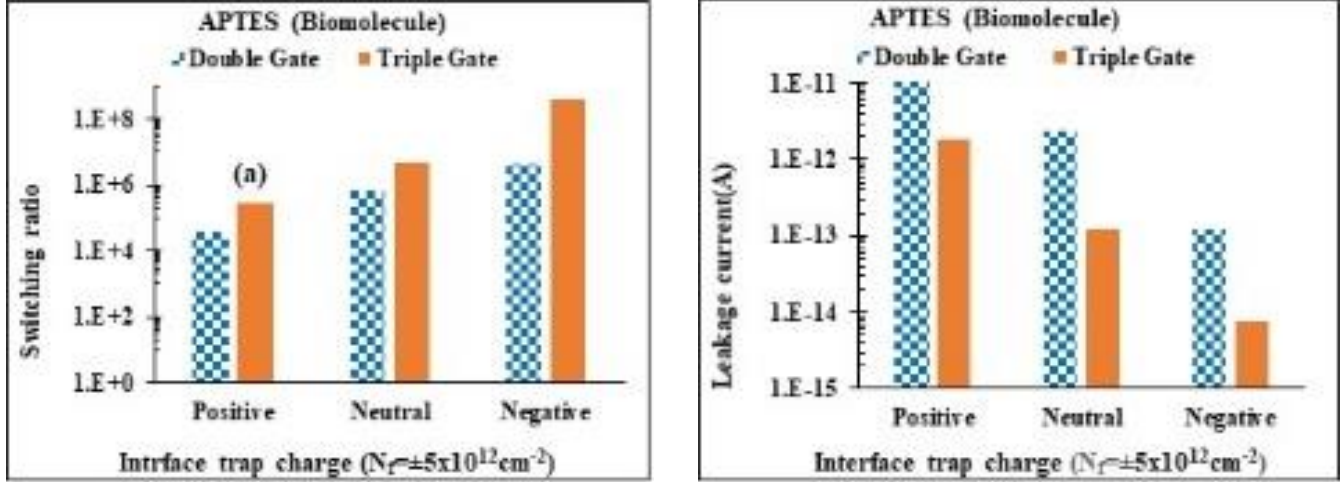


**Fig 5.** Variation of (a) shifting threshold voltage (b) sensitivity ( $S_{I_{off}}$ ), with ITCs for n-type double and triple metal gate high-k gate all around JL-NWFET at ( $V_{DS} = 0.05V$  and  $V_{GS} = 1.0V$ ).

Generally, Higher variation of threshold voltage is observed in a triple metal gate than a double metal gate. The work-function ( $\Phi_1$ ) near the source region increases uniformity, and mobility of carriers through the channel reduces hot carrier and impact ionization effects. Negative ITC in both devices is used to control electron velocity through the channel. In triple metal gate, the intermediate higher work-function the ( $\Phi_2$ ) and lower work-function( $\Phi_3$ ) reduces threshold voltage roll-off and drain-induced barrier lowering impacts in addition to parasitic resistance, thereby enhance gate capacity[42].

#### d) Impact of ITCs on switching ratio and leakage current

**Fig 6.** Illustrates the variation of (a) switching ratio ( $\frac{I_{on}}{I_{off}}$ ), (b) leakage current at  $V_D = 0.05V$  with ITCs ( $N_f = \pm 5 \times 10^{12}$ ) in both double and triple metal gate transistors. Lower leakage current and higher switching ratios are investigated in triple metal gate than double metal gate device. This is the dissimilar gate electrodes effect that reduces gate parasitic resistance and induced hot-carriers caused by the polysilicon gate and high drain electric field. In both devices, higher switching and lower leakage current are investigated with negative ITC compared to positive and neutral ITCs; negative ITCs can mitigate DIBL and induce hot-carrier effects, thereby increasing mobility carriers [42]. Thus, higher switching ( $I_{ON}/I_{OFF}$ ) ratio in the case of negative interface trap charges while reduced switching ( $I_{ON}/I_{OFF}$ ) ratio in the case of neutral and positive interface charges as illustrated in **Fig 6(a)**.



**Fig 6 (a).** Variation of switching ratio **(b)** leakage current, with different ITCs for n-type double and triple metal gate high-k gate all around junctionless NWFET at ( $V_{DS} = 0.05V$  and  $V_{GS} = 1.0V$ ).

When APTES (biomolecule) immobilizes in the nanogap cavity, drain on current increases while drain off-current decreases. The reason is higher biomolecule dielectric constant decreases electron tunneling from the gate and body substrate, led to improves gate electrostatic control in ultra-small gate oxide thickness in short channel device [14]. Drain off current ratio decreases/increases for positive /negative interface trap charge in all operation regions. Reduced  $I_{on}/I_{off}$  ratio for positive interface trap charge and improved  $I_{on}/I_{off}$  ratio for negative interface trap charge, as shown in **Fig 6(a)**. For instance, switching ( $I_{ON}/I_{OFF}$ ) ratio of APTES (biomolecule) are  $4.18 \times 10^6$  and  $4.18 \times 10^8$  respectively for double and triple metal gates of the proposed device at negative interface trap charge (ITC).

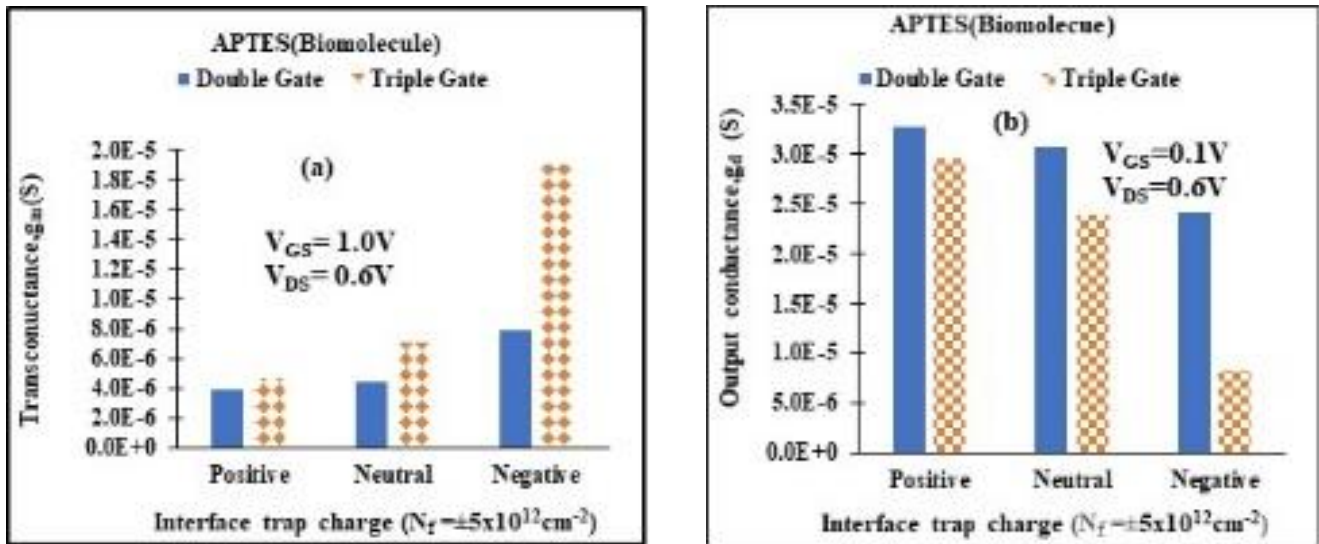
**Fig 6(b).** Demonstrates the impact of ITCs on leakage current with APTES biomolecule for double and triple metal gate high-k gate all around junctionless NWFET. It clearly shows, lower leakage current for negative ITCs than positive ITCs; the reason is that the negative interface trap charge increases mobility carriers through the channel while the positive ITCs reduce mobility carriers through the channel due to trapping localized charge and induced hot-carriers. Reduced charge carriers in the channel due to positive ITC allow the depletion layer to become thicker across the reverse junction that allows the flow of charge carriers in OFF-state, resulting from higher leakage current[16]. Hot-carriers generated high drain electric fields, grows serious problems, such as reliability and device efficiency[46].

The output characteristics such as transconductance, and output conductance are known as the device analog parameters, which can be used to examine the device's gain (amplification) and reliability[44].Fig 7. Illustrates the impact of ITCs on transconductance and output conductance for double and triple metal gate transistors. **Fig 7(a).** Transconductance  $g_m$  is higher for negative ITCs in both devices. Large transconductance of the device delivers greater amplification when other factors are kept constant and it can be given by **eq. (4)**.

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} \quad (4)$$

**Fig 7(b)**, illustrates the output conductance ( $g_d$ ) of double and triple metal gate high-k gate all around junctionless NWFET, which is used to characterize its output resistance ( $R_{out} = \frac{1}{g_d}$ ) of the device. In both device, outconductance is decreased for negative but increases for positive and it can be obtained using **eq. (5)** at constant gate voltage ( $V_{GS}$ ).

$$g_d = \frac{\partial I_{DS}}{\partial V_{DS}} \quad (5)$$



**Fig 7.** Variation of (a) transconductance (b) output conductance with ITCs for n-type triple metal gate high-k gate all around junctionless NWFET.

## 2 CONCLUSION

In this paper, impact of different ITCs on the electrical characteristics of double and TG-high-k-GAA-JL-NWFET based Alzheimer biosensor has been studied. We have observed that ITCs causes the change in switching ratio, shifting threshold voltage, transconductance, output conductance, leakage current, subthreshold slope, in the presence of APTES biomolecule. For instance, the results of SS at negative ITCs are (62.6 and 60.3)mV/decade for double and triple metal gate devices, respectively. Improved output characteristics, such as threshold voltage (0.47V and 0.54V), shifting threshold voltage (2.75mV and 7.81mV), switching ratio ( $4.18 \times 10^6$  and  $4.12 \times 10^8$ ) and transconductance ( $7.88 \times 10^{-6}$  and  $1.90 \times 10^{-5}$ ) has been examined at negative ITC of double and triple TG-high-k-GAA-JL-NWFET respectively when APTES biomolecule immobilizes in the nanogap cavity. Leakage current result when APTES biomolecule interact with the TG-high-k-GAA-JL-NWFET device at nanocavity in the presence of ITCs

( $N_f = \pm 5 \times 10^{12} \text{ cm}^{-2}$ ) are  $1.79 \times 10^{-12} \text{ A}$ ,  $1.24 \times 10^{-13} \text{ A}$  and  $1.79 \times 10^{-15} \text{ A}$  for positive, neutral, and negative ITCs, respectively. Reduced and rising leakage current due to negative and positive ITCs are 93.6% and 1,343.5%, respectively, have been investigated in the proposed device with respect to undamaged region. Increasing and decreasing of surface potential of the proposed device at ITCs ( $N_f = \pm 5 \times 10^{12} \text{ cm}^{-2}$ ) are 1.54% and 2.39% for positive and negative respectively with respect to undamaged region when APTES biomolecule is immobilized in the nanogap cavity. Generally, we have examined that negative ITC enhances the output characteristics, such as switching ratio, transconductance, output resistance for triple metal than double metal gate -high-k-GAA-JL-NWFET, when APTES biomolecule immobilize in the nanogap cavity. We can conclude that the APTES biosensor with negative ITC is the novel biomarker compared to the positive ITC of the silicon-based device. Since, it introduces reactive amine groups on the silicon surface to detect sugar level variation of saliva caused by Alzheimer's disease. It could also be a potential indicator/biomarker for Alzheimer's disease (AD) detection.

#### **AVAILABILITY OF DATA AND MATERIALS**

We announce that the materials mentioned in the manuscript, as well as all related raw data, will be freely accessible to any scientist who wishes to use them for non-commercial purposes without compromising participant confidentiality.

#### **AUTHORS' CONTRIBUTIONS**

The main idea of this paper was proposed by Dr. Rishu Chaujar prepared the manuscript initially and performed all the steps of the solutions in this research. Both authors read and approved the final manuscript.

#### **FUNDING**

The authors declare that no funding has been received to carry out this research work.

#### **ACKNOWLEDGMENT**

The authors are grateful to the Debre Tabor University, Ethiopia, and Delhi Technological University, India, for providing the necessary monetary and material assistance to carry out this research work.

#### **COMPETING INTEREST**

The authors declare that they have no competing interest.

#### **DISCLOSURE OF POTENTIAL CONFLICTS OF INTEREST**

'Not applicable'

#### **RESEARCH INVOLVING HUMAN PARTICIPANTS AND/OR ANIMALS**

'Not applicable'

#### **INFORMED CONSENT**

'Not applicable'

## References

- [1] Cibele Gouvea, "Biosensors for Health Applications," in *Open access peer-reviewed chapter*, Pier Andrea Serra, Ed. Universidade Federal de Alfenas, Brazil: IntechOpen.
- [2] Y. Wang and G. Li, "Simulation of a silicon nanowire FET biosensor for detecting biotin/streptavidin binding," *2010 10th IEEE Conf. Nanotechnology, NANO 2010*, pp. 1036–1039, 2010.
- [3] Y. Chen *et al.*, "Field-Effect Transistor Biosensor for Rapid Detection of Ebola Antigen," *Sci. Rep.*, vol. 7, no. 1, pp. 4–11, 2017.
- [4] K. Y. Park, M. S. Kim, and S. Y. Choi, "Fabrication and characteristics of MOSFET protein chip for detection of ribosomal protein," *Biosens. Bioelectron.*, vol. 20, no. 10 SPEC. ISS., pp. 2111–2115, 2015.
- [5] A. C. M. de Moraes and L. T. Kubota, "Recent trends in field-effect transistors-based immunosensors," *Chemosensors*, vol. 4, no. 4, 2016.
- [6] H. C. Lau, T. E. Bae, H. J. Jang, J. Y. Kwon, W. J. Cho, and J. O. Lim, "Saliva-based screening approach for Alzheimer's disease via the cell-oriented ion-sensitive field-effect transistor," *Sens. Lett.*, vol. 12, no. 6–7, pp. 1096–1101, 2014.
- [7] B. Shui *et al.*, "Biosensors for Alzheimer's disease biomarker detection: A review," *Biochimie*, vol. 147, no. January, pp. 13–24, 2018.
- [8] Ana Carolina Mazarin de Moraes and Lauro Tatsuo K, "Recent Trends in Field-Effect Transistors-Based Immunosensors," *hemosensors Rev.*, 2016.
- [9] J. Madan and R. Chaujar, "Superlattices and Microstructures Palladium Gate All Around - Hetero Dielectric -Tunnel FET based highly sensitive Hydrogen Gas Sensor," *Superlattices Microstruct.*, pp. 1–8, 2016.
- [10] A. Chhabra, A. Kumar, and R. Chaujar, "Sub-20 nm GaAs junctionless FinFET for biosensing application," *Vacuum*, vol. 160, no. December 2018, pp. 467–471, 2018.
- [11] S. M. Amoroso *et al.*, "Inverse Scaling Trends for Charge-Trapping-Induced Degradation of FinFETs Performance," *IEEE Trans. Electron Devices*, vol. 61, no. 12, pp. 4014–4018, 2014.
- [12] J. Wu, Y.-L. Shen, K. Reinhardt, H. Szu, and B. Dong, "A Nanotechnology Enhancement to Moore's Law," *Appl. Comput. Intell. Soft Comput.*, vol. 2013, pp. 1–13, 2013.
- [13] K. P. Pradhan, S. K. Mohapatra, P. K. Sahu, and D. K. Behera, "Impact of high-k gate dielectric on analog and RF performance of nanoscale DG-MOSFET," *Microelectronics J.*, vol. 45, no. 2, pp. 144–151, 2014.
- [14] N. Thapa and L. Maurya, "Performance advancement of High-K dielectric MOSFET," *Int. J. Innov. Adv. Comput. Sci.*, vol. 3, no. 3, pp. 98–103, 2014.
- [15] Sze, "Performance Investigation of Dual Material Gate Stack Schottky-Barrier Source/Drain GAA MOSFET for Analog Applications," *Phys. Semicond. Devices, Environ. Sci. Eng.*, vol. 10, no. December 2013, pp. 739–751, 2014.
- [16] N. Kumar and A. Raman, "Performance Assessment of the Charge-Plasma-Based Cylindrical GAA Vertical Nanowire TFET with Impact of Interface Trap Charges," *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4453–4460, 2019.
- [17] P. Saha, P. Banerjee, D. K. Dash, and S. K. Sarkar, "Impact of trapped interface charges on short channel characteristics of WFE high-K SOI MOSFET," *Proc. 3rd Int. Conf. 2019 Devices Integr. Circuit, DevIC 2019*, pp. 118–123, 2019.
- [18] A. S. Aji and Y. Darma, "Simulation of Charge-Trapping Effect on Floating Gate Si / Ge / Si Quantum Dots MOSFET Memory with High-  $\kappa$  Tunnel Oxide," in *2013 3rd International Conference on Instrumentation, Communications, Information Technology and Biomedical Engineering (ICICI-BME)*, 2013, no. 1, pp. 269–272.
- [19] Prerna, "Future MOSFET Devices using High-k (TiO<sub>2</sub>) Dielectric," *Int. J. Res. Appl. Sci. Eng. Technol.*, vol. 1, no. 2, pp. 23–28, 2013.
- [20] S. L. Tripathi, R. Mishra, and R. A. Mishra, "Multi-Gate Mosfet Structures With High-K Dielectric Materials," *ournal of Electron Devices*, vol. 16, pp. 1388–1394, 2012.
- [21] R. Chau *et al.*, "Application of high- $\kappa$  gate dielectrics and metal gate electrodes to enable silicon and non-silicon logic nanotechnology," *Microelectron. Eng.*, vol. 80, no. SUPPL., pp. 1–6, 2005.
- [22] S. K. Swain *et al.*, "Effect of High-K Spacer on the Performance of Non-Uniformly doped DG-MOSFET," *Proc. 3rd Int. Conf. 2019 Devices Integr. Circuit, DevIC 2019*, pp. 510–514, 2019.
- [23] V. Kumar, R. Gupta, R. Preet, P. Singh, and R. Vaid, "Performance Analysis of Double Gate n-FinFET Using High-k Dielectric Materials," *Int. J. Innov. Res. Sci. Eng. Technol.*, vol. 5, no. 7, pp. 13242–13249, 2016.
- [24] J. P. Colinge *et al.*, "Nanowire transistors without junctions," *Nat. Nanotechnol.*, vol. 5, no. 3, pp. 225–229, 2010.

- [25] V. P. Georgiev *et al.*, "Experimental and Simulation Study of Silicon Nanowire Transistors Using Heavily Doped Channels," *IEEE Trans. Nanotechnol.*, vol. 16, no. 5, pp. 727–735, 2017.
- [26] L. Ansari, B. Feldman, G. Fagas, J. P. Colinge, and J. C. Greer, "Simulation of junctionless Si nanowire transistors with 3 nm gate length," *Appl. Phys. Lett.*, vol. 97, no. 6, 2010.
- [27] Z. Huang, A. Gao, S. Chen, Y. Wang, and T. Li, "Highly Sensitive Junctionless Nanowire Transistor Biosensor in Detecting Breast Tumor Marker," *Proc. IEEE Sensors*, vol. 2018–Octob, pp. 1–4, 2018.
- [28] S. Ghosh, A. Chattopadhyay, and S. Tewari, "Optimization of Hetero-Gate-Dielectric Tunnel FET for Label-Free Detection and Identification of Biomolecules," *IEEE Trans. Electron Devices*, vol. 67, no. 5, pp. 1–8, 2019.
- [29] G. Jawade, Y. V. Chavan, and S. G. Wagaj, "Simulation of dual spacer double gate junctionless transistor," *Proc. - 2nd Int. Conf. Comput. Commun. Control Autom. ICCUBEA 2016*, pp. 1–4, 2017.
- [30] F. Ana and Najeed-ud-din, "Gate Workfunction Engineering for Deep Sub-Micron MOSFET's: Motivation, Features and Challenges," *Int. J. Electron. & Communication Technol.*, vol. 2, pp. 29–35, 2011.
- [31] E. G. Ioannidis, A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, G. Ghibaudo, and J. Jomaah, "Effect of localized interface charge on the threshold voltage of short-channel undoped symmetrical double-gate MOSFETs," *IEEE Trans. Electron Devices*, vol. 58, no. 2, pp. 433–440, 2011.
- [32] N. Garg, Y. Pratap, M. Gupta, and S. Kabra, "Analysis of Interface Trap Charges of Double Gate Junctionless Nanowire Transistor (DG-JNT) for Digital Circuit Applications," *Proc. Int. Conf. 2018 IEEE Electron Device Kolkata Conf. EDKCON 2018*, pp. 563–567, 2018.
- [33] M. I. B. Chowdhury, M. J. Islam, M. J. Islam, M. M. Hasan, and S. U. Farwah, "Silvaco TCAD based Analysis of Cylindrical Gate -All-Around FET Having Indium Arsenide as channel and Aluminium Oxide as Gate Dielectrics," *J. Nanotechnol. its Appl. Eng.*, vol. 1, no. 1, pp. 1–12, 2016.
- [34] A. Goel, S. Rewari, S. Verma, and R. S. Gupta, "Dielectric Modulated Triple Metal Gate All Around MOSFET (TMGAA) for DNA Bio-Molecule Detection," *2018 IEEE Electron Devices Kolkata Conf.*, vol. 1, pp. 337–340, 2019.
- [35] N. Bagga and S. Dasgupta, "Surface Potential and Drain Current Analytical Model of Gate All Around Triple Metal TFET," vol. XX, no. Xx, pp. 1–8, 2017.
- [36] Y. Pratap, M. Kumar, S. Kabra, S. Haldar, R. S. Gupta, and M. Gupta, "Analytical modeling of gate-all-around junctionless transistor based biosensors for detection of neutral biomolecule species," *J. Comput. Electron.*, vol. 17, no. 1, pp. 288–296, 2018.
- [37] D. S. Software, *Atlas User 's Manual*, no. 408. 2016.
- [38] J. S. Galsin, "Transport Phenomena," in *Solid State Physics*, Elsevier, 2019, pp. 223–242.
- [39] J. Madan and R. Chaujar, "Numerical Simulation of N+ Source Pocket PIN-GAA-Tunnel FET: Impact of Interface Trap Charges and Temperature," *IEEE Trans. Electron Devices*, vol. 64, no. 4, pp. 1482–1488, 2017.
- [40] D. Passeri, A. Morozzi, K. Kanxheri, and A. Scorzoni, "Numerical simulation of ISFET structures for biosensing devices with TCAD tools," *Biomed. Eng. Online*, vol. 14, no. 2, p. S3, 2015.
- [41] Y. S. Jean and C. Y. Wu, "The threshold-voltage model of MOSFET devices with localized interface charge," *IEEE Trans. Electron Devices*, vol. 44, no. 3, pp. 441–447, 1997.
- [42] S. M. W. Localized, "A Compact Model for Threshold Voltage of Interface Trapped Charges," vol. 58, no. 2, pp. 567–571, 2011.
- [43] S. K. Mohapatra, K. P. Pradhan, P. K. Sahu, G. S. Pati, and M. R. Kumar, "The effect of interface trapped charges in DMG-S-SOI MOSFET: A perspective study," *Adv. Nat. Sci. Nanosci. Nanotechnol.*, vol. 5, no. 4, 2014.
- [44] J. Yuan and J. C. S. Woo, "A Novel Split-Gate MOSFET Design Realized by a Fully Silicided Gate Process for the Improvement of Transconductance and Output Resistance," *IEEE ELECTRON DEVICE Lett.*, vol. 26, no. 11, pp. 829–831, 2005.
- [45] E. Rahman, A. Shadman, and Q. D. M. Khosru, "Effect of biomolecule position and fill factor on sensitivity of a Dielectric Modulated Double Gate Junctionless MOSFET biosensor," *Sens. Bio-Sensing Res.*, vol. 13, pp. 49–54, 2017.
- [46] A. Kumar, M. M. Tripathi, and R. Chaujar, "Reliability Issues of In<sub>2</sub>O<sub>5</sub>Sn Gate Electrode Recessed Channel MOSFET: Impact of Interface Trap Charges and Temperature," *IEEE Trans. Electron Devices*, vol. 65, no. 3, pp. 860–866, 2018.