**Supplementary Information**

**Ultra-fast Data Sanitization of SRAM by Back-biasing to Resist a Cold Boot Attack**

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**Erasing time depending on load capacitance**



**Figure S1.** Capacitance dependent erasing for **(a)** permanent and **(b)** temporary erasing at 298 K and 173 K.

**Layout innovation for back-bias utilized 6T-SRAM**



**Figure S2.** **(a)** Conventional layout of high-density 6T-SRAM. **(b)** Possible layout innovation to realize proposed data sanitization scheme by back-biasing.

**Cross-section of high-density 6T-SRAM layout**



**Figure S3.** Cross-section of conventional layout of high-density 6T-SRAM and possible layout innovation to realize proposed data sanitization scheme by back-biasing.