# Design,Simulation And Analysis of Junction Version Multi-Fin FINFET

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**Research Article**

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# Design, Simulation and Analysis of Junction version Multi-Fin FINFET

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*Abstract* — **This paper presents a 3-D statistical simulation study of Multi-fin junction FinFET for different technology nodes 32nm, 24 nm & 10 nm. For each and every technology node their corresponding Electrical parameters like on current (Ion), off current (Ioff), threshold voltage ($V_{th}$) are reported in the paper and also RF/Analog parameters like transconductance (gm), output conductance (gd), intrinsic gain (gm/gd) are reported. And also parameters like Electric field (E), Electron density ($n_e$), Electron mobility (μ) which are measured across the device length are simulated. The proposed structure showed performance improvement in all the parameters when the technology node is decreased.**

***Keywords: Technology node, Multi Fin, On current, Off Current, Trans conductance generation factor (TGF)***

## I. INTRODUCTION

Fin shaped Field effect transistor(FinFET) is one of the best alternative to replace a MOSFET, which is encountering the problem of short channel effects(SCE's)[1-3].SCE's like Drain induced barrier lowering, hot carrier degradation, Velocity saturation had a huge impact on drain current of the MOSFET, when the technology node is decreased. In a FinFET, channel is surrounded by gate in the shape of a fin which increases the gate controllability on a channel thus overcoming the major problem caused by SCE's. Finfet thus reducing the SCE's increases the drain current[4].

Many alternative structures like Double gate MOSFET[5-7], Triple gate MOSFET[8], Tunnel FET[9], Gate all around FET's[10] are proposed for reducing SCE's. FinFET comes under the classification of a triple gate device. A FinFET with single tall fin along with $SiO_2$ oxide layer is the first attractive way that was proposed to reduce the SCE's [11]. FinFET can be used for both low power and high-power applications. Research is growing in a faster pace in the area of memory applications like SRAM by using FinFET [12].

FinFET with multiple fins show promising results in terms of power gain when compared to a single tall fin[13]. Using a metal gate gives better performance in terms of current driving capability. As the metal work function increases an improvement in the device performance can be observed [14-15]. High k dielectrics are one best alternative for $SiO_2$ as a gate insulator. As $SiO_2$ after certain extent stop acting as an insulating layer because of tunneling effect. so as a replacement of $SiO_2$, $HfO_2$ is considered as an alternative [16-17]. All the dielectric materials which have k value greater than 10 are considered as high k dielectrics.$HfO_2$ has a dielectric constant value ranging from 20-25. Because of usage of $HfO_2$, gate oxide leakage will be reduced and there will be increase in drain current. The proposed structure is having multiple fins, high k dielectric and also a metal gate so the structure inculcates the advantages of all the three parameters. So, the Multi fin junction FinFET with decreasing technology nodes will have better performance in terms of increased drain current [18].RF/analog parameters like transconductance (gm), output conductance (gd), intrinsic gain (gm/gd), and Electric field(E), Electron density(ne), electron mobility (μ) along the device length in Multifin-FinFET structure are reported through sentaurus 3D TCAD simulator.

The paper is organized as follows. Section II gives the information of the device structure. It gives the brief out of materials used for device construction, range of doping concentrations used for source, drain and channels, and also device dimensions. Section II also give the information of how the graphs are visualized. It also gives the information of basic principle of FinFET, The device On and Off conditions are discussed in this section. Section III is all about resultsand their corresponding discussions. Section IV serves as the conclusion to the paper.

## II. DEVICE STRUCTURE & IT'S DIMENSIONS

In this Paper FinFET is developed on a buried oxide layer[19-20] with 3 fins and considering copper as gate material. For 32nm we used $SiO_2$ as oxide layer. But on reducing the technology node we considered $HfO_2$ as oxide layer as on reducing the technology nodes Short channel effects come into picture so to overcome them insulating layer has been changed from $SiO_2$ to $HfO_2$. In this structure, the $n^+$ source $n^+$ drain regions are doped with concentration of $10^{20}\ cm^{-3}$ and the p-type channel is doped with concentration of $10^{15}\ cm^{-3}$ or both $n^+$ and $p^+$ regions uniform doping is considered.[21]

The simulation of MULTI FIN FinFET for different technology nodes is carried out through Sentaurus TCAD Simulator. In the physics section, for carrier transport drift

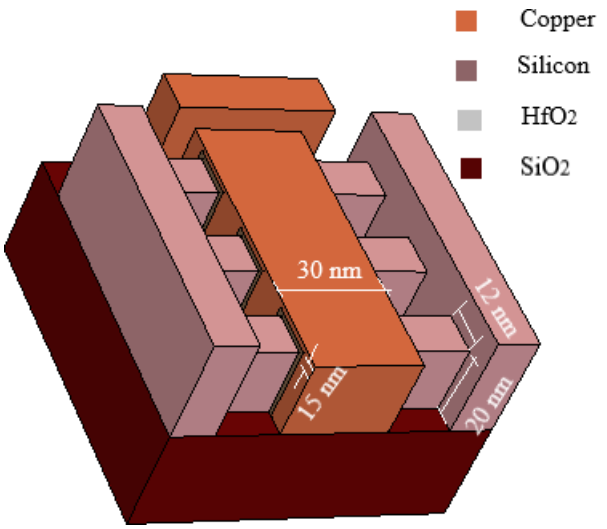


Fig. 1. 3D view of Multi-fin FinFET

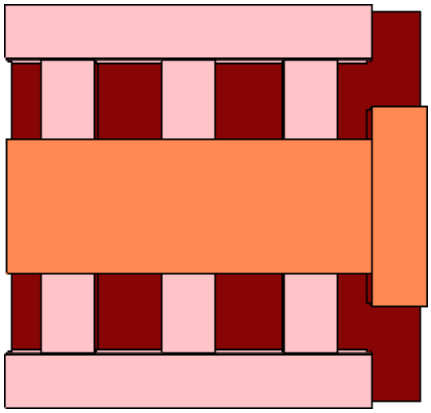

Fig. 2. 2D view of Multi-fin FinFET

diffusion model is considered, as the doping concentration of source and drain is around $10^{20}\ cm^{-3}$ which is high in number Fermi Dirac distribution is activated. Slot boom model is considered for Band Gap Narrowing effect.

Figure 1 shows the 3D view of a Multi fin FinFET and Figure 2 represents the 2D view Of a Multi fin FinFET The various dimensions considered for the Multifin-FinFET structure are: Thickness of fin (TSi) = 12 nm, Length of the gate(L) = 30 nm, Height of fin (Hfin) = 20 nm, Thickness of oxide structure is equal to (tox) = 1.5 nm, and channel length is varied to 32nm,24nm and 10nm.For these three different cases all the RF/Analog parameters were simulated

In this paper technology nodes has been decreased and results were observed. The code for the device is developed in Sentaurus structure editor and the graphs are observed in SVisual. For observing the electrical characteristics PLT file is used and for observing the characteristics like electron mobility, electron density, electric field etc.TDR file is usedin SVisual.

The basic principle for the behavior of Id-Vg simulation curves we observe in the section-3 is explained below When the Applied Gate Voltage is less than Threshold Voltage FINFET operates in cut off region and no channel is formed. As there is no formation of channel there is no movement of electrons and hence no drain current is observed

When gate voltage is increased beyond threshold voltage, channel is formed between source and drain and there will be current flow from source to drain which keeps increasing when there is increase in drain current which is called Linear region. For a FINFET to get into linear region it requires lower gate voltage when compared to the conventional planar devices which results in lower circuit delay, lower leakage and higher performance.

At a Particular Gate Voltage, there will be no increase in the current from source to drain even though there is an increase in the drain current, which is called Saturation region. Equations mentioned below represent the drain current equations for a FINFET in linear region and saturation region respectively.

$$I_{DS} \approx \frac{\mu}{L} Cins \ \ V_{GS} - V_{TH} - \frac{V_{DS}}{2} \ \ V_{DS}$$

$$I_{DS} \approx \frac{\mu}{2} C_{ins} (V_{GS} - V_{TH})^2$$

Above two equations are generally used in long channel FINFET's.

## III. RESULTS & DISCUSSIONS

The impact of change in channel length with a metal (copper) gate on the device structure is demonstrated. The entire device structure is demonstrated at fixed value of Vds (drain to source voltage) is taken as 0.75V

Figures 1 to 8 represent various input-output characteristics of the device and figures 9 to 11 represent behavior of different parameters along the length of the device.

Tabular form I mentioned below gives the information of On-current, Off Current and Thresh hold Voltage obtained for different technology nodes. Table II and Table III are comparison of On-current and Off Current of the proposed device with References

TABLE I
IMPACT OF CHANNEL LENGTH ON ION,IOFF AND VTH

| Channel length | Ion(A) | Ioff(A) | Vth(V) |
|---|---|---|---|
| 32nm | $3.6\times10^{-2}$ | $1.49\times10^{-14}$ | 0.72 |
| 24nm | $5.3\times10^{-2}$ | $7.81\times10^{-15}$ | 0.75 |
| 10nm | $6.6\times10^{-2}$ | $9.01\times10^{-15}$ | 0.8 |

From the tabular form we can clearly observe that On current has increased for 24nm when compared to 32nm by 1.47X and it has increased by 1.24X for 10nm when compared to 24nm and there is a decrease in off current when technology node is decreased from 32nm to 10nm.As there is a increase in on current and decrease in off current there will be a subsequent increase in drain current for 10nm when compared to 32 nm

The effect of decrease in channel length on transfer characteristics of Multifin-FinFET in linear scale is shown in Fig 3.Increase in On current when the technology node is decreased is observed. Increase of threshold voltage when there is decrease in technology node is observed[24-25]

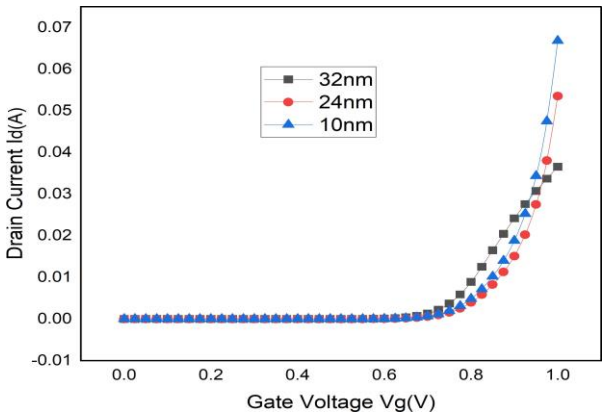


Fig. 3. Gate Voltage vs Drain Current

From figure 3 it is clear that there is an improvement of 47% in drain current from 32 nm to 24 nm and also there is also an improvement of 23% from 24nm to 10nm in drain current.

Trans conductance (gm) is used to define the gain of any circuit. Trans conductance is obtained by doing the 1st derivative of Id vs Vgs simulation. The highest value of gm is obtained in inversion region and which can be used for circuit applications [22-23].The trans conductance equation is given below

$$g_m = \frac{\partial I_D}{\partial V_{gs}}$$

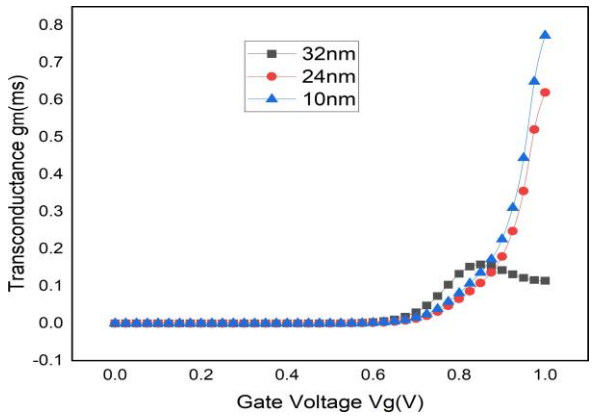


Fig. 4. Gate Voltage vs Trans conductance

Figure 4 mentioned above represents Gate Voltage vs Trans conductance. From Figure 4 it is clear that 10nm is giving better performance when compared to 32 nm. So device with less channel length has better performance

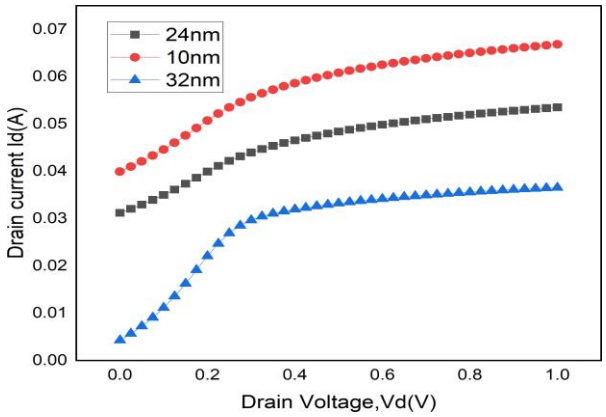


Fig. 5. Drain Voltage vs Drain current

Fig 5 represents drain voltage vs drain current. From results it is clear that 24nm drain current has been improved by 1.3X when compared to 32nm when drain current is measured across drain voltage similarly there is an improvement by 1.62X for 10 nm when compared to 24nm. Vd vs Id simulation helps in finding out the output conductance. Output conductance is obtained by doing the 1st derivative of Vd vs Id graph. Formula for calculating output conductance is given by

$$g_d = \frac{\partial I_D}{\partial V_{ds}}$$

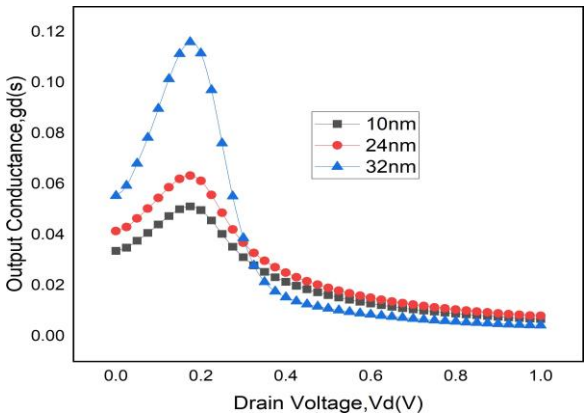


Fig. 6. Drain Voltage vs output conductance

Fig 6 represents drain voltage vs output conductance. Here 10nm exhibits lower output impedance and 32nm represents higher output impedance. For a circuit to perform better especially for amplifier circuits they should have lower output impedance in order to increase the power. So 10nm provides better power as it have lower output impedance.

Figure 7 shown below represents the Gate voltage vs TGF (Transconductance generation factor). Mathematical formula for calculating TGF is given below

$$\text{TGF} = \frac{g^m}{I_d}$$

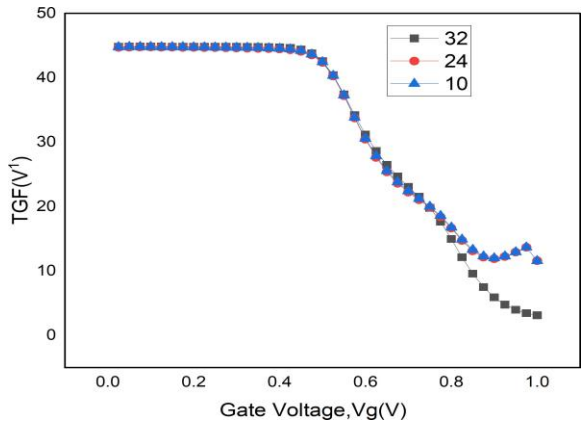


Fig. 7. Gate voltage vs TGF

Transconductance generation factor (TGF) is used for checking the level of translation of trans-conductance for a certain level of drain current. TGF value is maximum at starting of the inversion region. The system with higher valuesof TGF is used for microwave applications

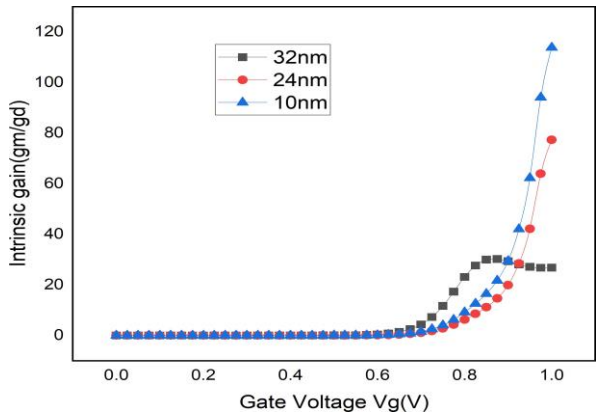


Fig. 8. Gate Voltage vs Intrinsic gain

Figure 8 represents Gate Voltage vs Intrinsic gain. There is an improvement of gain in 10 nm by 4.4X when compared to 32nm. Mathematical Formula for intrinsic gain is mentioned below

$$\text{Intrinsic gain} = \frac{g^m}{g_d}$$

Fig 9 shows the electron density along length of the device. Electron density is observed in source drain and fin regions.

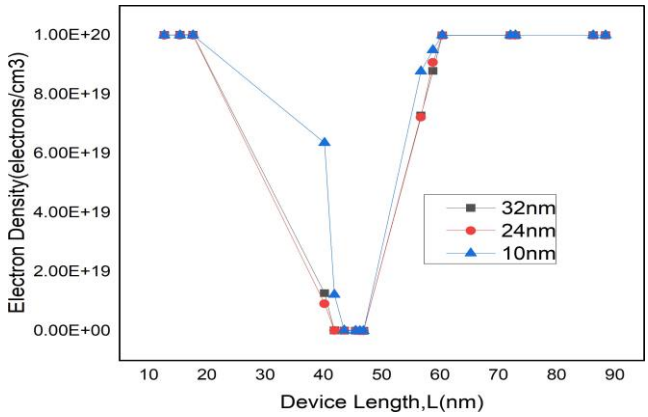


Fig. 9. Length of the device vs Electron density

In source and drain regions electron density is 1e20 as source, drain regions are doped with phosphorus concentration(n-type material) and in fin region it has been decreased as it doped with boron concentration(p-type material). So, the resultant graph is of V-Shape. And the graphs for all the three technology nodes are almost similar.

E-Mobility is higher in the center region as when positive gate voltage is applied all the minority carrier electrons are attracted towards the gate where either side, the mobility of electrons is less. There is an improvement of electron mobility for 10nm when compared to 32nm by a factor of 1.35

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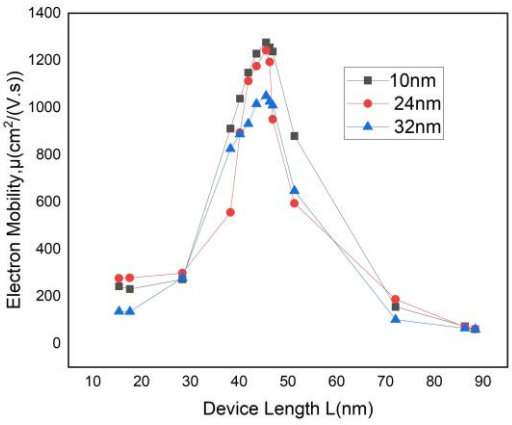


Fig. 10. Length of the device vs Electron Mobility

Figure 11 shows the behavior of electric field along the length of the device. Electric field increases as the distance between source and drain decreases [26]. So as the technology node decreases the electric field increases, from figure it is clear that there is an increase of electric field by 2.6X for 10nm when compared to 32nm

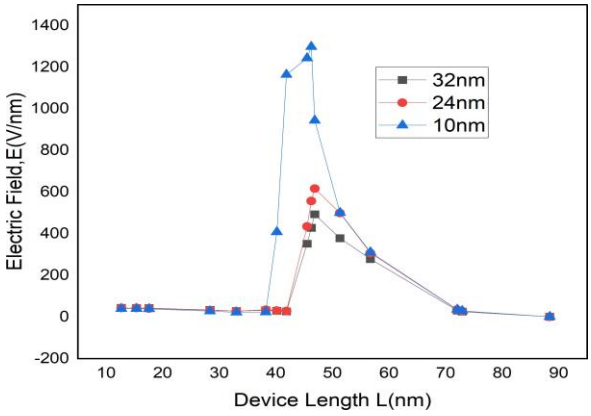


Fig. 11. Length of the device vs Electric field

TABLE II
COMPARISON OF ION, IOFF WITH REFERENCE PAPER 21

| Ion(A) | Ioff(A) | Ref21,Ion(A) | Ref21,Ioff(A) |
|---|---|---|---|
| $3.6\times10^{-2}$ | $1.49\times10^{-14}$ | $8.01\times10^{-4}$ | $1.04\times10^{-8}$ |

TABLE III
COMPARISON OF ION, IOFF WITH REFERENCE PAPER 27

| Ion(A) | Ioff(A) | Ref27,Ion(A) | Ref27,Ioff(A) |
|---|---|---|---|
| $3.6\times10^{-2}$ | $1.49\times10^{-14}$ | $30.6\times10^{-6}$ | $4.6\times10^{-13}$ |

Table II and Table III mentioned above clearly shows that the proposed device of Multi fin Structure shows a very good On current and Off Current when compared to the references

## IV. CONCLUSION

We have reported a statistical simulation study of different electrical parameters for different channel lengths 32nm, 24nm and 10nm through sentaurus TCAD simulator. It is observed that there is a subsequent increase of 47% in On current from 32nm to 24nm and an increase of 24% from 24nm to 10nm respectively. Intrinsic gain of 10nm is increased by 4.4X when compared to 32nm.Electric field is observed to be improved by a factor of 2.6 for 10nm when compared to 32nm.Electron mobility is increased by 1.35X for 10nm when compared to 32nm. Electron density is observed to be same for three technology nodes 32nm, 24nm and 10nm.From the above results it can be concluded that 10nm is exhibiting better performance when compared to 32nm.

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**Ethical Approval and Consent to participate:** "All procedures performed in studies involving human participants were in accordance with the ethical standards of the institutional and/or national research committee and with the 1964 Helsinki declaration and its later amendments or comparable ethical standards.

**Informed Consent** "Informed consent was obtained from all individual participants included in the study."

**Research involving Huan Participants and/ or Animals:** Not Applicable

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