Performance analysis of optical AND gate using T-shaped waveguide

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Abstract **-** Ultra-compact all-optical AND logic gate is realized for optical processing and photonic integrated devices with two-dimensional photonic crystal waveguides based on beam interference principle. The performance of the structure is examined and evaluated by optimized parameters such as refractive index and silicon rod radius. The results obtained from a numerical calculation using the finite-difference time-domain (FDTD) method and plane wave expansion method. The photonic crystal based all-optical AND logic gate has benefits of compact size as 38.88 μm^2, operated at low power levels, high transmission ratio and good time response as 0.124 ps. Associated with conventional semiconductor optical amplifiers, Mach-Zehnder interferometer and photonic crystal ring resonators proposed methodology provides better performance with a high achieved more than 97% transmission ratio, at a wavelength of 1.55 µm.

Keywords: all-optical AND gate; photonic crystals; beam-interference; transmission ratio; response time.

1. INTRODUCTION

Photonic crystals (PhCs) have a periodic micro or nanostructures in optical nature, which have a photonic bandgap (PBG) similar way of energy bandgap in conventional electronic devices to control and confinement of light flow [1]. The PhCs have properties such as low power dissipation, smaller in size and operates at a low power level. These assistances of PhCs can be achieved by creating the defects into waveguide [2-3]. Due to these properties' researchers have widely implement all-optical logic gates using PhCs.

In recent all-optical logic gates are realized using PhCs such as SOA [4-7], Mach-Zehnder interferometer (MZI) [8-11], plasmonic waveguides [12-14], single-mode interference [15-17], multi-mode interference (MMI) [18-19], photonic crystal ring resonator

(PCRR) [20-21] and photonic crystal waveguides (PhCWs) [22-26]. Devices implemented with some of the prior technologies have limitations such as, due to carrier's recovery time in SOA-based devices circuit response time is decreases hence, speed of the device is decreased [4-5]. Devices based on MZI technologies have a problem of complex integration [8-11], optical ring resonator-based devices were operated with low input signal power, but performance of these circuits is slow [20-21]. Prior designs of all-optical AND logic gate implemented with PCRR and PhCWs have a problem of complex structures and have less contrast ratio (CR). In this work to overcome the earlier problems, optical AND gate is realized by PhCWs having small size, high CR and high transmission ratio (TR).

The multiple interferences inside PhC waveguides form photonic bandgap, which is the same as the semiconductor bandgap. The propagation of electromagnetic waves in an arbitrary medium is defined by eigenvalues using Maxwell's equation given below,

$$\nabla \times \frac{1}{\varepsilon(\vec{r})} \nabla \times \vec{H}(\vec{r}) = \frac{\omega^2}{C^2} \vec{H}(\vec{r})$$

Where $\varepsilon(\vec{r})$ is the space-dependent dielectric function, C is the speed of light in vacuum, and $\vec{H}(\vec{r})$ is the optical magnetic field vector of a definite frequency ω.

This paper is ordered as follows: Design and working principle of an all-optical AND logic gate are given in Section 2. Section 3 describes simulation results and performance analysis. Finally, a conclusion is presented in Section 4.

2. STRUCTURAL DESIGN OF ALL-OPTICAL AND LOGIC GATE

The all-optical AND logic gate is used as sampling gate in optical sampling oscilloscope because it have ultrafast operation as compared to electrical components [2]. In this work all-optical AND gate has been implemented using 2-D square lattice PhCs waveguides with an array of 12 silicon rods in X direction and 9 silicon rods in Z direction. The structure contains three junction silicon rods with the radius, r_{j1} = 0.3a, r_{j2} = 0.35a and r_{j3} = 0.07a respectively and two reflecting rods having radius r_e = 0.2a. The structure implemented with lattice constant of 'a' is 0.6μm and refractive index (RI) is 3.46. Junction rods r_{j1} , r_{j2} and two reflecting rods r_e provides fewer back reflections into input ports and, r_{j3} is chosen to avoid the unwanted less intensity light signals to outport. Figure. 1 indicates the design of an all-optical AND logic gate with two T- shaped waveguides. This structure is designed by using OptiFDTD tool OptiWave software.

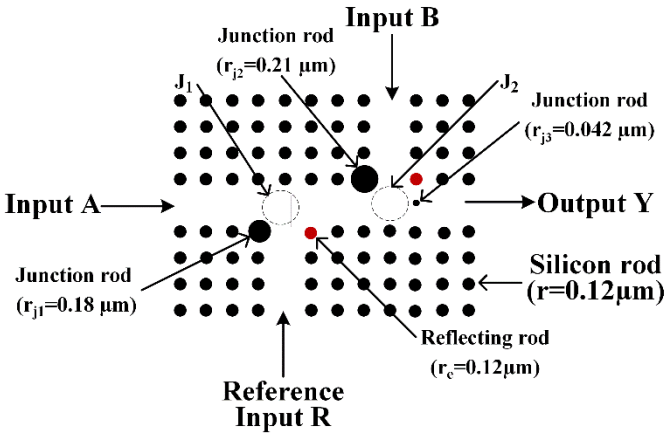

Fig 1. Diagram of all-optical AND logic gate with two T-shaped photonic crystals

A proposed all-optical AND logic gate works on the principle of beam-interference. Depends upon relative phase angle or path length of input light signal either constructive or destructive interference has occurred. The phase difference of 2nπ (where n = 0, 1, 2, 3, …) or even integer multiples path difference produces constructive interference and Phase difference of (2n + 1) π or odd integer multiples path difference produces destructive interference.

Table 1 represents the input signals from port A, B, and R with initial phase and describes the resultant interference takes place at junction J_1 and J_2.

Table 1: Resultant interference at junctions J_1 and J_2 based on phase of input light beams

Input logic			Input phase			Path traverse		Path difference	Phase difference	Type of Interference
A	B	R	A	B	R					
0	0	1	-	-	0^0	At J_1	R=4a	-		-
0	1	1	-	0^0	0^0	At J_2	R=8a B=4a	4a	0^0	Destructive (due to r_{j3} = 0.07a)
1	0	1	180^0	-	0^0	At J_1	R=4a A=4a	0	180^0	Destructive
1	1	1	0^0	180^0	0^0	At J_1	R=4a A=4a	0	0^0	Constructive
						At J_2	R=8a B=4a	4a	180^0	Constructive (due to r_{j3} = 0.07a)

3. SIMULATION RESULTS & DISCUSSIONS

The finite-difference time-domain (FDTD) method is used to calculate the propagation of light inside waveguides numerically by discretizing fields into space and time with governing Maxwell's equations. Time step is estimated by Courant limit along the X-and Z-directions are Δx and Δz, respectively

$$\Delta t <= 1/\left(c\sqrt{1/\Delta x^2 + 1/\Delta z^2}\right)$$

where 'c' is the speed of light in vacuum. Simulation results are as follows:

Case 1: Port A is '0' and Port B is '0'

In this case, the absence of a light signal at port A and B indicated as logic '0' and signal incident at port R with the relative phase of 0^0 is represented as logic '1'. The incident reference signal from port R would reach output port Y with very little power due to the usage of reflecting and junction rods. Figure 2 depicts no optical signal that has appeared at output port Y, which is indicated as a logic '0'.

Case 2: Port A is '0' and Port B is '1'

Absence of signal at port A is representing logic '0' and presence of a signal at port B and R represented as logic '1' with an initial phase of 0^0. The path travelled by the signals from port B to J_2 is 4a and from port R to J_2 is 8a. Destructive interference takes place at junction J_2 due junction rod r_{j3}. Therefore, at output port Y, no light has appeared as shown in Fig. 3.

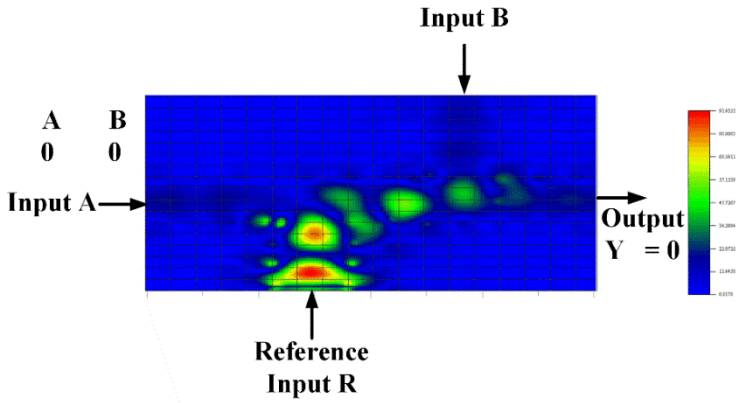

Fig 2. Light propagation for input condition A and B is '0'

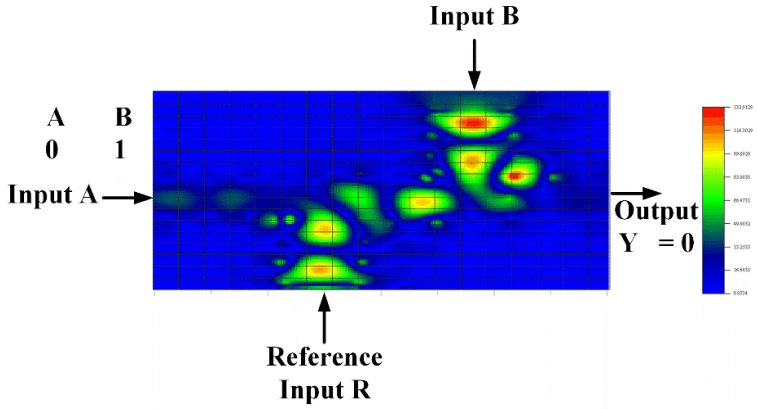

Fig 3. Light propagation for input condition A is '0' and B is '1'

Case 3: Port A is '1' and Port B is '0'

Signal incident at ports A and R are representing logic '1' with a relative phase angle of 180^0, 0^0 respectively and no light signal is incident at port B representing logic '0'. The

path covered by the signals from port A to J_1 is 4a and from port R to J_1 is 4a. The path and phase difference between these two signals is 0 and 180^0, therefore destructive interference has occurred at junction J_1. Hence, no light signal has appeared across output port Y as shown in Fig. 4.

Case 4: Port A is '1' and Port B is '0'

Presence of light signal at port A, B, and R, are representing logic '1' with a phase angle of 0^0, 180^0 and 0^0 correspondingly. Signals from port A and R are reached junction J_1 with path length 4a, hence at junction J_1 both signals have constructively interfered. The resultant signal is propagated to junction J_2 with path length 4a and path traversed by a signal from port R to junction J_2 is 4a. Constructive interference is taking place at junction J_2 due junction rod r_{j3} and resultant high-intensity light signal propagated to output port Y as shown in Fig. 5.

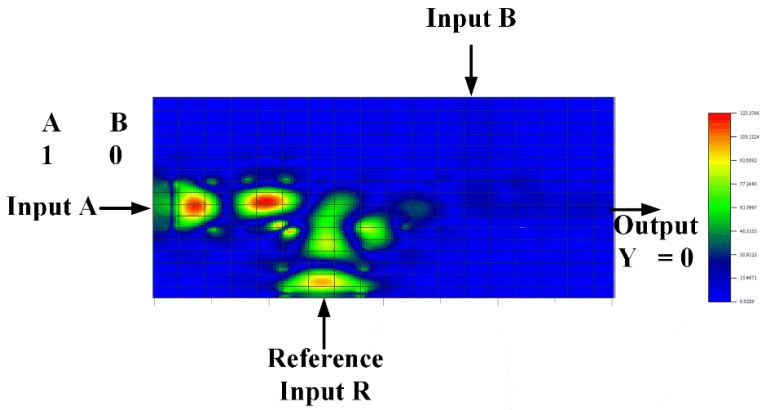

Fig 4. Light propagation for input condition A is '1' and B is '0'

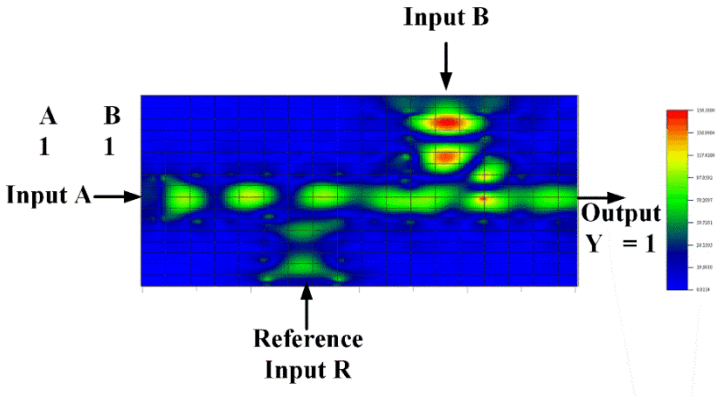

Fig 5. Light propagation for input condition A = 1 and B = 1

Table 2 represents the optical power levels of AND logic gate across output port Y with all input conditions for different values of RI. The values of RI are varied from 3.4 to 3.6 while keeping all other design parameters constant and the output powers are observed for each case.

Table 2. All-optical AND logic gate for different RI values with normalized input and output power values

Input		Output Power			
		Refractive Index Variations			
A	B	3.42	3.44	3.46	3.48
0	0	0.02	0.042	0.024	0.032
0	1	0.14	0.12	0.088	0.03

1	0	0.010	0.017	0.012	0.021
1	1	0.75	0.75	0.731	0.671

Table 3. All-optical AND logic gate for different silicon rod radius values with normalized input and output power values while optimized RI of 3.42

Input		Output Power			
		Silicon rod radius values			
A	B	0.16a	0.18a	0.2a	0.22a
0	0	0.08	0.05	0.02	0.04
0	1	0.18	0.21	0.14	0.16
1	0	0.017	0.015	0.010	0.02
1	1	0.7	0.72	0.75	0.65

Table 3 represents output power levels of the all-optical AND logic gate with various silicon rod radius values, for all input conditions with normalized input and output power values; while optimizing RI value with 3.42.

The refractive index of the proposed structure is optimized by varying the RI value from 3.4 to 3.48 but RI of 3.4 not satisfied the functionality of optical AND gate. However, RI of 3.42 to 3.48 are perfectly works as AND gate, out of which 3.42 provides the best output power levels. According to obtained values which are depicted in Table 2, CR is calculated and variations of CR for different RI values are indicated in Figure 6.

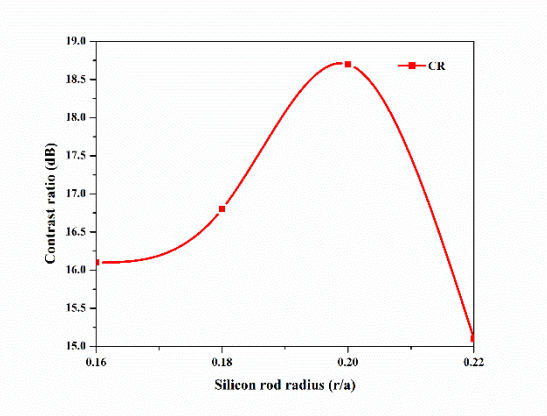

Fig 6. Contrast ratio of all-optical AND logic gate for different (a) refractive index

However, radius of the silicon rod is also optimized by verifying the functionality of AND gate for various radius values. The radius of silicon rod varied from 0.16a to 0.22a and resultant values are indicated in Table3. The CR is calculated and variations of CR for various radius values are depicted in figure 7. From the figures 6 and 7, it is observed that the optimized value for RI and silicon rod radius is 3.42 and 0.2a respectively. The ON-OFF logic level CR is specified with the below equation,

$$CR = 10 \log_{10} (P_1/ P_0) \qquad (1)$$

In equation 1, P_1 and P_0 are represented optic field levels of logic ‘1’ and ‘0’ respectively.

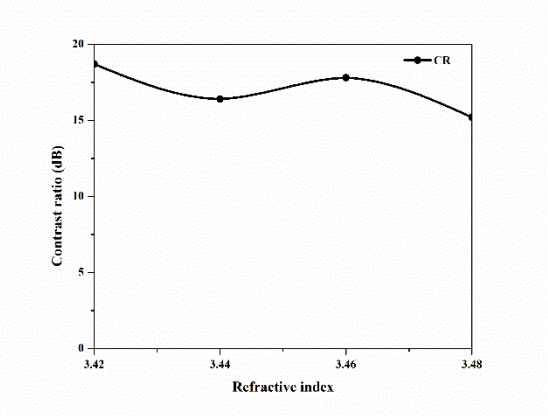

Fig 7. Contrast ratio of all-optical AND logic gate for different (a) silicon rod radius

The response time curve is determined to analyse the performance of proposed design as similar to Refs. [22,23 & 27]. Fig. 8 determines the response time of the proposed AND gate for the input condition '11'. Time required for the output power to climb 0-90% of average output power P_{av} in the final steady state is ct = 37.4 μm or 0.124 ps. The response time is the combination of transmission delay time t_1 = 0.06 ps and time to reach the 0.1 to 90% of the average output power t_2 = 0.064 ps. Due to usage of nonlinear material fall time is considered as approximately equal to rise time. Therefore, a narrow pulse was produced at the output port as a width of $2t_2$ = 0.128 ps. Response time of the design is the sum of ON and OFF period of pulse signal is 0.256 ps and proposed design operated at a bit rate of 1.18 Tbps.

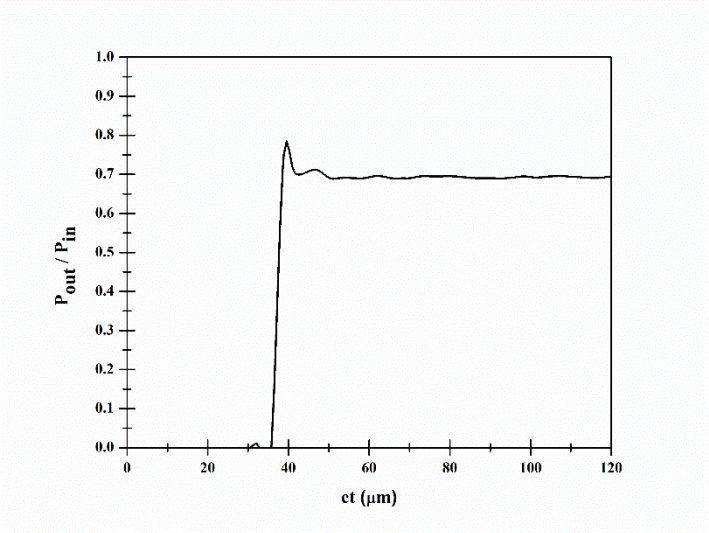

Fig 8. Time response curve of the output power for input condition '11'

The performance of the structure has been analysed by calculating the CR and transmission ratio (TR). The TR is defined as

$$TR = \frac{P_Y}{P_A + P_B + P_R} \times 100\%$$

where, P_Y is optical power at output port *Y*, $P_A + P_B + P_R$ is the total input power

The proposed design is compared with exciting designs in terms of different parameters such as size, CR, TR response time, rise and fall times as depicted in Table 7. As per the mentioned parameters in Table 7 prior design suffer from less CR and occupies high footprint [16,22], the design of AND gate not mentioned about rise and fall times [23] and design of all-optical AND gate has less transmission ratio and occupies more area [26]. As compared with earlier designs the proposed structure occupies less area, provides high TR, high CR, and response time is low.

Table 4. Comparison of proposed design with earlier designs in terms of various parameters

Dimensions	Contrast ratio	Transmission ratio	Response time	Ref
9.45×13.5 μm^2	6.7 dB	-	-	16
9×9 μm^2	6.017 dB	-	0.63 ps	22
8.64 × 5.64 μm^2	19.46 dB	-	0.15 ps	23
8.1×12.5 μm^2	-	92%	-	26
7.2× 5.4 μm^2	18.7 dB	97%	0.124 ps	Proposed

4. CONCLUSION

In this work, structure of the all-optical AND logic gate is realized using 2-D PhC waveguide with square lattice silicon rods in the background of air. The performance of the structure is analysed by optimizing the parameters such as refractive index and silicon rod radius. In this structure, reflecting rods and junction rod is used to propagate the light into essential output by reducing unnecessary back reflections. This design exhibits a maximum CR of 18.7dB and more than 97% of TR at 1.55 μm wavelength. The proposed AND logic gate is compact in size, operates at low power levels and power consumption is also less. Therefore, this structure plays an important role in realizing optical devices for computer networks, signal processing and communication systems.

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REFERENCES

[1] Watcharakitchakorn. O., Silapunt, R.D.: Design and Modeling of the Photonic Crystal Waveguide Structure for Heat-Assisted Magnetic Recording. Adv. Mat. Sci and Eng. 1-11, 2018.

[2] Yabu, T., Geshiro, M., Kitamura, T., Nishida, K., Sawa, S.: All-optical logic gates containing a two-mode nonlinear waveguide. IEEE J. Quant. Electron. 38(1), 37–46, 2002.

[3] Johnson, S.G., Villeneuve, P.R., Fan, S., Joannopoulos, J.D.: Linear waveguides in photonic-crystal slabs. Phy. Review B. 62, 8212–8222, 2000.

[4] Zhang, X., Wang, Y., Sun, J., Liu, D., Huang, D.: All-optical AND gate at 10 Gbit/s based cascaded single-port-couple SOAs. Opt. Exp. 12, 361–366, 2004.

[5] Ma, S., Chen, Z., Sun, H., Dutta, N.K.: High speed all optical logic gates based on quantum dot semiconductor optical amplifiers. Opt. Exp. 18, 6417–6422, 2010.

[6] Soto, H., Diaz, C. A., Zopomondzo, J., Erasme, D., Schares, L., Guekos, G.: All-optical AND gate implementation using cross-polarization modulation in a semiconductor optical amplifier, IEEE, Photon.Tech. Lett. 14, 498–500, 2002.

[7] Kumar, S., Singh, l., Chen, N.: Design of All-Optical Universal Gates Using Plasmonics Mach-Zehnder Interferometer for WDM Applications. Plasmonics. 13, 1277-1286, 2017.
[8] Choudhary, K., Kumar, S.: Design of an Optical OR Gate using Mach-Zehnder Interferometers. J. Opt. Commun. 39, 1-5, 2016.
[9] Mostafa, T.S., Mohammed, N.A., Rabaie, E.E.: Ultra-High bit rate all-optical AND/OR logic gates based on photonic crystal with multi-wavelength simultaneous operation. J. Modern Opt. 66, 1-12, 2019.
[10] Kumar, S., Singh, G., Bisht, A., Sharma, S., Amphawan, A.: Proposed new approach to the design of universal logic gates using the electro-optic effect in Mach–Zehnder interferometers. Appl. Opt. 54, 8479-8484, 2015.
[11] Zaghloul, Y.A., Zaghloul, A.R.M. Complete all-optical processing polarization-based binary logic gates and optical processors. Opt. Exp. 14, 9879-9895, 2006.
[12] Abdulnabi, S.H., Abbas, M.N.: All-optical logic gates based on nanoring insulator–metal–insulator plasmonic waveguides at optical communications band. J. Nano. Photon. 13(1), 1-19, 2019.
[13] Dolatabady, A., Granpayeh, N.: All Optical Logic Gates Based on Two Dimensional Plasmonic Waveguides with Nano disk Resonators. J. Opt. Soc. Korea. 16, 432-442, 2012.
[14] Zahra, M., Najmeh, N., Farzin, E.: High contrast all-optical logic gates based on 2D nonlinear photonic crystal. Opt.Commun. 355, 130–136, 2015.
[15] Zhu, Z.H., Ye, W.M., Ji, J.R., Yuan, X.D. Zen, C.: High-contrast light-by-light switching and AND gate based on non-linear photonic crystals. Opt. Exp. 14, 1783–1788, 2006.
[16] Ishizaka, Y., Kawaguchi, V., Saitoh, K. Koshiba, M.: Design of ultra-compact all-optical XOR and AND logic gates with low power consumption. Opt. Commun. 284, 3528–3533, 2011.
[17] Sahu, P.: All-optical switch using optically controlled two mode interference couplers. Appl. Opt. 51, 2601-2605, 2012.
[18] Enaul haq, S., Nakkeeran, R.: Multi-mode interference-based photonic crystal logic gates with simple structure and improved contrast ratio. Photo. Netw. Commun. vol 34, pp. 140-148, 2017.
[19] Chunrong, T., Dou, X., Lin, Y., Yin, H., Wu, B. Zhao, Q.: Design of all-optical logic gates avoiding external phase shifters in a two-dimensional photonic crystal based on multi-mode interference for BPSK signals. Opt. Commun. 316, 49–55, 2014.
[20] Swaranakar, S., Rathi, S., Sharma, S.: Design of all optical XOR gate based on Photonic Crystal ring resonator. J. Opt. Commun. 1-9, 2017.
[21] Ashkan, P., Mahdi, Z., Hamed, A.: All-optical AND/OR/NOT logic gates based on photonic crystal ring resonators. Opt. Exp. 9, 578-584, 2016.
[22] Rani, P., Yogita, K., Sinha, R.K.: Realization of AND gate in Y-shaped photonic crystal waveguide. Opt. Commun. 227–231, 2013.
[23] Enaul haq, S., Nakkeeran, R.: Design of photonic crystal based all-optical AND gate using T-shaped waveguide. J. Modern Opt. 63, 941–949, 2015.
[24] Swaranakar, S., Kumar, S., Sharma, S.: Design of XOR/AND gate using 2-D Photonic Crystal principle. Proc. of SPIE. 10130, 1-11, 2017.
[25] Rao, D.G.S., Swaranakar, S., Kumar, S.: Performance analysis of all-optical NAND, NOR and XNOR logic gates using photonic crystal waveguide for optical computing applications. Opt. Eng. 59 (5), 057101 1-11, 2020.
[26] Rekha, M., Kajal, B.: Design and Simulation of 2-D Photonic Crystal Based All-Optical AND Logic Gate. IEEE CICN. 973-977, 2014.
[27] Chic, J. W., Chung, P. L., Zhengbiao, O.: Opmact and low power optical logic NOT gate based on photonic crystal waveguides without optical amplifiers and nonlinear materials. Appl. Opt. 51, 680-685, 2012.