RESEARCH

A Reconfigurable Analog Back-End for CubeSat Communications

José L. Alvarez-Flores^{1*}, Jorge Flores-Troncoso², Remberto Sandoval-Arechiga², Joel A. Castillo², Jorge Simón³, Manuel Hernandez-Calviño² and Leonel Soriano-Equigua¹

*Correspondence:

alvarez_jose@uicol.mx

¹University of Colima, México,
333 University Ave., Colima, Mx

Full list of author information is
available at the end of the article

Abstract

Current small satellite platforms such as CubeSats, require robust and versatile communication subsystems that allow the reconfiguration of the critical operation parameters such as carrier frequency, transmission power, bandwidth, or filter roll-off factor. In this paper, a reconfigurable Analog Back-End for CubeSat communications is proposed. This prototype is implemented using CAD software, on a 6-layer PCB of 10 cm² to implement a transceiver that operates from 0.070 to 6 GHz and complying with CubeSat and IPC-2221 standards. An Software-Defined Radio approach implemented on a baseband processor is used for control purposes. Measurements showed that the signal power at the output of the proposed analog back-end is suitable to feed the subsequent antenna subsystem.

Keywords: Radiofrequency; analog back-end; field-programmable gate arrays; CubeSat; transceiver.

1 INTRODUCTION

Applying the new electronic communication technologies to spatial missions either for remote observation or surface exploration of the earth or other astronomical bodies, promises the improvement of sustainability, robustness, and truthfulness of the current missions when sharing spatial resources [1]. This new paradigm requires the use of diverse technologies to achieve a flexible reconfiguration capability of the communication systems between heterogeneous satellites.

The trend in electronic design is governed by Moore's Law which establishes capacities of the General Purpose Processors (GPP's), Digital Signal Processors (DSP's), and Field Programmable Gate Arrays (FPGA's) [2]. As a result of this, the processing flow of radio signals traditionally made with blocks of specialized hardware- could be defined and controlled by software, known as Software-Defined Radio (SDR). The embedded SDR technique used on a System on a Chip (SoC) turns out to be suitable to implement a flexible, adaptable and reconfigurable satellite communication systems and eliminates the need to implement hardware for each application. Also, this technique allows reducing development time, costs, and system mass.

Several examples of embedded SDR on a SoC for satellite applications are found in the literature. For example, in [3] a system based on a commercial BladeRFx115[®] is explained, this works with an LMS6002D Integrated Circuit (IC) from 0.30 to 3.8 GHz with a programmable bandwidth from 1.5 to 28 MHz. This one is controlled

with a Raspberry Pi 2[®] which is integrated in an embedded GNU-Radio way; all this with the purpose to integrate a launchable network based on Commercial-Off-The-Shelf (COTS) components and for emulating a network of federated satellites. This challenging implementation interconnects several external subsystems that use a SoC for improving performance, costs, and volume. In [4] an SDR architecture is proposed in which the FPGA and SoC (FMCOMMS3 from Analog Devices[®]) are combined with a programmable radio frequency (RF) transceiver to solve the reconfiguration challenges of transmitter and the receiver. It involves the use and implementation of COTS such as the FMCOMMS3(using AD9361 IC for RF stage) and a ZYNQ 7020 from Xilinx[®] among other devices. In [5], Tian et al. designed and implemented an AD9361 based platform for software radio exclusively for the receiver stage and a ZC706 applied to the digital baseband processing module of SoC.

There are other implementations based on similar architecture (using COTS like FMCOMMS3) as the one presented on [6], where SDR is applied to the ground segment and develops the Digital Down Converter (DDC) stage using the hardware descriptive language VHDL, in addition to some other baseband processes such as channel coding, and data interleaver, among others. The disadvantage of that proposal is that the IP-Cores involved are Xilinx[®] intellectual property and the transmission rates achieved are relatively low, 1.2 to 19.2 Kbps. Finally, it should be mentioned that there are companies in the market that offer satellite communications subsystems based on SDR, like the one commercialized by [7], which can be reconfigured to use different frequency bands such as L, S or K. Nevertheless, it has the drawbacks both of being expensive and proprietary architecture.

The authors in [8] concluded that hardware reuse is a novel approach in the implementation of SDR systems, which results in better performance of communications schemes. In [9], a design of an RF front-end for a nanosatellite is presented, using low-cost commercial components like the CC2510 IC, for both the reception and transmission stages. This IC works in a narrow bandwidth of 2.400 to 2.483 GHz.

In [10], a communication system was implemented in a Zynq 7020 as part of the baseband processor (BBP), however, the RF stage was simulated.

As pointed, there are several applications based on digital implementations for SDR systems proposed in the literature and others offered as COTS components. However, the RF analog back end remains partially unexplored and represents an opportunity area for research.

This document describes the design, implementation, and testing of a low-cost reconfigurable prototype of the communications subsystem, called the Reconfigurable Analog Back-End (RABE), for the space segment that meets the CubeSat standard. The proposed RABE consists of two stages; The first performs baseband processing, control, and reconfiguration for the second stage, and is implemented in a commercial SoC architecture. The RF stage (second stage), in which this work is focused, is based on the design, implementation, and testing, the protocol for this work which includes digital/analog conversion, mixer, and filters based on COTS, which operates from 0.070 to 6 GHz.

The rest of the paper is organized as follows: in Section II the RABE system architecture, the design and development of the PCB for RF stage, the testbed design, and the software tools used are described; in Section III implementation and testing are shown; in Section IV the main results obtained are presented and discussed; and in Section V, the conclusions are exhibited.

2 METHODS AND EXPERIMENTAL SETUPS

A. System Architecture

The RABE design features two interfaces, the first one is a digital I/O data, control, and communication interface between the prototype and the SoC, which is controlled by an FPGA, and which is part of the BBP; the connection interface with the RF stage is achieved through an FMC connector; the second one is an RF analog output with SMA connector as the interface to the RF filtering stages, power amplifier, and antenna. The main core of the RABE is powered by an AD9354 IC.

Fig. 1 shows the communication model, which was implemented, the RF stage (this work) was designed, implemented, tested, and tuning for the RABE in yellow, which was the contribution of the paper.

The BBP stage consisted in the development and coupling of the Serial Communication Protocol (SPI), as well as the programming of the registers to control the flow of data, synchronization, and processing of the data from the BBP to the RABE through the FMC connector, which is responsible for carrying all the bits for the operation of both devices, including the voltage and ground lines.

In the RF stage, the SPI was synchronized to program all the necessary registers in the IC, the DACs, the filtering stage, the preamplifiers, and the local oscillator, that were configured to be tuned at the required frequency, it is noteworthy that each of the configured actions corresponds to the programming of registers groups in order to obtain the correct result shown in yellow in Fig. 2.

B. RF stage design

During the design stage of the RABE subsystem prototype, the necessary requirements for the development of the PCB (Printed Circuit Board) were specified to guarantee correct operation, allowing interoperability between the subsystem devices. The requirements are detailed in Table 1.

In general, the design of the RABE features two interfaces, the first one is the digital I/O data, control, and synchronization interfaces between the prototype and the SoC; the second one is the analog RF output with an SMA connector.

The RABE has a read/write registers interface carry out via the Serial SPI. Therefore, one of the preliminary task to do was to implement the SPI port in the BBP, since it is not a native protocol in the FPGA.

The data lines for the PCB of the RF stage are divided into two sets: the differential and single-ended lines as shown in Fig.3 . The maximum data transfer frequency achieved is 245.76 and 61.44 MHz for the differential bus and single-ended respectively. However, it depends on the IP-Core processing speed of the SoC and FPGA

used by the implementation. The RF output feeds the next stage (it is not the scope of the work) comprised of power amplifiers, filters, and antennas, in order to achieve a high signal-to-noise ratio (SNR) and considering a link range of 2000 km in the free-space Low Earth Orbit(LEO) satellite.

RF stage of the RABE prototype uses the AD9364 transceiver, internally composed of ADC converters, DACs, filters, GPOs, PLLs, and an SPI communication control port [11], as illustrated in Fig.4.

In this work, the transmission, data entry, DAC, filters, and SPI serial communication stages are used. The radio transmitter is implemented with the ability to operate in various frequency bands, mainly S-band. In addition to this, the configuration to modify in the application of the IC data such as the transmission power, the filtering, and, most importantly, that the prototype design must comply with the size proposed for the CubeSat standard. The IC AD9364 from Analog Devices[®] [11] is configured as an RF transceiver, operating in the 0.070 to 6.000 GHz frequency range with the ability to tune the bandwidths (BW) from 0.2 to 56.0 MHz and allowing applications proposed by the manufacturer such as point-to-point communication systems, base stations (BS) for femto/pico/microcells and general-purpose radio systems.

Further, the AD9364 IC is set by reading/writing into the registers set described in [12]. According to the manufacturer, the IC has a list of almost 1,014 (0x3F6) 8-bit registers with configuration capabilities intended for diverse applications. These IC-specific application steps are initialization, configuration, transmission, reception, and analog records in reception (see Table 2). Record data flow modes can be: read, write, or both. The SPI port of the AD9364 operates at a recommended maximum speed of 50 MHz, according to the manufacturer's specifications [11]. However, a frequency of 8 MHz was used for testing purposes in this work to ensure a safe transfer of information to registers.

Regarding the operating and configuration modes of the registers, there are a relatively large number of reserved and/or empty positions, so, in order not to cause improper operation of the system, it is advisable not to refer to them.

To reduce transients while changing the transmission frequency setting on the device, the power to the couplers on the transmission lines is directly connected to a 1.3V voltage source. The capacitors shown in Fig. 5 are intended for removing noise and transients at the transmitter output.

It is worth mentioning that all the designs, measurements, and tests for the resulting devices were carried out in a test laboratory with a controlled environment (temperature, voltage levels, electromagnetic noise, electric shocks, among others) in such a way that the results obtained are completely similar to those obtained by simulations tools.

Design rules concerning the CubeSat standard [13] and PCB design [14] were applied to the electronic design process. The final result was a 6-layer PCB, of 10 cm x 10 cm (see Fig. 6), on the other hand, the manufacturer suggests a fixing or

soldering area on the PCB with the intention of achieving high performance and achieving adequate operation of the IC [12]. In Table 3, the thickness of the 6 PCB layers is shown.

The PCB for the radio transmitter was designed using Altium®, a high-end PCB design software package. The simulation of signal behavior on the PCB was carried out using Keysight® EMPro® and Genesys® tools. The purpose of the simulation was both to validate low levels of electromagnetic interference (EMI) between interconnecting tracks and to avoid radiation to other components included in the board before PCB fabrication.

C. Testbed design

The testbed showed in Fig. 7 was integrated to measure the transmission power and frequency values, also to check the operation of the RABE prototype. The hardware devices and software used for the testbed implementation are: Keysight® N9030A Signal Analyzer, personal desktop computer, Digilent/Xilinx® brand Zedboard test card, RF cables with SMA connector, ethernet cable, RABE prototype, control and programming software for AD9364 IIO Oscilloscope, and IP address monitoring software.

The steps for running the testbed are as follows:

- Step 1. Download and install the IIO Oscilloscope software on your PC.
- Step 2. Insert the ABE-R into the Zedboard through the FMC connector.
- Step 3. Connect the RF cable from the RABE SMA connector to the N9030A.
- Step 4. Connect the ethernet and USB cable between the PC and the Zedboard.
- Step 5. Run the IIO Oscilloscope software on your PC.
- Step 6. Use the IIO Oscilloscope to configure the transmission frequency, bandwidth, attenuation, and other parameters.
- Step 7. Configure the N9030A to perform a scan on parameters value close to those set in the previous step.
- Step 8. Save the data to the N9030A.

3 RESULTS AND DISCUSSION

Using the configuration described in section 3.C, the testbed was implemented to test the RABE prototype, obtaining similar results to those from the IC manufacturer's test card AD9364 [11].

Two types of experimental measurements were carried out in order to verify the proper operation of the implemented prototype. In both scenarios, the same settings were used for output power, transmission frequency, and bandwidth parameters. As a result, it was noted that RABE output power (Fig. 8 (a)) was reduced by 2 dB compared to FMCOMMS4 (Fig. 8 (b)), which was 7 dB. It is important to mention that according to the AD9364 datasheet, it is able to transmit with a maximum power of 7.5 dBm when matched to 50 Ohms load at 2.4 GHz.

According to Nyquist's bandwidth equation, the maximum transmission rate equals two times bandwidth (BW) symbols per second. If each symbol can carry

M different distinguishable levels, then each pulse carries $\log M$ bits of information, which is described by

$$C = 2BW \log_2(M) \text{ bps} \quad (1)$$

Since the bandwidth of the AD9364 ranges from 200 KHz to 56 MHz, the data rate capacity for quaternary modulation, $M=4$, will be between 0.800 and 224 Mbps.

In Fig. 9, the graph of the data collected in the test bench shows the spectrum transmitted by a signal with a carrier frequency of 2.6095 GHz to verify the correct operation of the design. The output power available at the carrier frequency was -20 dBm, as shown. A Gaussian 3 dB resolution bandwidth (RBW) filter was applied into the signal analyzer followed by a Fast Fourier Transform (FFT) with a BW of 411.9 kHz.

The BBP was set in a QAM modulation scheme at the testbed (as shown in fig. 10). The resulted modulation process was controlled and synchronized by the BBP to the RABE stage via the FMC connector.

Total harmonic distortion (THD) percentage was measured as described in [15] and is given by

$$THD_n = \sqrt{\frac{\sum_{n=2}^{\infty} P_{o_n}}{P_{o_1}}} \times 100, \quad (2)$$

where: P_{o_n} is the output power of the n -th harmonic in watts and P_{o_1} is the output power of the fundamental frequency in watts.

According to measurements made in the Lab using the N9030A Signal Analyzer, for $n = 10$ harmonics, as shown in Table 4, it was found that

$$THD_n = 3.81\% .$$

The distortion values due to the harmonics generated by the transmitter stage could reach values of up to 3.8%, reducing the output power of the RF signal as shown in Table 4.

Communication systems with a low THD produce less interference between electronic devices connected to or close to the PCB.

In fig. 11, the spectrum generated by the RABE is shown, which was taken directly from the RF output by the N9030A analyzer, all this at a frequency centered at 2,300 GHz, in which it is allowed by the Mexican government for experimental satellite links according to the frequency allocation table.

Although the tests performed on the RABE were in a very small notch of the RF spectrum, the resulting device transmits from 0.070 to 6,000 GHz.

On the other hand, it is worth mentioning that the development of the PCB was taking into account the CubeSat standard, with the idea of a possible inclusion as a payload in a satellite platform and carrying out transmission tests from space.

CONCLUSIONS

In this paper, the design, construction, verification, and test of a prototype for a reconfigurable radio-transmitter called RABE were presented. The proposed prototype can be used as the communication subsystem in a nanosatellite based on the CubeSat standard. Construction and testing were performed under quality standards in a controlled environment. Results show the correct operation of our card similar to that one commercialized by the IC manufacturer.

The resulting implementation of RABE guarantees the reconfiguration of a nanosatellite communication subsystem. Because of this reconfiguration capacity, it is possible to either have a communication with the terrestrial segment or with other devices orbiting in space, as in the BBP stage different processing stages can be selected (e.g. modulation scheme). Similarly, the RF stage parameters can be modified (e.g. carrier frequency or transmitter power).

In short, this design allows reducing the number of unnecessary components, optimizing the dimensions of the PCB, and having a weight and size adequate to the specifications of the CubeSat standard.

It should be noted that power values achieved in the RF output stage of the RABE are sufficient for the subsequent stages of the nanosatellite communications subsystem, which include filters, power amplifiers, and antennas, among others.

However, in the future, it will be necessary to carry out measurements of compatibility and electromagnetic susceptibility to the RABE prototype, in order to identify anomalies like interferences with other devices that make up the satellite. In addition to this, it is recommended to carry out vibration and thermal vacuum tests to verify the robustness of the design when it comes to being placed in orbit. Also, as future work, it is recommendable that both baseband processing, control, and reconfiguration stage, and the RF stage, could be integrated on a single PCB trying to minimize the size of the communication system, and at the same time optimizing the operating speed.

Abbreviations

CAD: Computer-Aided Design

PCB: Printed Circuit Board

GPP: General Purpose Processor

DSP: Digital Signal Processor

FPGA: Field Programmable Gate Array

SDR: Software-Defined Radio

SoC: System on a Chip

IC: Integrated Circuit

GHz: Gigahertz

MHz: Megahertz

COTS: Commercial-Off-The-Shelf **RF:** Radio Frequency

DDC: Digital Down Converter

VHDL: Vhsic Hardware Description Language

BBP: BaseBand Processor

RABE: Reconfigurable Analog Back-End

SMA: SubMiniature version A

FMC: FPGA Mezzanine Card

SPI: Serial Communication Protocol

DAC: Digital-Analog Converter

I/O: Input/Output

SNR: Signal-to-Noise Ratio

LEO: Low Earth Orbit

km: Kilometer

GPO: General-Purpose Output

PLL: Phase-Locked Loop

BS: Base Stations

EMI: ElectroMagnetic Interference

BW: BandWidth

KHz: Kilohertz

RBW: Resolution BandWidth

FFT: Fast Fourier Transform

THD: Total Harmonic Distortion

Competing interests

The authors declare that they have no competing interests.

Author's contributions

All authors have read and approved the manuscript. JLAF has completed the design and manufacture of the prototype, with the accompaniment of JAAA and under the supervision of JFT, JSR, MHC and LSE. JLAF, JFT, RSA, LSE, MHC and JSR made the translation for the present work. JLAF, JFT and JSR participated in the design of this paper.

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Author details

¹University of Colima, México, 333 University Ave., Colima, Mx. ²Autonomous University of Zacatecas, México, 801 Ramon Lopez Velarde, Ave., 98010 Zacatecas, Mx. ³Catedras CONACYT, Autonomous University of Zacatecas, México, 801 Ramon Lopez Velarde Ave., 98010 Zacatecas, Mx.

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Figures

Figure 1: **Communication system model.** A block sequence about the communication system model and its architecture.

Figure 2: **Radio Frequency model.** RF PCB scheme and AD9364 architecture.

Figure 3: **Schematic design of the RABE.** In this figure shown how is get AD9364 connected with FMC connector to the FPGA and RF Output to the power amplifier stage (not shown at this work).

Figure 4: **Block diagram of the IC AD9364.** In this figure, the manufacturer of the AD9364 describes how it is connected internally.

Figure 5: **RF coupling.** The RF coupling stage, designed to avoid interferences for 2-3 GHz.

Figure 6: **RABE Printed Circuit Board.** 3D model of the RABE (top and bottom layers).

Figure 7: **Testbed block diagram.** Configuration for the connection of the testbed for the prototype.

(a) Testbed implemented for ABE-R test. (b) Testbed implemented for FM-COMMS4 test.

Figure 8: Measurements from (a) RABE and FPGA and (b) FMCOMMS4 and FPGA (only COTS) card.

Figure 9: **Spectrum of signal transmitted at 2.6095 GHz.** Further processing of the data shows the spectrum of the carrier signal transmitted at 2.6095 GHz

Figure 10: **Signal analyzer, RABE and Zedboard on QPSK.** The RABE prototype transmitting with 4-tone QPSK modulation, with 1MHz frequency separations.

Figure 11: **Spectrum radiated by RABE at 2.300 GHz.** Image obtained from the signal analyzer with the prototype transmitting a single tone with a frequency of 2.300 GHz.

Tables

Table 1: General requirements of the ABE-R.

Request	Value	Units
Power Suply Vcc	5	volts
PCB size	95x95	mm
Working frequency	2.2 - 2.3	GHz
Input connector	FMC ASP-134604-01	
RF connector	female SMA	
Reference CK	Integrated	
IC	AD9364	
PCB	6 layers	

Table 2: Functions of the AD9364 registers.

Modes	Initial	Final
Initialization	0x000	0x017
Setting	0x018	0x05F
Transmitter Configuration	0x060	0x0D7
Receiver Configuration	0x0F0	0x1FC
Rx Analog Registers	0x230	0x3F6

Table 3: RABE PCB layers.

Layer	Type	Material	thickness (mm)	thickness (mil)
Top	Surface	Air		
	Conductor plane	Copper	0.0514	2.025
L1_PWR	Dielectric	FR-4	0.2032	8
	Conductor plane	Copper	0.0342	1.35
L2_SIG	Dielectric	BT-epoxy	0.1524	6
	Conductor plane	Copper	0.0342	1.35
L3_SIG	Dielectric	FR-4	0.2032	8
	Conductor plane	Copper	0.0342	1.35
L4_PWR	Dielectric	BT-epoxy	0.1524	6
	Conductor plane	Copper	0.0342	1.35
Bottom	Dielectric	FR-4	0.2032	8
	Conductor plane	Copper	0.0514	2.025
	Surface	Air		

Table 4: Total Harmonic Distortion.

Harmonic	Frequency (GHz)	Amplitude (dBm)	Power (watts)
1	2.3	-12.01	$6.30E^{-5}$
2	4.6	-40.4	$9.12E^{-8}$
3	6.9	-72.25	$5.96E^{-11}$
4	9.2	-81.3	$7.41E^{-12}$
5	11.5	-80.9	$8.13E^{-12}$
6	13.8	-79.9	$1.02E^{-11}$
7	16.1	-79.7	$1.07E^{-11}$
8	18.4	-76.9	$2.04E^{-11}$
9	20.7	-75.11	$3.08E^{-11}$
10	23	-74.32	$3.70E^{-11}$

Figure 1 Communication system model.

Figure 2 Radio Frequency model

Figure 3 Schematic design of the RABE

Figure 4 Block diagram of the IC AD9364

Figure 5 RF coupling

RF COUPLING 2-3 GHz

Figure 6 RABE Printed Circuit Board

Figure 7 Testbed block diagram

Figure 8a Testbed implemented for ABE-R test

Figure 8b Testbed implemented for FMCOMMS4 test

Figure 9 Spectrum of signal transmitted at 2.6095 GHz

Figure 10 Signal analyzer, RABE and Zedboard on QPSK

Figure 11 Spectrum radiated by RABE at 2.300 GHz