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Subthreshold Analytical Model of Asymmetric Gate Stack Triple Metal Gate All Around MOSFET (AGSTMGAAFET) for Improved Analog Applications

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Abstract— In this paper, we have proposed a 2D analytical model for Asymmetric gate stack triple metal gate MOSFET(AGSTMGAAFET) and performed a comparative analysis with the simulation results obtained using the SILVACO 3D simulation software. Existing devices such as gate all around single metal (SMGAAFET), gate all around triple metal (TMGAAFET), gate stack single metal (GSSMGAAFET), gate stack triple metal (GSTMGAAFET) and asymmetric gate stack single metal (AGSTMGAAFET) have been compared with our proposed structure AGSTMGAAFET. Our device provides excellent performance in terms of drain current, transconductance, output conductance, current gain, maximum transducer power gain which shows our device's suitability for various analog applications moreover the potential and electric field plots obtained have twostep profile and extremely low electric field near the drain region which ordains our device with the ability to suppress various SCE's like DIBL and hot-carrier effect. The analytical model and simulation results show good convergence in values which validate the correctness of the proposed model.

Keywords— Single Metal Gate All Around (SMGAAFET) MOSFET, Triple Metal Gate All Around (TMGAAFET) MOSFET, Gate Stack Single Metal Gate All Around (GSSMGAAFET) MOSFET, Gate Stack Triple Metal Gate All Around (GSTMGAAFET) MOSFET, Asymmetric Gate Stack Single Metal Gate All Around (AGSSMGAAFET) MOSFET, Asymmetric Gate Stack Triple Metal Gate All Around (AGSTMGAAFET) MOSFET, Short Channel Effects (SCE).

I. INTRODUCTION

In modern day world where there is need for continuous miniaturization of MOSFET used in variety of integrated circuits, device scaling has been one of the prime tools to achieve this goal. However, device scaling is restricted up to a limit mainly due to short channel effects (SCE) [1]. The continued downscaling of CMOS has led to the need for ultra-thin gate dielectrics as well. However, the thinning of oxide layer is limited by direct tunneling which increases the leakage current. Thus, combination of these effects leads to major reliability issues and causes performance degradation over a period of time.

Thus, a number of device structures like Schottky barrier MOSFET (SBCGAA MOSFET), Schottky barrier graded stack MOSFET (SBGS-CGAA MOSFET) and Dual metal Schottky barrier graded stack MOSFET (DMSBGSCGAA) have been proposed earlier to overcome short channel effects. These gate all around MOSFET have greater control over the channel as they surround the substrate from all sides, provide increased packing efficiency and avoid corner effects [2]. However, they suffer from DIBL effects, threshold voltage fluctuations and difficulties in fabrication. In this paper we have proposed a triple material gate FET that helps in overcoming existing DIBL, impact ionization and eliminates oxide breakdown effects to large extent by improved transport efficiency. This when used with gate stack provides high transconductance. For better carrier generation and improved performance, a high-k dielectric material like HfO_2 has been used along with SiO_2 in the proposed structure which reduces leakage current [3]. However, high-k materials result in fringing fields from the source/drain regions which tends to decrease the control of the gate over the channel. Thus, an ultra-thin SiO_2 interlayer between the high-K layer and silicon substrate has been introduced which improves the quality of interface by decreasing trap density and provides stability [2]. To overcome shallow source/drain at junction and for easy fabrication metallic material instead of doped material is used. Hence overall proposed structure consists of asymmetric gate stack and triple material gate which collectively improve drain current characteristics and reduce SCE's by providing better gate control.

Using graphical simulation for the proposed Asymmetric Gate Stack Triple Gate (AGSTMGAAFET) the device showed best performance results in terms of drain current, conductance, intrinsic gain, transconductance, maximum transducer power gain (MTPG), current gain and output conductance (g_d) as compared to Asymmetric gate stack single metal FET(AGSSMGAAFET) ,Gate all around single metal FET (SMGAAFET) ,Gate all around triple metal FET(TMGAAFET), Gate stack single metal FET(GSSMGAAFET) and Gate stack triple metal FET(TMGSAAAFET) which have been proposed earlier to overcome SCE's to a great extent. Section 2 describes the

device structure of the proposed and the models used to simulate the various devices for comparison. Section 3 presents the analytical model of the device. Section 4 displays the comparative analysis of our device against those previously proposed and the comparison is made on the basis of various parameters such as electric field, potential, subthreshold current for different lengths and radius, MTPG, current gain, transconductance, output conductance, I_{DS} vs V_{GS} and I_{DS} vs V_{DS} graphs and also the potential contour plots of all the devices has been studied. In section 5 we provide the conclusion, in section 6 we acknowledge the inputs of all those who have guided us throughout the course of our research and section 7 presents the calculated coefficients of the analytical model.

II. DEVICE STRUCTURE

The three-dimensional view of Asymmetric Gate Stack Triple Metal Triple Metal Gate All Around (AGSTMGA AFET) MOSFET is presented in the figure 1(a). The gate material is composed of three metals each having different work functions. The highest work function metal (4.8 eV) is present at the source end and between the two the metal with work function 4.62 eV is present while the with the least work function metal (4.4 eV) is present at the drain end. Source and drain are doped with a concentration of 10^{19} cm⁻³ (n-type) and the substrate is doped with concentration of 10^{16} cm⁻³ (p-type). The thickness of the silicon substrate is $t_{Si}=10$ nm. Hafnium Oxide (HfO₂) is the gate stack material used in the device ($t_{HfO_2}=2$ nm, $\epsilon_{r,HfO_2}=22\epsilon_0$). Two methods namely Newton & Gummel are used for solving using ATLAS-3D.

The decreasing gradient of work functions from source towards the drain helps in reducing the value of electric field at the drain end thereby regulating it throughout the channel. Due to this, electron overshooting is prevented which is basically the hot-carrier effect (another type of SCE).

The 2-D cross-sectional view of AGSTMGA AFET is shown in figure 1(b). This topology divides the device into 4 regions. First region consisting of the gate material M₁ (first). Second region consisting of half of gate material M₂ (second), with SiO₂ as the layer between HfO₂ and the substrate. Third region consisting of the other half of gate material M₂ (second), with HfO₂ as the layer between HfO₂ and the substrate and fourth region consisting of the gate material M₃ (third).

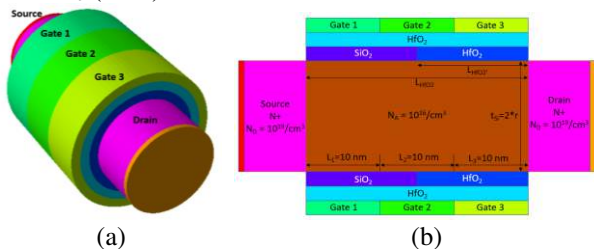


Fig 1.(a) 3-D Structural View of Asymmetric Gate Stack Triple Metal Gate All Around MOSFET (b) 2-D Cross sectional View of Asymmetric Gate Stack Triple Metal Gate All Around MOSFET

The list of various parameters used for all the single metal and all the triple metal device structures are tabulated in table 1 and 2 respectively. The list and description of

models used for the simulation of the device using ATLAS-3D are tabulated in table 3 [4].

TABLE 1. Single Metal Devices Structural parameters

Parameters	SMGAA MOSFET	GSSMGAA MOSFET	AGSSMGAA MOSFET
L (nm)	30	30	30
N _A (cm ⁻³)	1 x 10 ¹⁶	1 x 10 ¹⁶	1 x 10 ¹⁶
N _D (cm ⁻³)	1 x 10 ¹⁹	1 x 10 ¹⁹	1 x 10 ¹⁹
t _{ox} (nm)	2	2	2
t _{hfo2} (nm)	-	2	2
L _{hfo2'} (nm)	-	-	15
t _{Si} (nm)	20	20	20
φ _m (eV)	4.8	4.8	4.8
L _{S/D} (nm)	10	10	10

TABLE 2. Triple Metal Devices Structural parameters

Parameters	TMGAA MOSFET	GSTMGA MOSFET	AGSTMGA MOSFET
L (nm)	30	30	30
N _A (cm ⁻³)	1 x 10 ¹⁶	1 x 10 ¹⁶	1 x 10 ¹⁶
N _D (cm ⁻³)	1 x 10 ¹⁹	1 x 10 ¹⁹	1 x 10 ¹⁹
t _{ox} (nm)	2	2	2
t _{hfo2} (nm)	-	2	2
L _{hfo2'} (nm)	-	-	15
t _{Si} (nm)	20	20	20
φ _{m1} (eV)	4.8	4.8	4.8
φ _{m2} (eV)	4.62	4.62	4.62
φ _{m3} (eV)	4.4	4.4	4.4
L _{S/D} (nm)	10	10	10

TABLE 3. List of Models used

S. No.	Model Used	Description
1.	SRH	Shockley-Read-Hall which is a generation and recombination model is used with fixed lifetimes.
2.	CONMOB	Concentration dependent mobility model is used which basically is a doping-mobility table (valid at 300K).
3.	FLDMOB	This specifies the transverse field degradation for electrons. Standard saturation models are used for both electrons and holes (specified from the values of EVSATMOD and HVSATMOD which indicates which parallel field dependent mobility model to be used).
4.	BOLTZMANN	Boltzmann is the carrier statistics model which is used for preventing impact ionization and overshooting.

III. ANALYTICAL MODEL

The Asymmetric gate stack triple metal exhibits a symmetry which is cylindrical in nature therefore to take advantage of this it is a good choice to resort to the use of cylindrical coordinates instead of cartesian coordinates because it greatly simplifies the solution procedure that is the solution is gotten using the 2D Poisson's equation rather than 3D Poisson's equation this luxury is afforded to us as a result of the fact that the potential and electric field distribution in our device do not depend on the variation of the azimuthal angle. The 2D Poisson's equation for a AGSTMGA MOSFET is given by-

$$\frac{1}{r} \frac{\partial}{\partial r} \left(r \frac{\partial \Phi_i(r, z)}{\partial r} \right) + \frac{\partial^2 \Phi_i(r, z)}{\partial z^2} = \frac{q N_A}{\epsilon_{si}} \quad (1)$$

$$0 \leq r \leq \frac{r_{si}}{2} \text{ and } L_{i-1} \leq z \leq L_i \text{ where } i=1,2,3,4$$

Here 'r' represents the channel radius and 'z' represents the axis along which we measure the length of the channel and $\Phi_i(r, z)$ represents the potential as a function of r and z.

The form of the solution is as shown below where the use of boundary condition gives us the required coefficients by using the parabolic approximation method.

$$\phi(r, z) = a_0 + a_1 r + a_2 r^2 \quad (2)$$

Where a_0, a_1, a_2 represent the coefficients which are a function of 'z'. The calculation of these coefficients is done using the following boundary conditions: -

1. The electric field vanishes along the axis of symmetry

$$\frac{\partial \Phi_i(r, z)}{\partial r} \Big|_{r=0} = 0 \quad (3)$$

2. The electric field should be invariant crossing over from the dielectric to the silicon body

$$\frac{\partial \Phi_i(r, z)}{\partial r} \Big|_{r=\frac{r_{si}}{2}} = \frac{\epsilon_j (\phi_{gsi} - \phi_{si})}{\epsilon_{si} t_k} \quad (4)$$

Where $\phi_{gsi} = V_{gs} - V_{fbi}$, $\phi_{si} = \Phi_i(r, z)|_{r=0}$ and $i=1,2,3,4$, $j=1,2, k=1,2$

$$\epsilon_1 = \epsilon_{ox} \text{ for } i = 1,2 \text{ and } \epsilon_2 = \epsilon_{hf} \text{ for } i = 3,4$$

$$t_1 = R \ln(1 + \frac{t_{oxeff1}}{R}) \text{ and } t_2 = R \ln(1 + \frac{t_{oxeff2}}{R}), R = \frac{r_{si}}{2} \quad (5)$$

$$t_{oxeff1} := t_{ox} + \frac{\epsilon_{ox}}{\epsilon_{hf}} \cdot t_{hf}, t_{oxeff2} := t_{ox} + t_{hf} \quad (6)$$

3. The potential should not vary as we move from a region under one metal to another having different work functions.

$$\Phi_i(r, L_i) = \Phi_i(r, L_{i+1}), i=1,2,3 \quad (5)$$

4. The electric field should not vary as we move from a region under one metal to another having different work functions.

$$\frac{\partial \Phi_i(r, z)}{\partial z} \Big|_{z=L_i} = \frac{\partial \Phi_i(r, z)}{\partial z} \Big|_{z=L_{i+1}}, i=1,2,3 \quad (6)$$

5. Potential measured at the source should be V_{bi}

$$\Phi_1(r, 0) = V_{bi} \quad (7)$$

Where $V_{bi} = V_T \ln(\frac{N_A N_D}{n_i^2})$, $V_T = \frac{kT}{q}$

6. Potential measured at the drain should be $V_{bi} + V_{DS}$

$$\Phi_4(r, L_4) = V_{bi} + V_{DS} \quad (8)$$

We apply the first two boundary conditions and rearrange the equation to solve for the surface potential.

$$\frac{\partial^2 \phi_{s_1}(z)}{\partial z^2} - K_1^2 \phi_{s_1}(z) = Y_1, 0 \leq z \leq L_1 \quad (9)$$

$$\frac{\partial^2 \phi_{s_2}(z)}{\partial z^2} - K_1^2 \phi_{s_2}(z) = Y_2, L_1 \leq z \leq L_2 \quad (10)$$

$$\frac{\partial^2 \phi_{s_3}(z)}{\partial z^2} - K_2^2 \phi_{s_3}(z) = Y_3, L_2 \leq z \leq L_3 \quad (11)$$

$$\frac{\partial^2 \phi_{s_4}(z)}{\partial z^2} - K_2^2 \phi_{s_4}(z) = Y_4, L_3 \leq z \leq L_4 \quad (12)$$

Where,

$$K_1 := \left(\frac{2 \cdot \epsilon_{ox}}{R^2 \cdot \epsilon_{Si} \cdot \ln\left(1 + \frac{t_{oxeff1}}{R}\right)} \right)^{0.5} \quad K_2 := \left(\frac{2 \cdot \epsilon_{hf}}{R^2 \cdot \epsilon_{Si} \cdot \ln\left(1 + \frac{t_{oxeff2}}{R}\right)} \right)^{0.5}$$

$$Y_1 := \frac{q \cdot N_A}{\epsilon_{Si}} - K_1^2 \cdot (V_{gs} - V_{FB1}) \quad Y_2 := \frac{q \cdot N_A}{\epsilon_{Si}} - K_1^2 \cdot (V_{gs} - V_{FB2})$$

$$Y_3 := \frac{q \cdot N_A}{\epsilon_{Si}} - K_2^2 \cdot (V_{gs} - V_{FB3}) \quad Y_4 := \frac{q \cdot N_A}{\epsilon_{Si}} - K_2^2 \cdot (V_{gs} - V_{FB4})$$

$$V_{Fbi} = \phi_{Mi} - \phi_{si}, i = 1,2,3$$

Here ϕ_{Mi} represents the work function of the gate material and ϕ_{si} represents the work function of the silicon substrate.

$$\phi_{si} = \chi_{si} + \frac{E_g}{2q} + \phi_f, \text{ where } \phi_f = V_T \ln\left(\frac{N_A}{n_i}\right)$$

The solution for this equation is obtained in two parts that is in terms of the forced and natural solutions.

$$\phi_S(z) := \begin{cases} A_1 \cdot e^{K_1 \cdot z} + B_1 \cdot e^{-K_1 \cdot z} - \frac{Y_1}{K_1^2} & \text{if } 0 \leq z \leq L_1 \\ A_2 \cdot e^{K_1 \cdot z} + B_2 \cdot e^{-K_1 \cdot z} - \frac{Y_2}{K_1^2} & \text{if } L_1 \leq z \leq L_2 \\ A_3 \cdot e^{K_2 \cdot z} + B_3 \cdot e^{-K_2 \cdot z} - \frac{Y_3}{K_2^2} & \text{if } L_2 \leq z \leq L_3 \\ A_4 \cdot e^{K_2 \cdot z} + B_4 \cdot e^{-K_2 \cdot z} - \frac{Y_4}{K_2^2} & \text{if } L_3 \leq z \leq L_4 \end{cases} \quad (13)$$

To obtain the necessary coefficients we employ the boundary condition discussed above. The coefficients are presented in the appendix at the end. The electric field which is the negative gradient of the potential is obtained simply by taking the first derivative of the potential.

$$EF(z) = -\frac{\partial \phi_i(r, z)}{\partial z} \quad (14)$$

$$EF(z) := \begin{cases} K_1 \cdot A_1 \cdot e^{K_1 \cdot z} - K_1 \cdot B_1 \cdot e^{-K_1 \cdot z} & \text{if } 0 \leq z \leq L_1 \\ K_1 \cdot A_2 \cdot e^{K_1 \cdot z} - K_1 \cdot B_2 \cdot e^{-K_1 \cdot z} & \text{if } L_1 \leq z \leq L_2 \\ K_2 \cdot A_3 \cdot e^{K_2 \cdot z} - K_2 \cdot B_3 \cdot e^{-K_2 \cdot z} & \text{if } L_2 \leq z \leq L_3 \\ K_2 \cdot A_4 \cdot e^{K_2 \cdot z} - K_2 \cdot B_4 \cdot e^{-K_2 \cdot z} & \text{if } L_3 \leq z \leq L_4 \end{cases} \quad (15)$$

The subthreshold current can be calculated using the formula [5].

$$I_{sub} := 2 \cdot R \cdot \pi \cdot \mu \cdot k \cdot T \cdot \eta_1 \cdot \left(\frac{-q \cdot \frac{V_{ds}}{k \cdot T}}{1 - e^{\frac{-q \cdot V_{ds}}{k \cdot T}}} \right) \int_0^{L_1+L_2+L_3+L_4} \frac{1}{e^{\frac{\phi_i(r, z)}{k \cdot T}}} dz \quad (16)$$

Where $k=1.38 \times 10^{23}$ J/K represents the boltzmann's constant, T represents temperature and $\mu = 1300 \text{ cm}^2/V_s$ represents the electron mobility.

And the corresponding sub threshold slope is given by [5].

$$SS = \frac{1}{\frac{d \log I_{sub}}{dV_{gs}}} \quad (17)$$

IV. RESULTS AND DISCUSSION

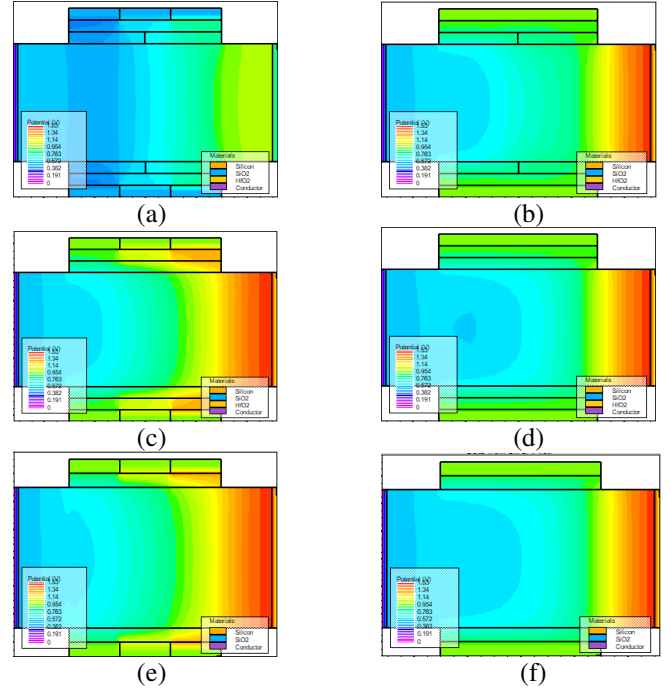


Figure 2: Contour potential plots for the various devices under study where (a) AGSTMGA AFET (b) AGSGSMGA AFET (c) GSTMGA AFET (d) GSSMGA AFET (e) TMGA AFET (f) SMGA AFET

Potential is an important parameter for understanding device physics as it explains the different FET's behavior under the same biasing condition as potential would instigate the charge distribution across the channel. On this charge distribution across the channel, complete device characteristics are dependent. We can clearly observe from the contour plots in Fig 2. that the increase in potential in triple metal FET's is much more as compared to the single metal FET's this basically leads to a reduction in short channel effects like hot carrier effect and impact ionization. Also, the use of asymmetric gate stack with high dielectric leads to a large capacitance and greater control over the channel. This in turn increases the electric field throughout the channel and also reduces any possibility of gate tunneling.

Figure 3 gives us an idea of the dependence of potential on position in the channel for all the devices under study. We are analyzing devices with a single and triple gate material; the latter case leads us to observe two steps in the potential moving from source to drain, this ordains our device with the ability to overcome DIBL to a great extent also this leads to an improvement in the efficiency of carrier transport and also the carrier speed leading to improved drain current [2]. This can be attributed to the change in work function moving from source to drain. Another point of interest is that devices with gate stack exhibit relatively lower potential which can be attributed to the use of triple metal gate with different work function [5].

Figure 4 analyses the dependence of electric field on the position the channel. Electric field is the first order derivative of potential. This graph exemplifies the benefit of

using an asymmetric gate stack which as shown leads to lower electric field values. In nano-scale device architectures reduction of SCE's is of paramount importance and tis lower electric field especially visible at the drain end goes a long way in achieving that [2].

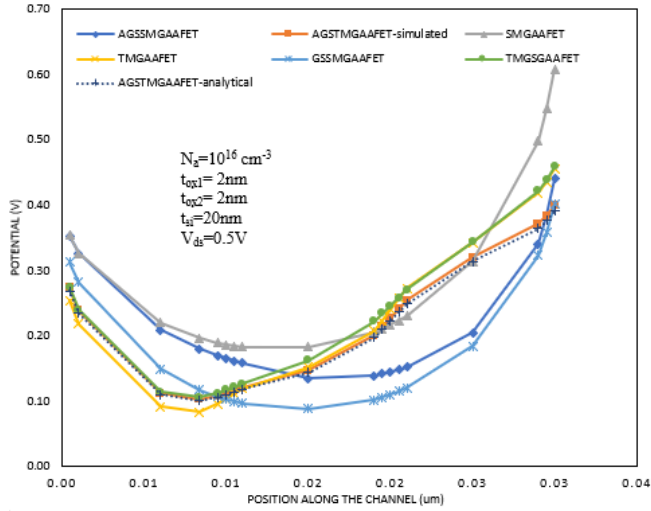


Figure 3: Surface Potential for all 6 models and analytical model for AGSTMGAFAET

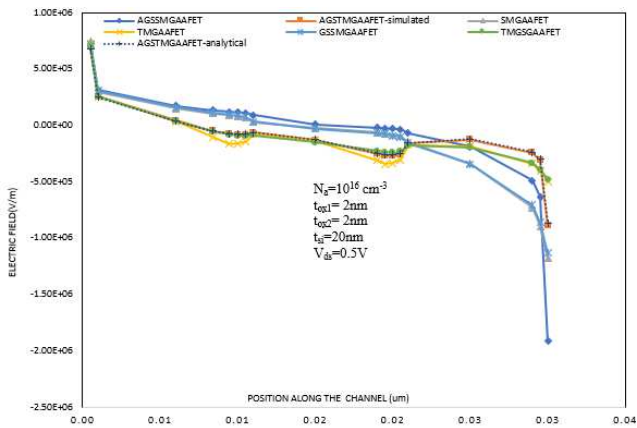


Figure 4: Electric Field for all 6 models and analytical model for AGSTMGAFAET

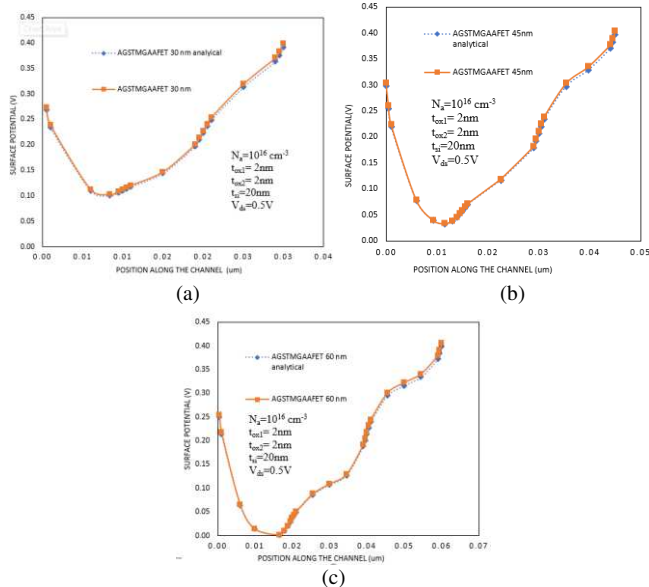


Figure 5: Surface Potential vs Channel Length for AGSTMGAFAET
(a) L = 30 nm (b) L = 45 nm (c) L = 60 nm

Figure 5 gives us the distribution of surface potential as a function of channel length ,now the first thing to observe here is the fact that the potential has a minima which progressively decreases as we increase the channel length this can be attributed to the decrease in charge control linear region which leads to the entire potential to slide in the direction of source [5].The analytical results are much in co-ordinance with the simulated results.

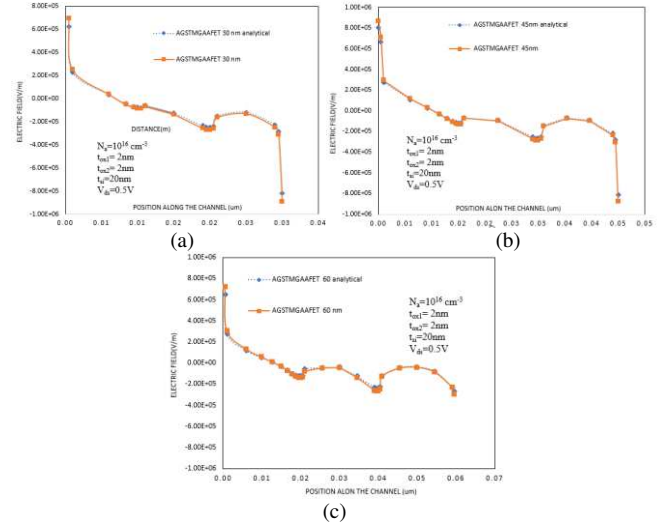


Figure 6: Electric Field vs Channel Length for AGSTMGAFAET
(a) L = 30 nm (b) L = 45 nm (c) L = 60 nm

Figure 6 presents the electric field distribution at the surface as a function of position in the channel for three values of channel length (L=30 nm,45nm,60nm). The triple metal asymmetric gate stack MOSFET gives us a twostep profile for the electric field where the steps occur at the interface of two gate metals [6]. This is extremely beneficial because it leads to the electric field being averaged out throughout the length of the channel moreover, we observe a marked reduction in electric field near the drain, both of these help in reducing SCEs [2].

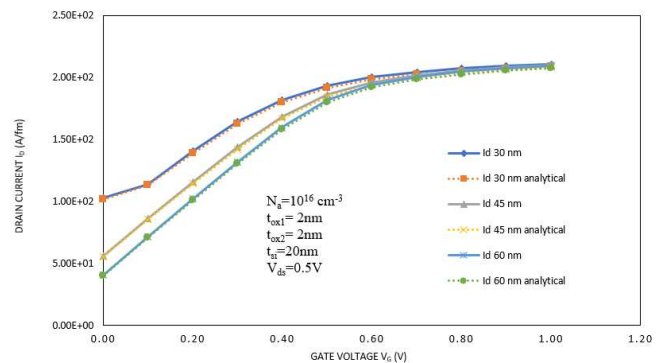


Figure 7: Subthreshold current (I_D) vs gate voltage (V_{GS}) for AGSTMGAFAET for L = 30, 45 and 60 nm

Figure 7 gives the graphical relationship between subthreshold current and the applied gate input voltage. Now the thing to observe here is that as we decrease the length of the channel correspondingly the value of subthreshold current increases leading to increased power consumption and other related SCEs [5].

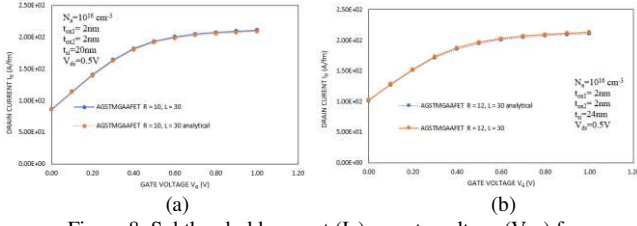


Figure 8: Subthreshold current (I_D) vs gate voltage (V_{GS}) for AGSTMGA AFET with $L = 30$ nm and different radius (a) $R = 10$ nm (b) $R = 12$ nm

In figure 8, we have shown a comparison between source to drain and gate input voltage for different radii of the channel region and for a particular channel length(30nm). The observation to make here is that smaller the channel radius greater the subthreshold slope leading to lower off current and hence lower power dissipation [7].

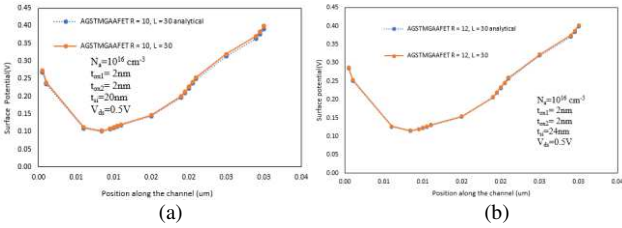


Figure 9: Surface Potential for AGSTMGA AFET with $L = 30$ nm and different radius (a) $R = 10$ nm (b) $R = 12$ nm

In figure 9, we show the variation of surface potential with different values of channel radii. The observation to be made here is that as the length of the channel goes up the position of potential minima also rises up as a result of the fact that controllability of the gate over the channel goes down with increasing channel thickness, this causes V_T to decrease as we increase channel radius so a smaller channel radius is desirable to keep off current in check [8].

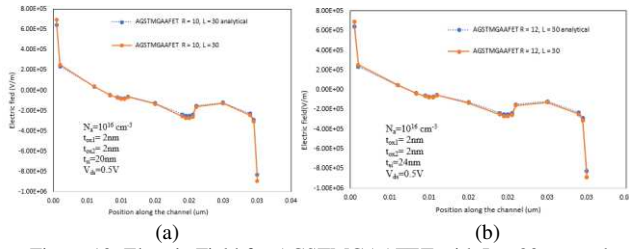


Figure 10: Electric Field for AGSTMGA AFET with $L = 30$ nm and different radius (a) $R = 10$ nm (b) $R = 12$ nm

In figure 10, the clear decline in electric field near the drain region because of the high - k dielectric (HfO_2) and triple metal gate this gives us the benefit of reduced hot-carrier effect and therefore additional reduction in power dissipation [9].

Figure 11 shows the variation in the drain current (I_{DS}) with the gate voltage (V_{GS}) for SMGA AFET, TMGA AFET, GSSMGA AFET, GSTMGA AFET, AGSSMGA AFET and AGSTMGA AFET MOSFET devices. It can be seen that the AGSTMGA AFET generates the highest drain current. Because of the amorphous nature, HfO_2 has high kinetic stability. This ensures less leakages in the corresponding MOSFET [10]. Also, in its presence the concentration of electrons increases in the channel because of higher

capacitance which then results in higher I_{DS} [11]. The strength of the fringing electric fields also increases thereby increasing I_{DS} [12]. Gate stack devices give higher current than non-gate stack devices because of their presence of high dielectric (HfO_2) graded channel. Triple metal devices give higher current than single metal devices as they reduce the overshooting of the electrons. The general order of drain current is asymmetric gate stack greater than gate stack greater than non-gate stack FETs.

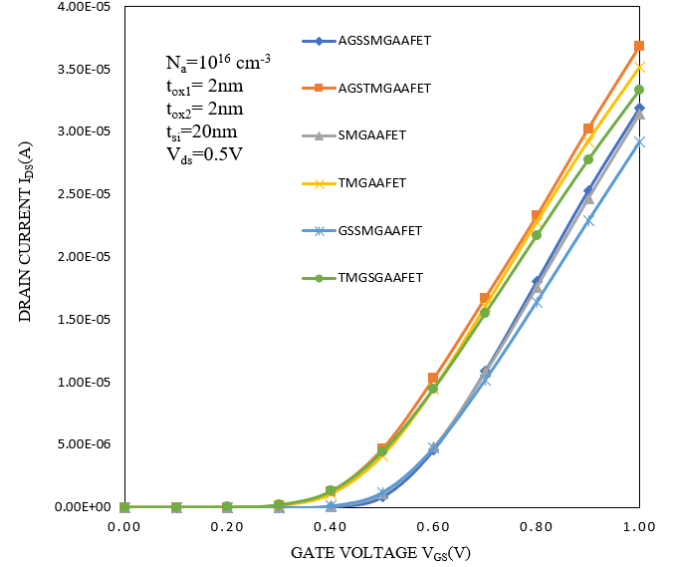


Figure 11: Plot of the change in drain current (I_{DS}) relative to change in gate voltage (V_{GS})

Figure 12 shows the variation in the transconductance (g_m) with the gate voltage (V_{gs}) for SMGA AFET, TMGA AFET, GSSMGA AFET, GSTMGA AFET, AGSSMGA AFET and AGSTMGA AFET devices. Transconductance is calculated by derivation of drain current relative to the gate voltage at constant V_{ds} [13].

$$g_m = \left. \frac{\partial I_{ds}}{\partial V_{gs}} \right|_{V_{ds}}$$

It can be seen that initially the transconductance increases since the device is in linear region and then it tends to decrease when device enters the saturation region. In the presence of triple metal surrounding gates and HfO_2 the carrier mobility increases and the gate control over the channel region becomes more enhanced. This, in turn, increases the drain current and hence increases the transconductance (since g_m is proportional to I_{DS}). As g_m increases, it also implies a higher cut off frequency (f_T) [13].

Figure 13 shows the variation of the current flowing from source to drain with respect to the applied voltage V_{DS} . It can be seen clearly from the figure that our proposed model AGSTMGA AFET gives superior performance in terms of current as compared to all other devices under inspection. Owing to the amorphous nature of HfO_2 which gives us the benefit of high kinetic stability, leakage current is greatly reduced further the asymmetric gate stack provides a much higher drain current owing to its high relative permittivity, also the triple metal gate leads to a large reduction in short channel effects such as hot carrier effect, impact ionization, etc.

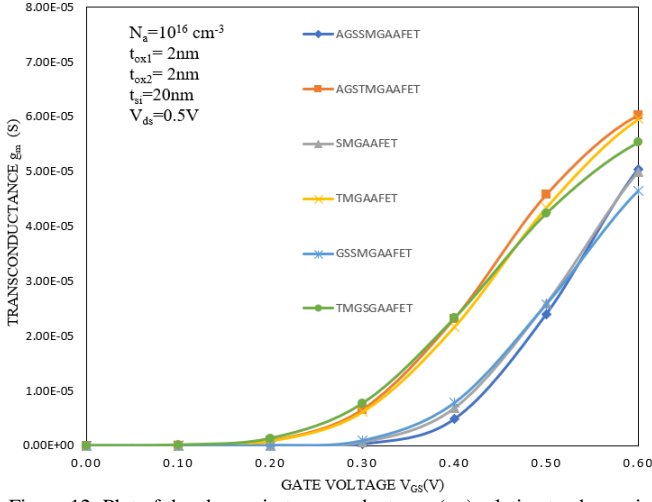


Figure 12: Plot of the change in transconductance (g_m) relative to change in gate voltage (V_{GS})

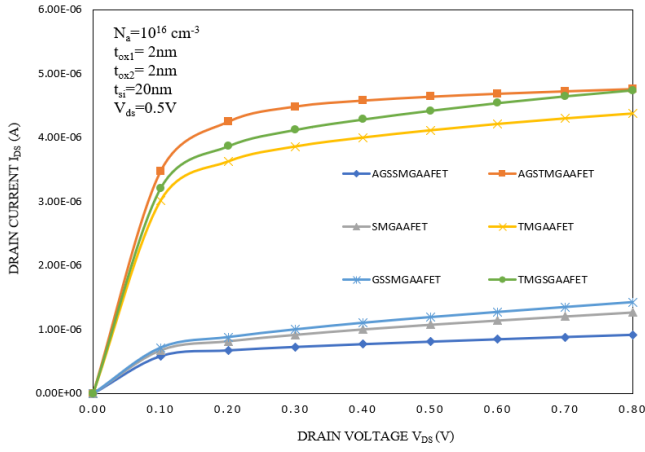


Figure 13: Plot of the change in drain current (I_{DS}) relative to change in drain voltage (V_{DS})

Figure 14 gives the variation of output conductance (g_d) with respect to the drain to source voltage (V_{DS}). The mathematical expression for output conductance is given as [13]:

$$g_d = \left. \frac{\partial I_{DS}}{\partial V_{DS}} \right|_{V_{GS}}$$

It is observed that increased drain current obtained by the AGSTMGA AFET because of the excellent control over the channel which is provided by the asymmetric gate stack. The high relative permittivity of HfO_2 increases the capacitance of the device which in turn enhances the drain current and subsequently g_d as well.

Figure 15 clearly gives us the idea that the current gain offered by the proposed device AGSTMGA AFET is superior to the other devices under study, this result can be attributed to the fact that our device simply provides excellent performance in terms of drain current. The use of high-K dielectric (HfO_2) increases the gate capacitance, this in turn enhances the electric field as a by-product of which electron velocity increases leading to better current gain. Moreover, the decreasing work function of the gate material as we move from the source to the drain reduces unwanted SCE's.

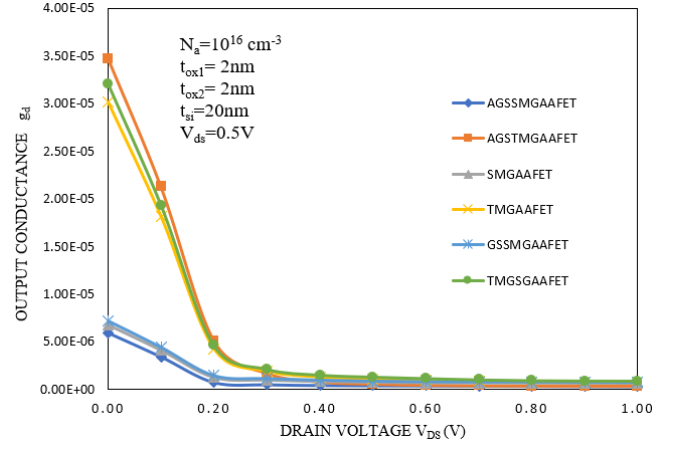


Figure 14: Plot of the change in output conductance (g_d) relative to the change in drain voltage (V_{DS})

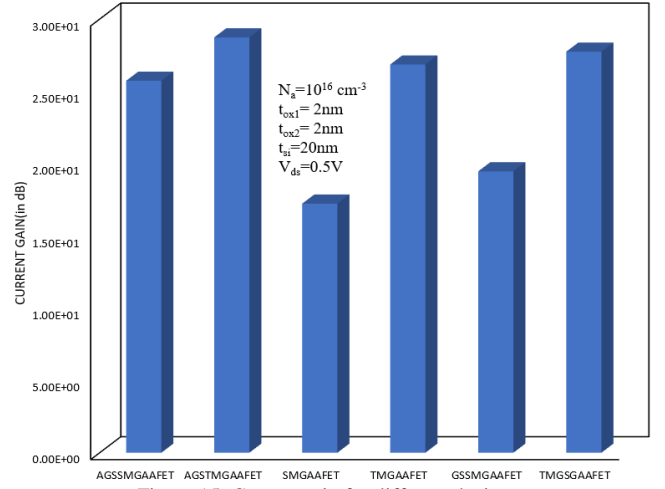


Figure 15: Current gain for different devices

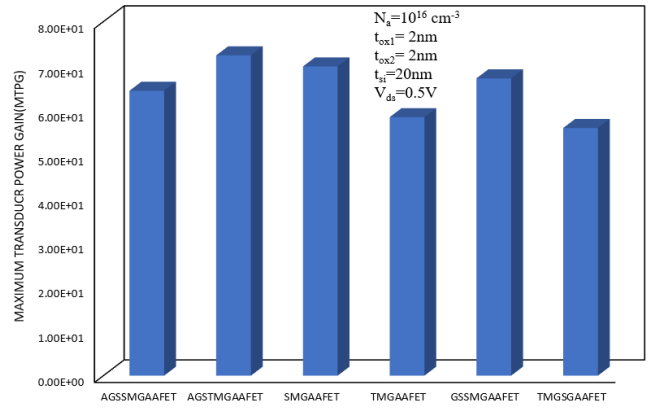


Figure 16: Maximum transducer power gain (MTPG) for various devices

Figure 16 gives the comparison of the Maximum transducer power gain (MTPG) of the various devices under study. This parameter basically gives the highest amount of power delivered to the load as a ratio of the power available from the source. This situation occurs when the load (Z_L) is matched to the devices output impedance (Z_O). The proposed device gives excellent performance in this respect as well.

$$MTPG = \left. \frac{P_{load}}{P_{source}} \right|_{Z_L = Z_O^*}$$

Now the combination of asymmetric gate stack with high-K dielectric and triple metal gate leads to the device having a large capacitance which in turn leads to a large electric field which causes a high saturation velocity for the charge carriers which leads to a large current value going from source to drain leading to a large MTPG.

V. CONCLUSION

In this paper AGSTMGAAFET is studied in terms of various device parameters. Excellent performance in terms of drain current, transconductance, output conductance, current gain, maximum transducer power gain which shows our device's suitability for various analog applications. Our device provides the advantages of triple work function gate and asymmetric gate stack which leads to increased carrier velocity, improvement of efficiency in carrier transport and alleviation of DIBL, hot-carrier effect and other SCE's moreover it leads to reduced power dissipation. Overall, the proposed device is suitable for various analog application requiring high gain and low power dissipation. The proposed analytical model for AGSTMGAAFET has been analyzed for different channel length ($L = 30, 45, 60$ nm) and radius of substrate ($R = 10, 12$ nm). It is so found that the analytical results for potential, electric field and subthreshold current are in close accordance with the simulated results.

VI. ACKNOWLEDMENT

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VII. FUNDING STATEMENT

Not Applicable

VIII. CONFLICT OF INTEREST

There are no conflicts of interest amongst the authors

IX. AUTHOR CONTRIBUTIONS

The authors have contributed mutually regarding this paper.

X. AVAILABILITY OF DATA AND MATERIAL

Not Applicable

XI. COMPLIANCE WITH ETHICAL STANDARDS

Not Applicable

XII. CONSENT TO PARTICIPATE

All the authors have complete consent to participate.

XIII. CONSENT FOR PUBLICATION

All the authors have complete consent for publication.

XIV. APPENDIX

$$\begin{aligned}
 P &:= -\frac{(K_2 - K_1)}{2 \cdot K_2 \cdot d_3^{-1}} \left[V_{bi} + X_1 - \frac{(X_1 - X_2)}{2 \cdot d_1^{-1}} \right] \cdot d_2 + \frac{(K_2 + K_1)}{2 \cdot K_2 \cdot d_3^{-1}} \cdot \frac{(X_1 - X_2)}{2 \cdot d_1^{-1}} \cdot d_2^{-1} + \frac{(X_3 - X_4)}{2 \cdot d_4} \cdot d_5^2 + \frac{(X_3 - X_4)}{2 \cdot d_4^{-1}} \\
 B_1 &:= \frac{(V_{bi} + V_{ds} + X_4) \cdot d_5 + \frac{(X_2 - X_3)}{2 \cdot d_3} \cdot d_5^2 + \frac{(X_2 - X_3)}{2 \cdot d_3^{-1}} - \frac{(K_2 + K_1)}{2 \cdot K_2 \cdot d_3} \left[V_{bi} + X_1 - \frac{(X_1 - X_2)}{2 \cdot d_1^{-1}} \right] \cdot d_2 \cdot d_5^2 + \frac{(K_2 - K_1)}{2 \cdot K_2 \cdot d_3} \cdot \frac{(X_1 - X_2)}{2 \cdot d_1^{-1}} \cdot d_2^{-1} \cdot d_5^2 + P}{\frac{(K_2 + K_1)}{2 \cdot K_2 \cdot d_3^{-1}} \cdot d_2^{-1} - \frac{(K_2 - K_1)}{2 \cdot K_2 \cdot d_3^{-1}} \cdot d_2 + \frac{(K_2 - K_1)}{2 \cdot K_2 \cdot d_3} \cdot d_2^{-1} \cdot d_5^2 - \frac{(K_2 + K_1)}{2 \cdot K_2 \cdot d_3} \cdot d_2 \cdot d_5^2} \\
 B_2 &:= B_1 + \frac{(X_2 - X_1)}{2 \cdot d_1^{-1}} \quad B_3 := \frac{(K_2 - K_1)}{2 \cdot K_2 \cdot d_3^{-1}} \cdot A_2 \cdot d_2 + \frac{(K_1 + K_2)}{2 \cdot K_2 \cdot d_3^{-1}} \cdot B_2 \cdot d_2^{-1} - \frac{K_2 \cdot (X_2 - X_3)}{2 \cdot K_2 \cdot d_3^{-1}} \\
 B_4 &:= \frac{(K_2 - K_1)}{2 \cdot K_2 \cdot d_3^{-1}} \left[V_{bi} - B_1 + X_1 - \frac{(X_1 - X_2)}{2 \cdot d_1^{-1}} \right] \cdot d_2 + \frac{(K_2 + K_1)}{2 \cdot K_2 \cdot d_3^{-1}} \cdot \left[B_1 - \frac{(X_1 - X_2)}{2 \cdot d_1^{-1}} \right] \cdot d_2^{-1} - \frac{(X_2 - X_3)}{2 \cdot d_3^{-1}} - \frac{(X_3 - X_4)}{2 \cdot d_4^{-1}} \\
 A_1 &:= V_{bi} - B_1 + X_1 \quad A_2 := A_1 - \frac{(X_1 - X_2)}{2 \cdot d_1^{-1}} \quad A_3 := \frac{(K_1 + K_2)}{2 \cdot K_2 \cdot d_3} \cdot A_2 \cdot d_2 + \frac{(K_2 - K_1)}{2 \cdot K_2 \cdot d_3} \cdot B_2 \cdot d_2^{-1} - \frac{K_2 \cdot (X_2 - X_3)}{2 \cdot K_2 \cdot d_3}
 \end{aligned}$$

$$A_4 := \frac{(K_2 + K_1)}{2 \cdot K_2 \cdot d_3} \cdot \left[V_{bi} - B_1 + X_1 - \frac{(X_1 - X_2)}{2 \cdot d_1} \right] \cdot d_2 + \frac{(K_2 - K_1)}{2 \cdot K_2 \cdot d_3} \cdot \left[B_1 - \frac{(X_1 - X_2)}{2 \cdot d_1^{-1}} \right] \cdot d_2^{-1} - \frac{(X_2 - X_3)}{2 \cdot d_3} - \frac{(X_3 - X_4)}{2 \cdot d_4}$$

Where,

$$X_1 := \frac{Y_1}{K_1^2}, X_2 := \frac{Y_2}{K_1^2}, X_3 := \frac{Y_3}{K_2^2}, X_4 := \frac{Y_4}{K_2^2}, d_1 := e^{K_1 \cdot L_1}, d_2 := e^{K_1 \cdot L_2}, d_3 := e^{K_2 \cdot L_2}, d_4 := e^{K_2 \cdot L_3}, d_5 := e^{K_2 \cdot L_4}$$

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Figures

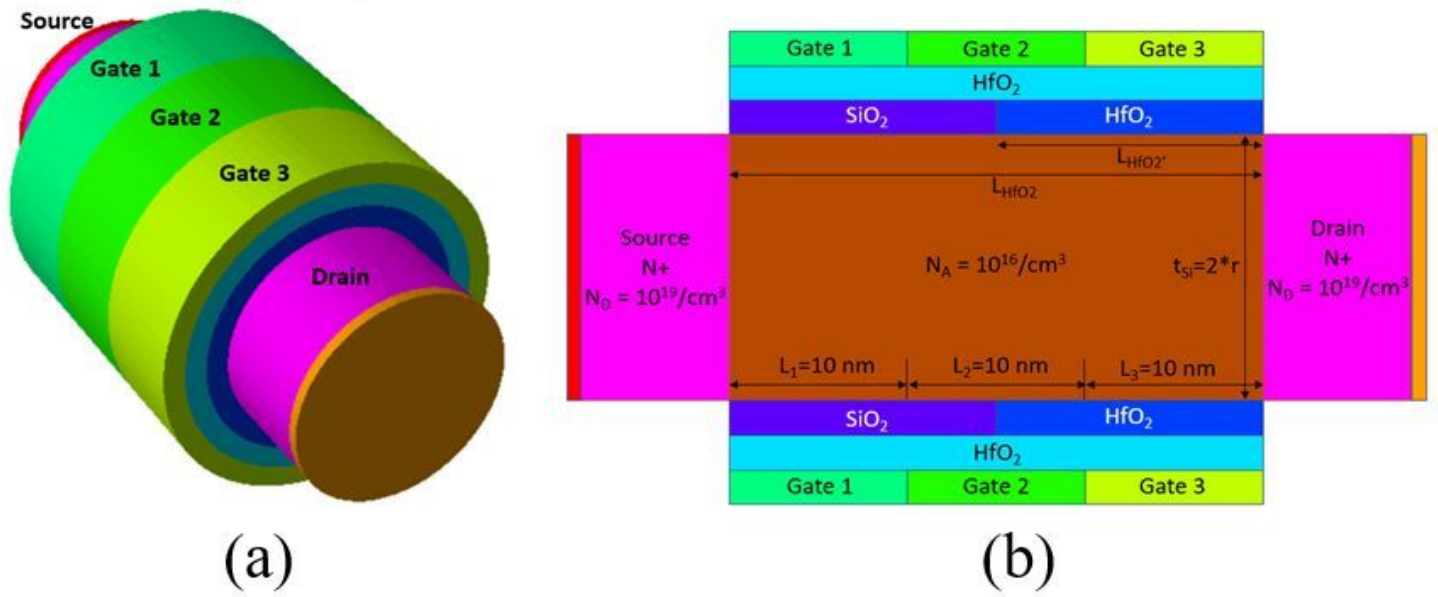
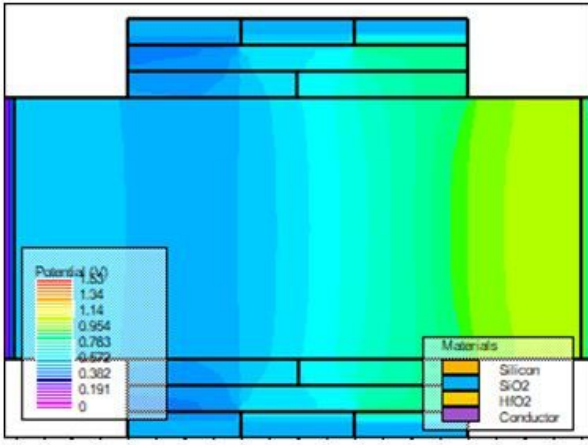
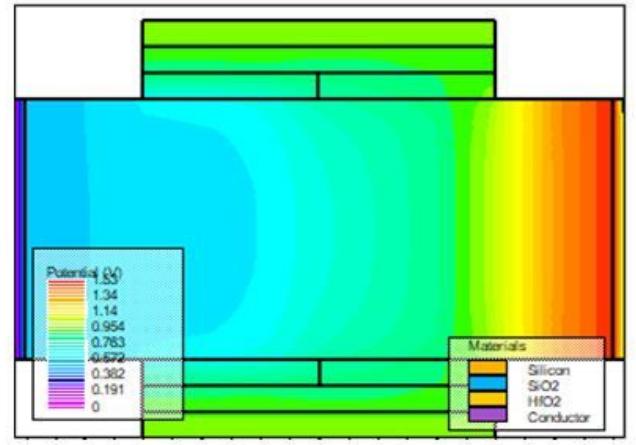


Figure 1

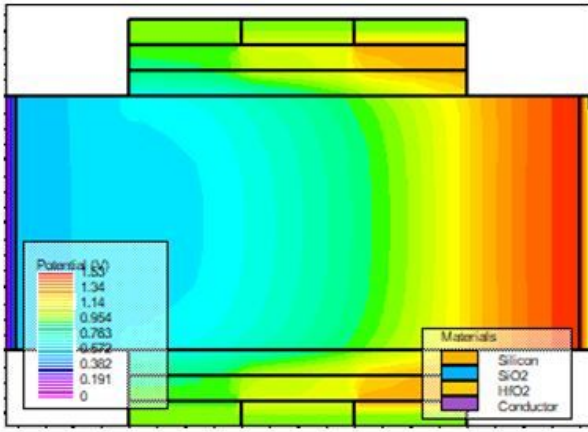
.a) 3-D Structural View of Asymmetric Gate Stack Triple Metal Gate All Around MOSFET (b) 2-D Cross sectional View of Asymmetric Gate Stack Triple Metal Gate All Around MOSFET



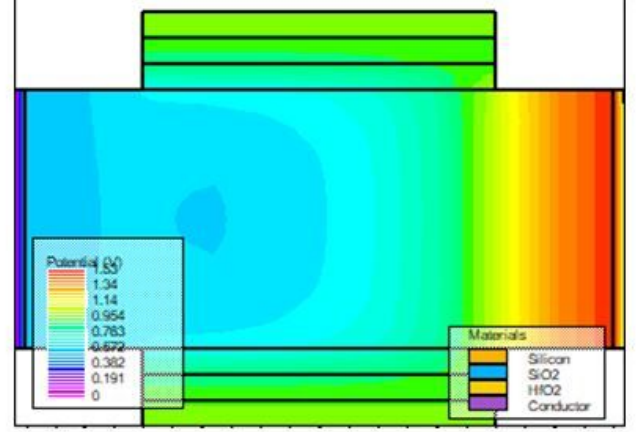
(a)



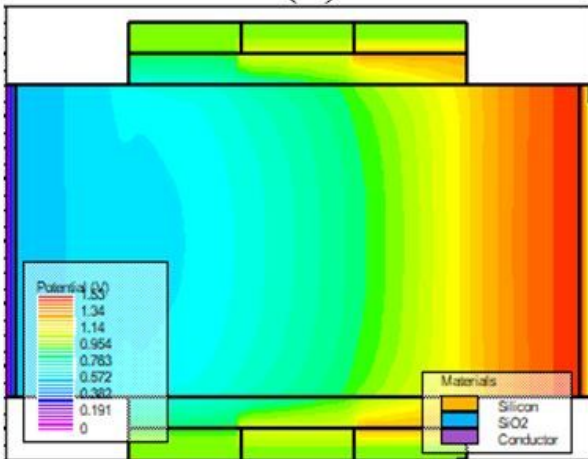
(b)



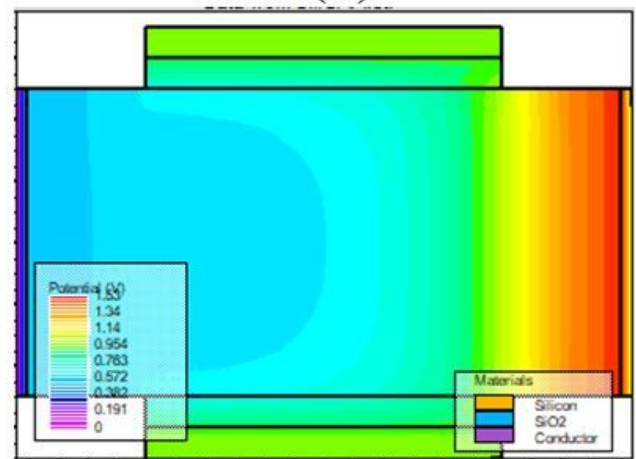
(c)



(d)



(e)



(f)

Figure 2

Contour potential plots for the various devices under study where (a) AGSTMGAAFET (b) AGSGSMGAAFET (c) GSTMGAAFET (d) GSSMGAAFET (e) TMGAAFET (f) SMGAAFET

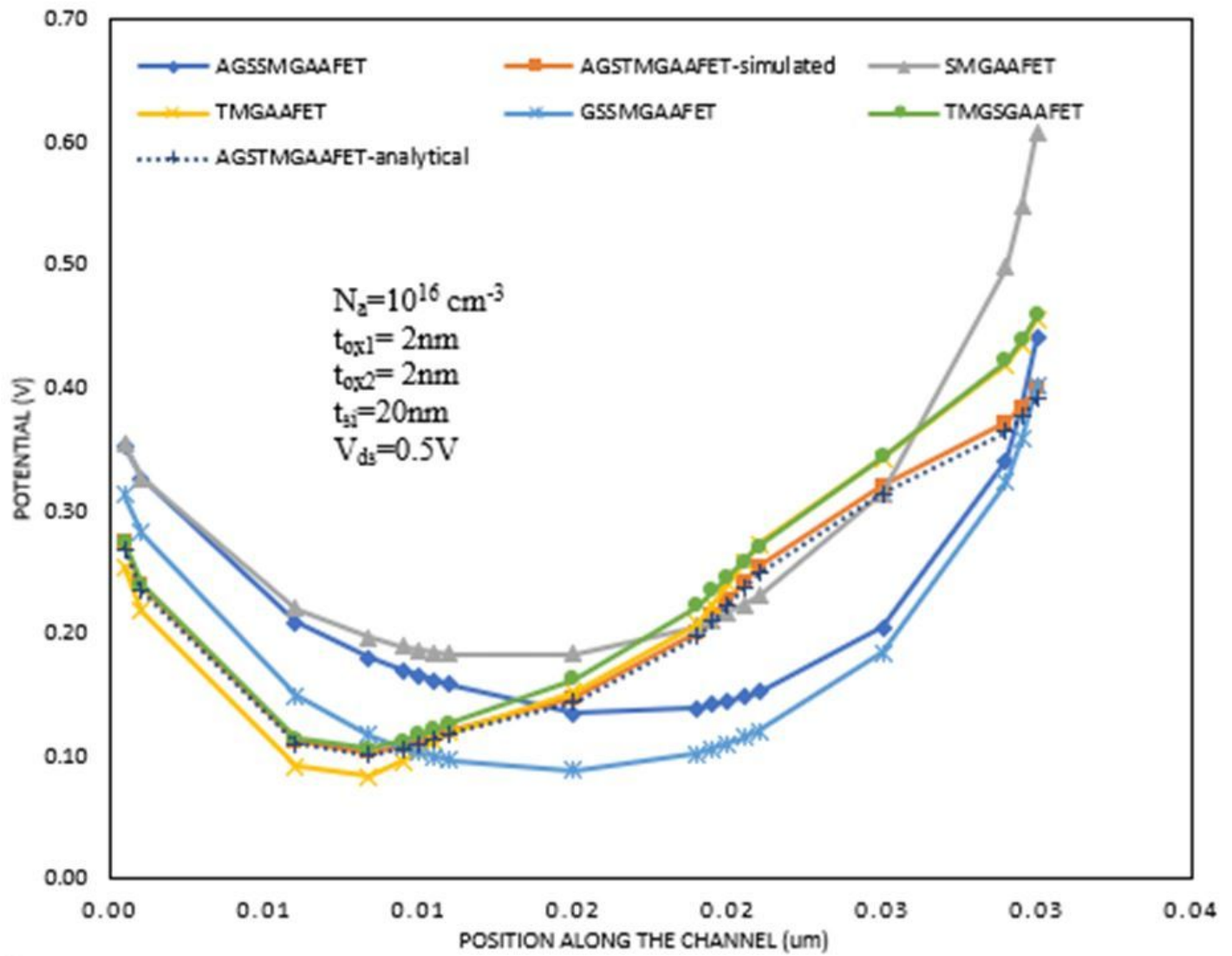


Figure 3

Surface Potential for all 6 models and analytical model for AGSTMGAAFET

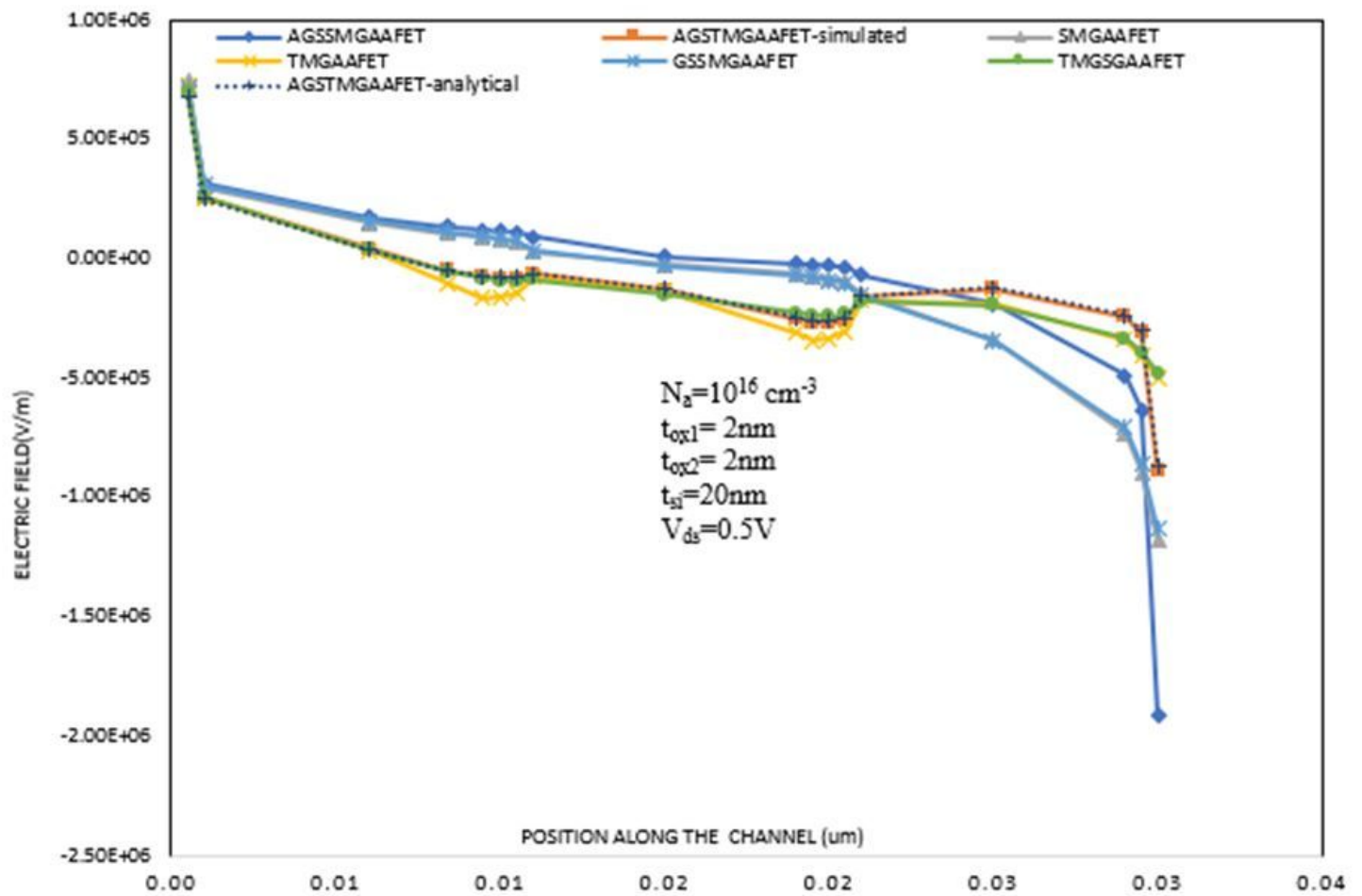
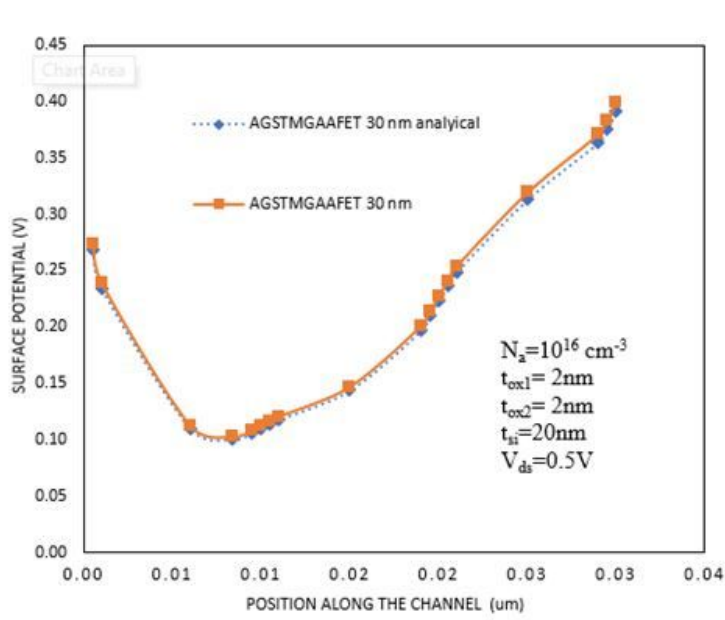
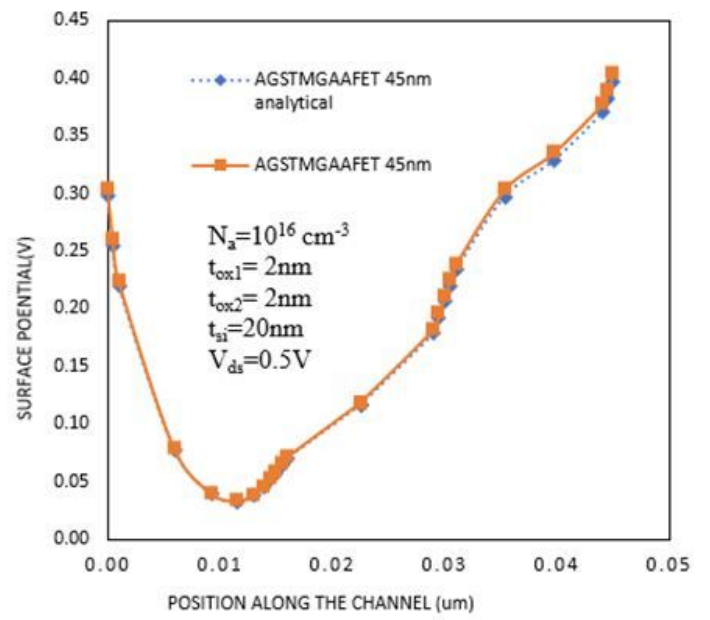


Figure 4

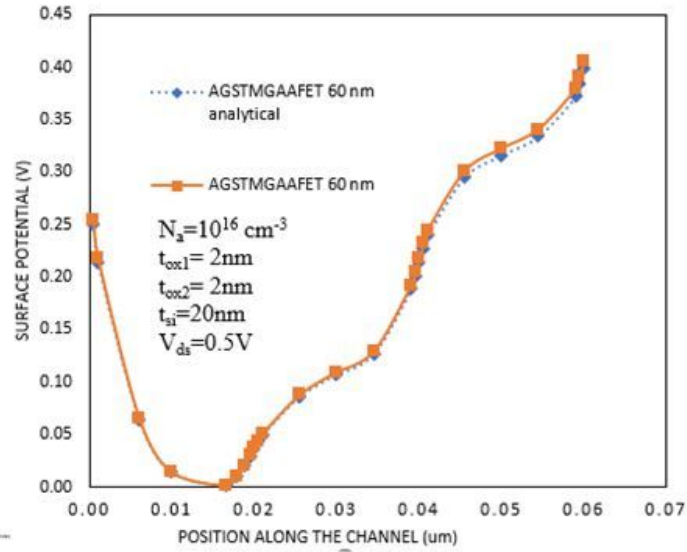
Electric Field for all 6 models and analytical model for AGSTMGAAFET



(a)



(b)



(c)

Figure 5

Surface Potential vs Channel Length for AGSTMGAAFET (a) L = 30 nm (b) L = 45 nm (c) L = 60 nm

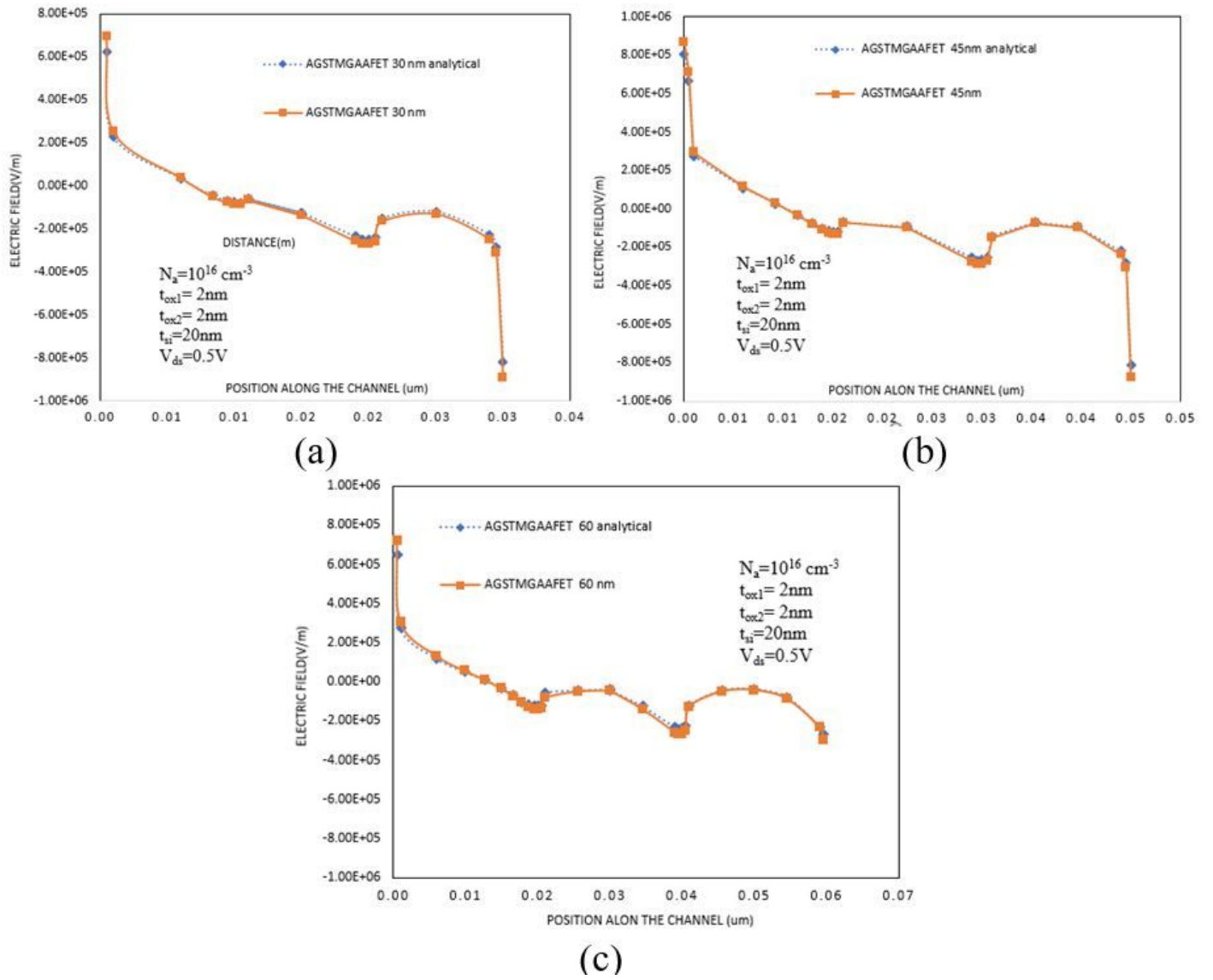


Figure 6

Electric Field vs Channel Length for AGSTMGAAFET (a) $L = 30 \text{ nm}$ (b) $L = 45 \text{ nm}$ (c) $L = 60 \text{ nm}$

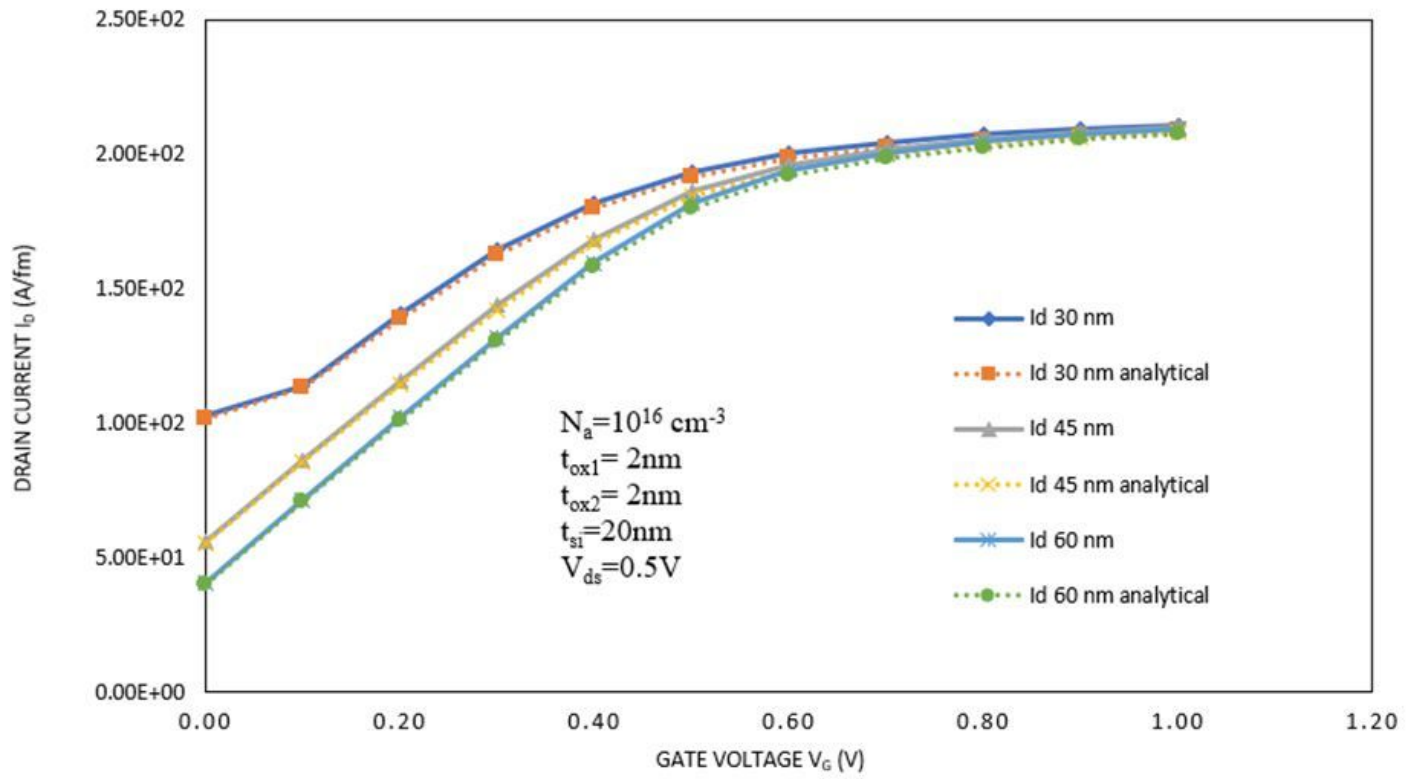


Figure 7

Subthreshold current (I_D) vs gate voltage (V_G) for AGSTMGAAFET for $L = 30, 45$ and 60 nm

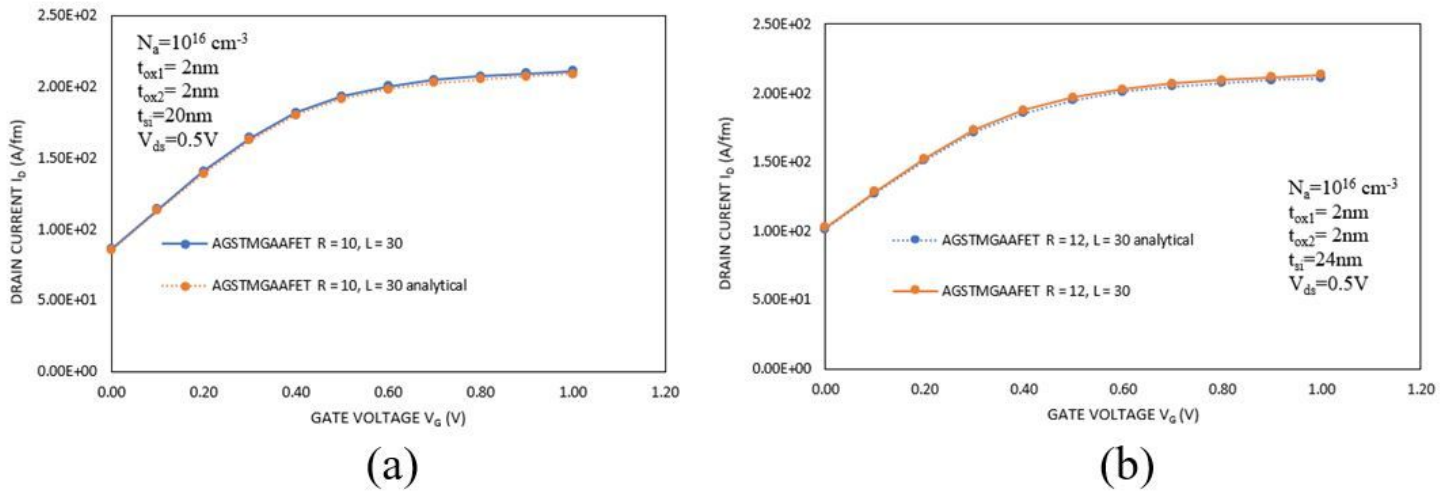


Figure 8

Subthreshold current (I_D) vs gate voltage (V_G) for AGSTMGAAFET with $L = 30$ nm and different radius
(a) $R = 10$ nm (b) $R = 12$ nm

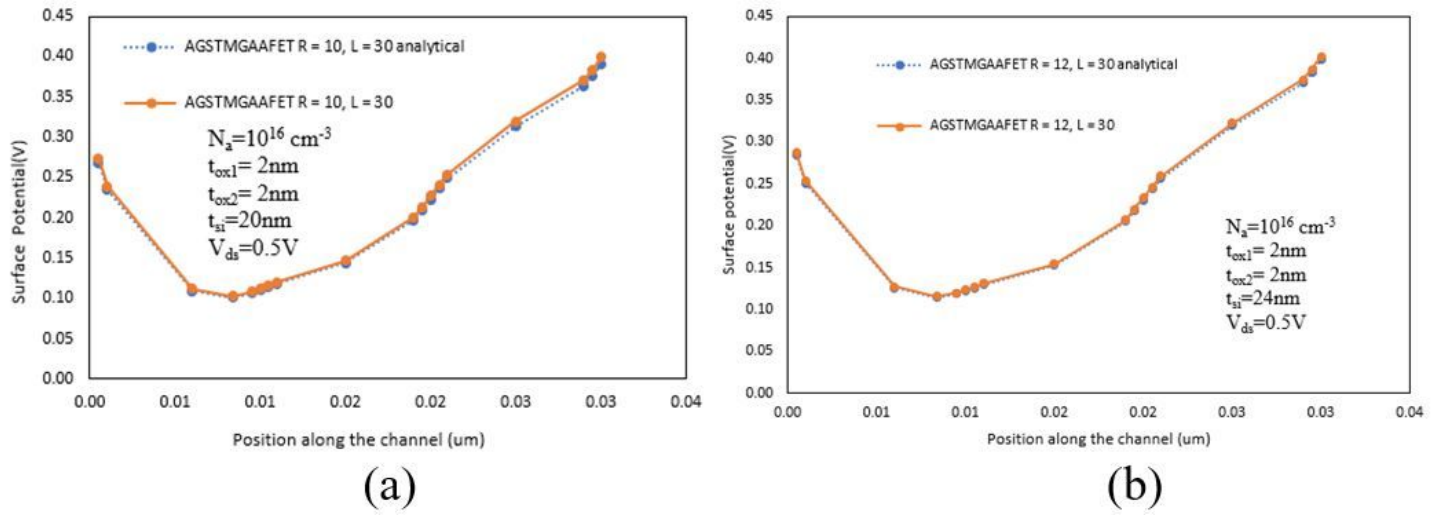


Figure 9

Surface Potential for AGSTMGAAFET with L = 30 nm and different radius (a) R = 10 nm (b) R = 12 nm

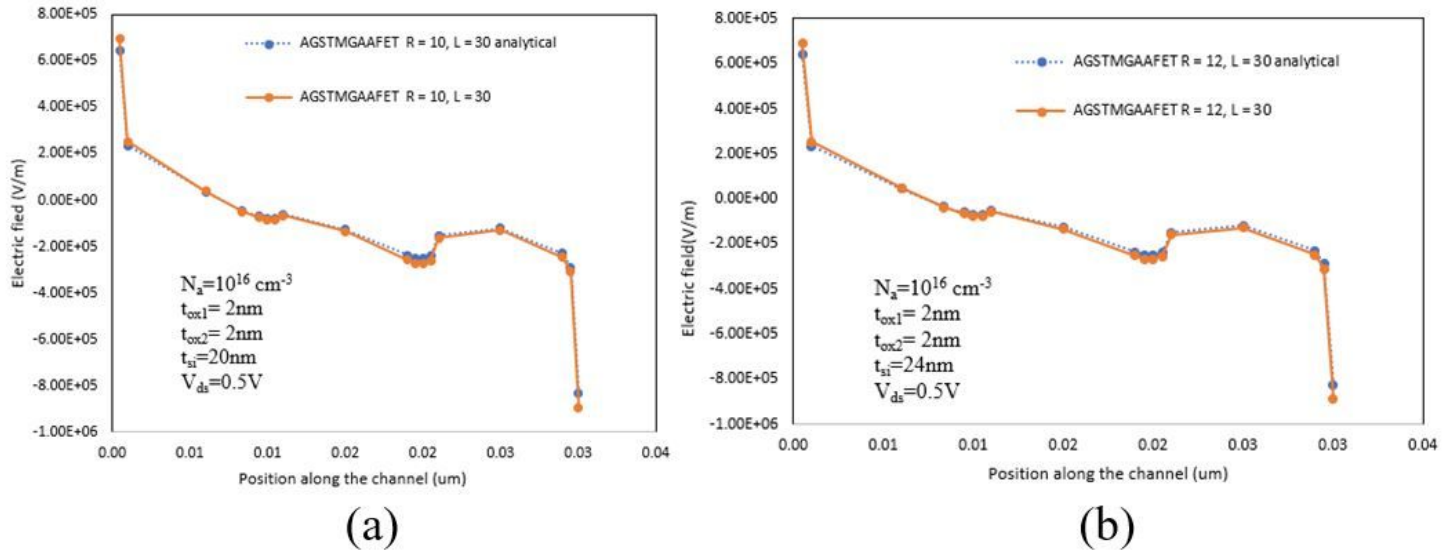


Figure 10

Electric Field for AGSTMGAAFET with L = 30 nm and different radius (a) R = 10 nm (b) R = 12 nm

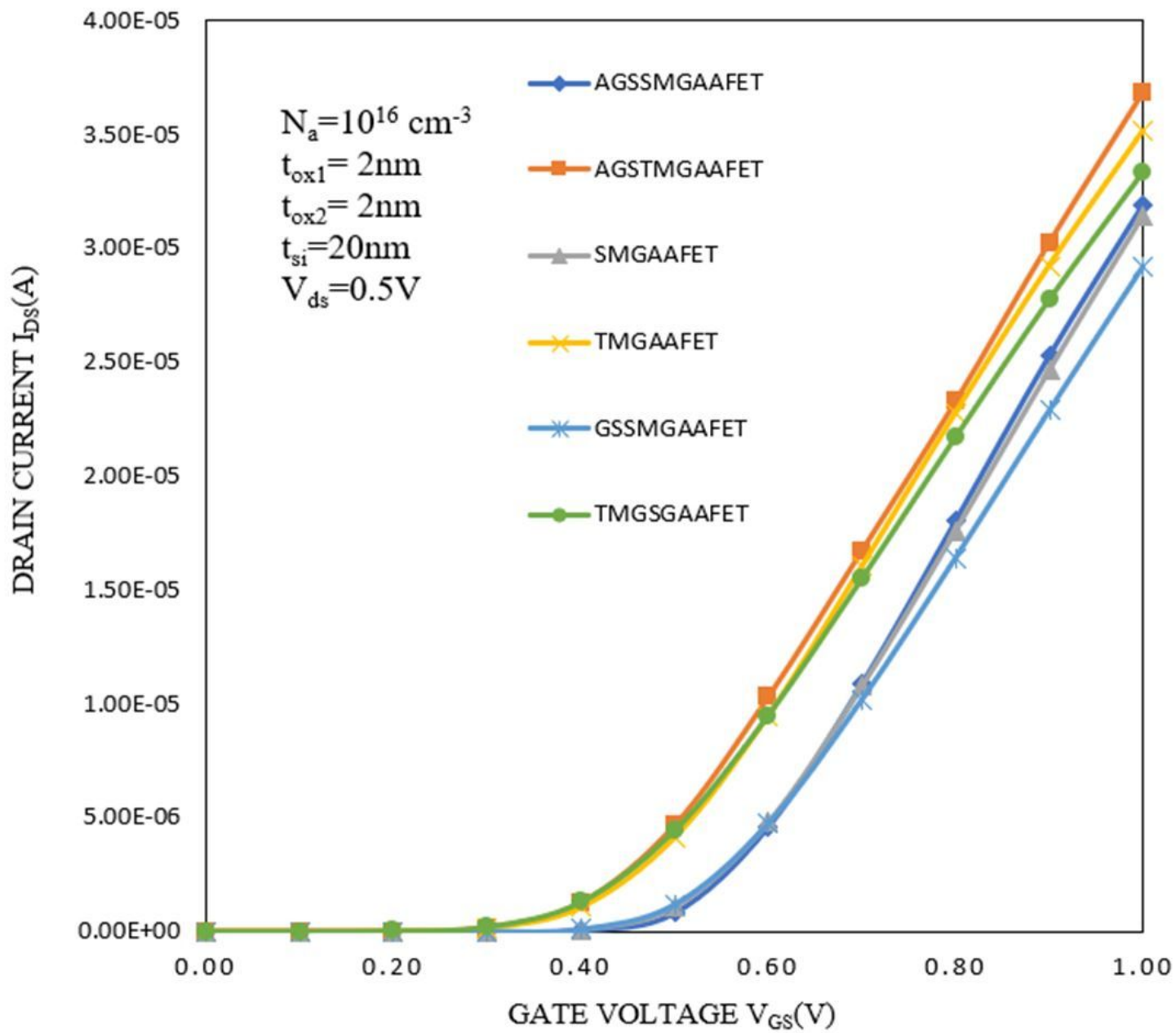


Figure 11

Plot of the change in drain current (I_{DS}) relative to change in gate voltage (V_{GS})

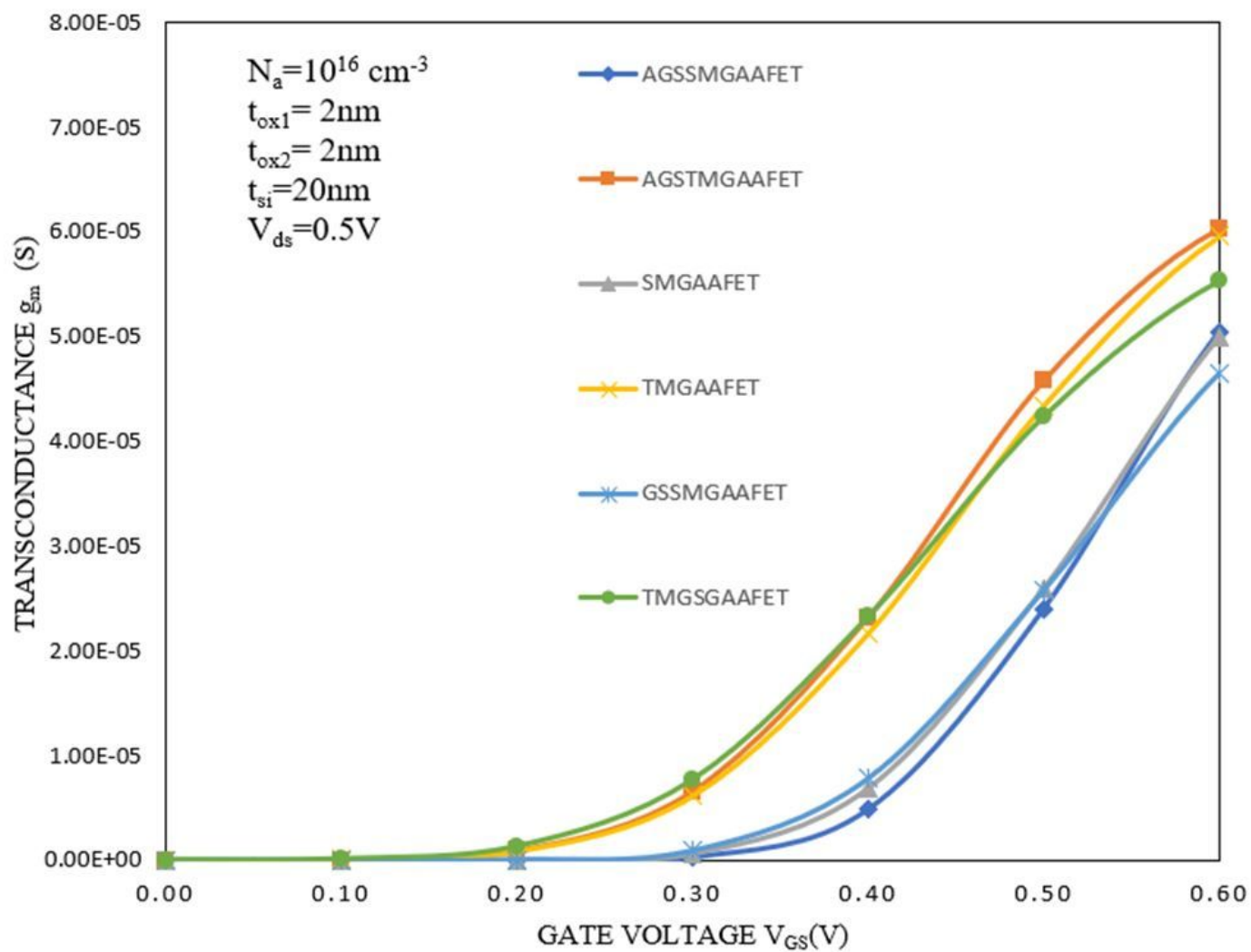


Figure 12

Plot of the change in transconductance (g_m) relative to change in gate voltage (V_{GS})

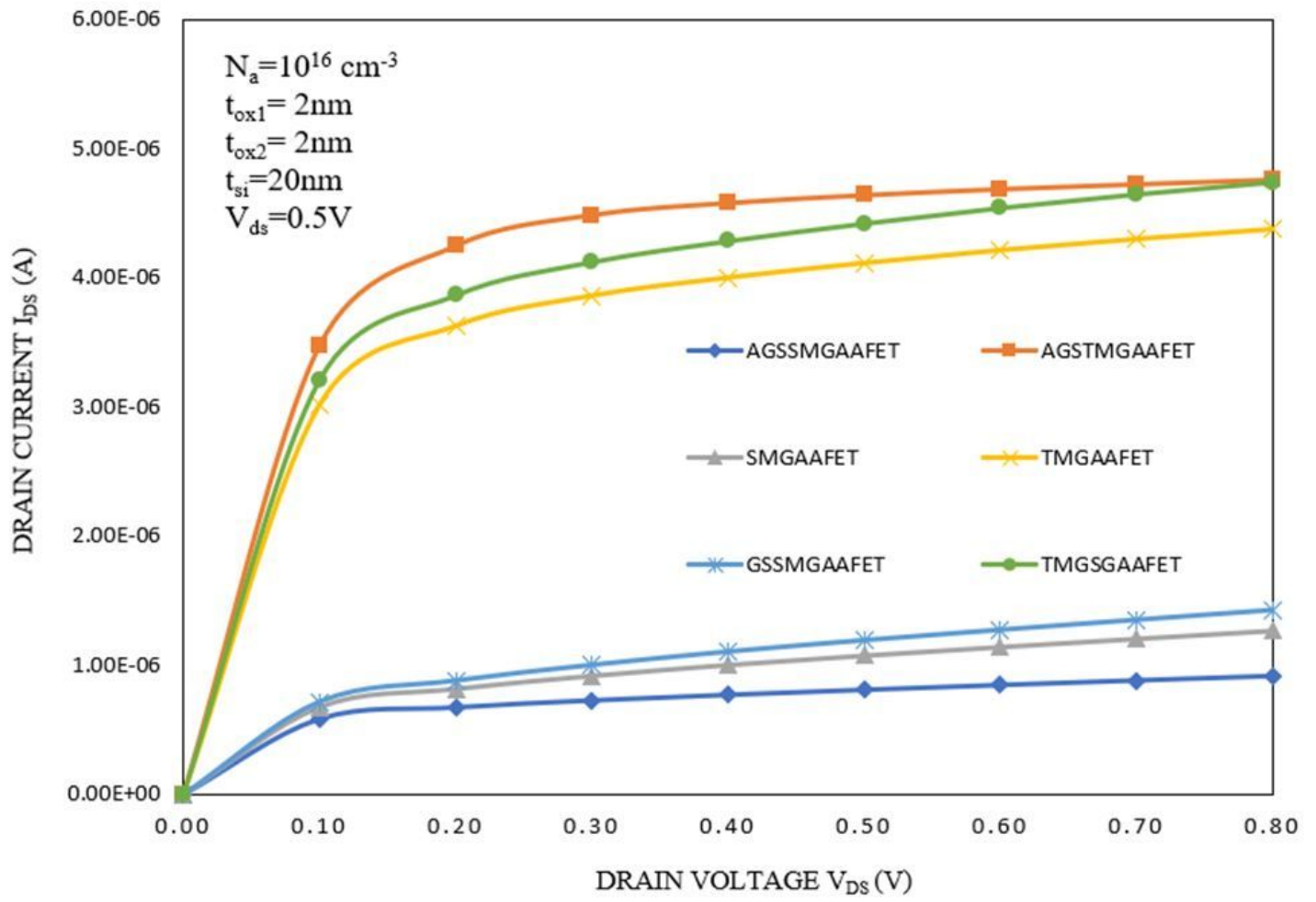


Figure 13

Plot of the change in drain current (I_{DS}) relative to change in drain voltage (V_{DS})

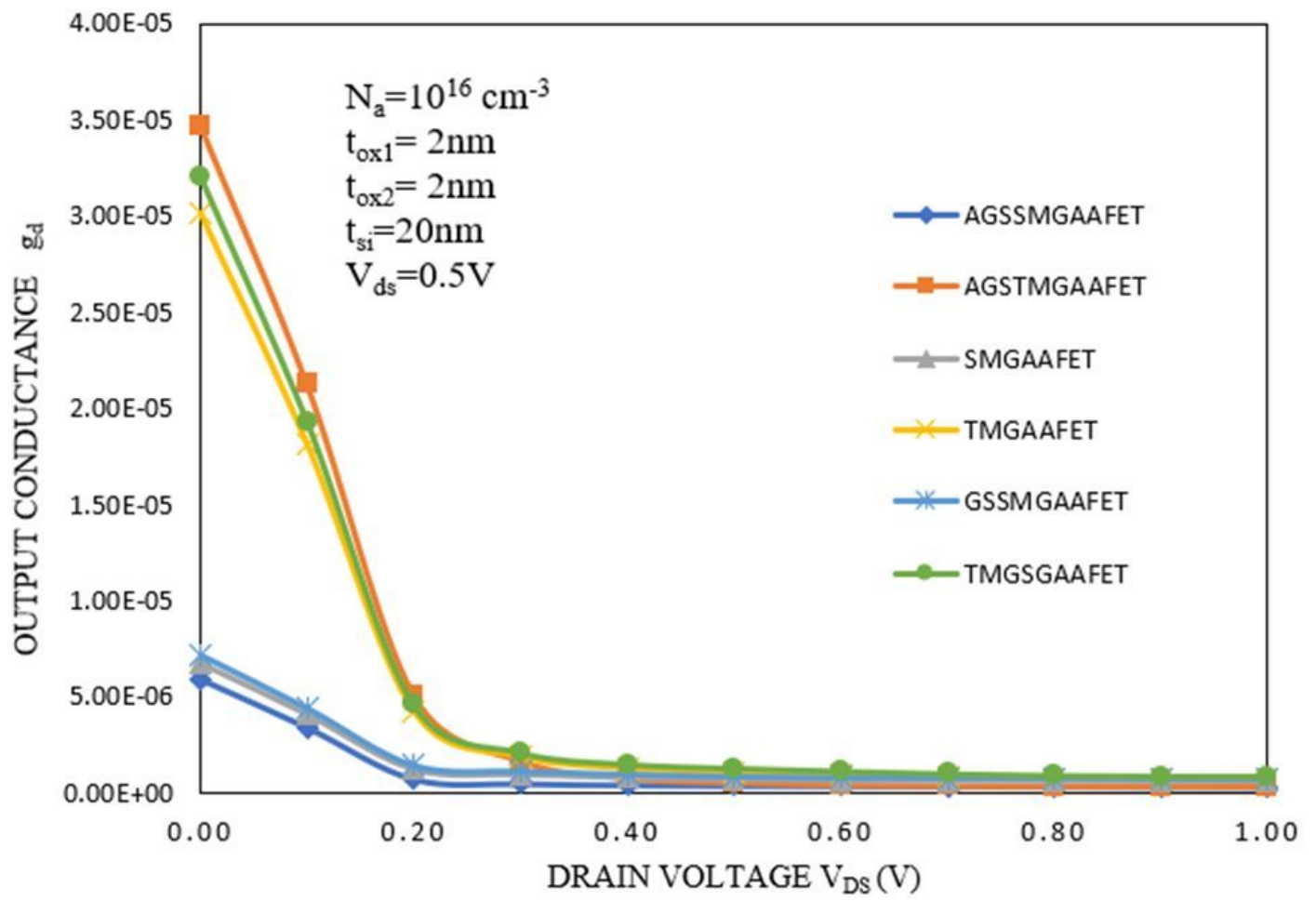


Figure 14

Plot of the change in output conductance (g_d) relative to the change in drain voltage (V_{DS})

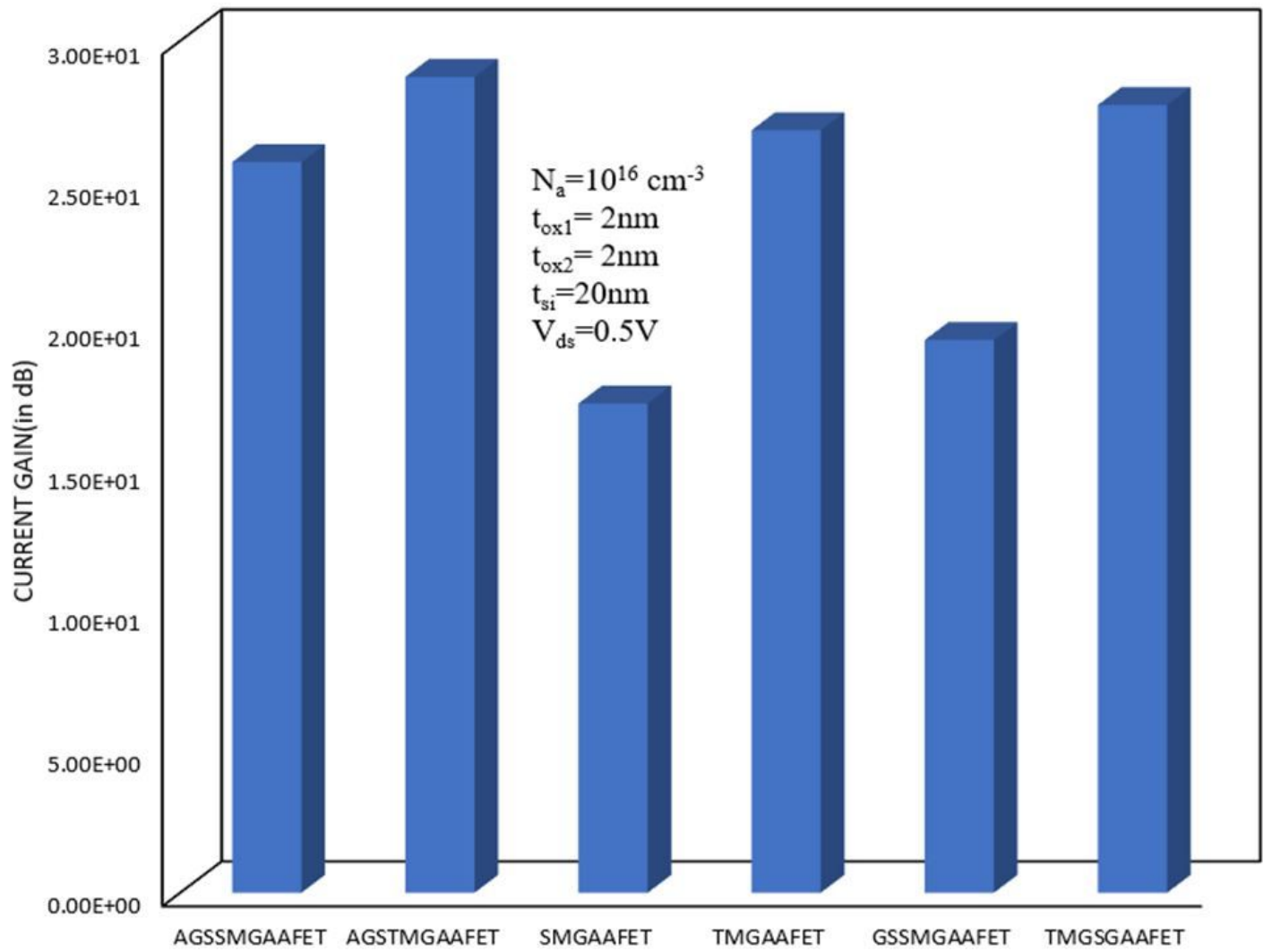


Figure 15

Current gain for different devices

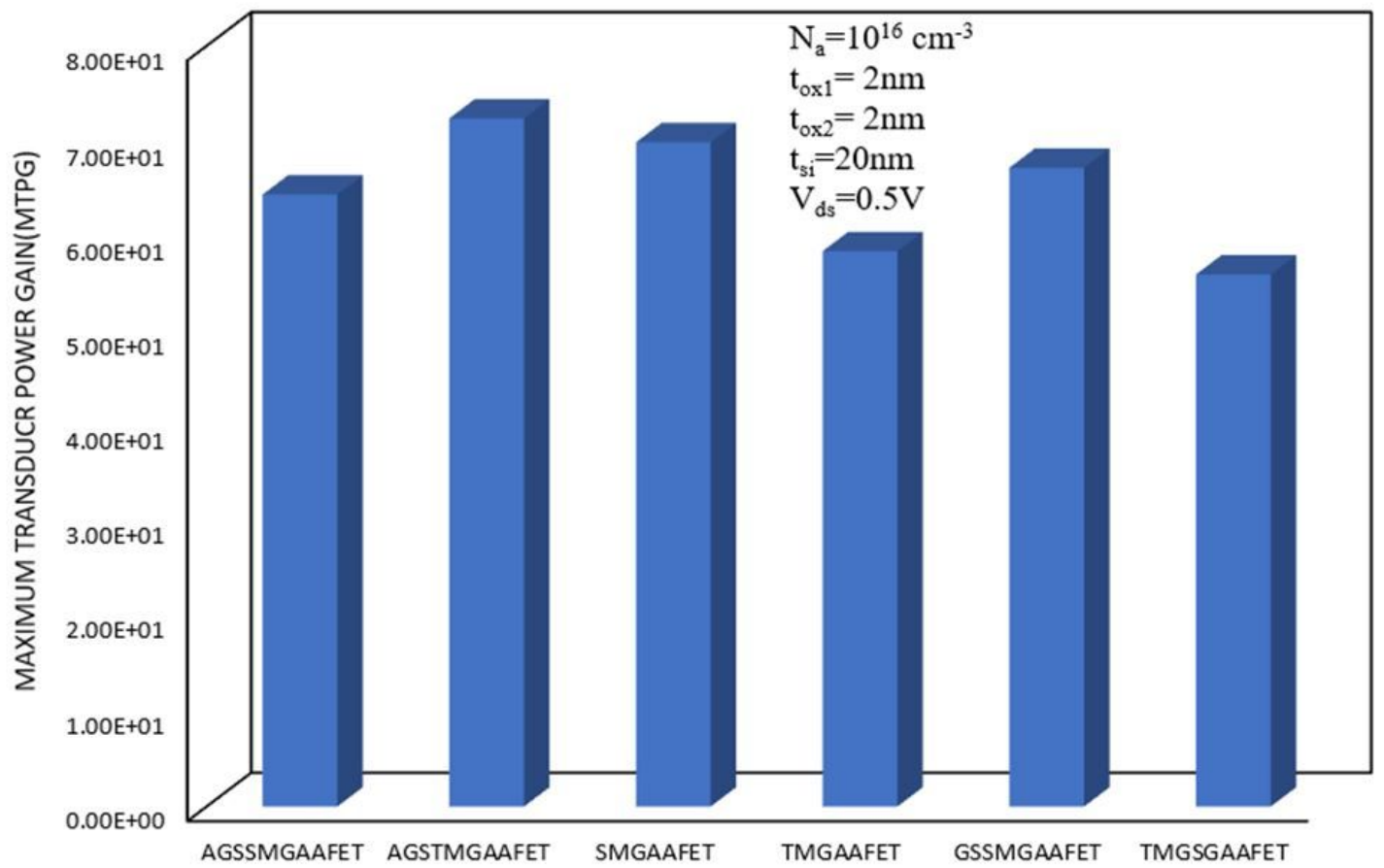


Figure 16

Maximum transducer power gain (MTPG for various devices)