# A Novel Superjunction MOSFET with Ultralow Reverse Recovery Charge and Low Switching Loss

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**Research Article**

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# A Novel Superjunction MOSFET with Ultralow Reverse Recovery Charge and Low Switching Loss

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*Abstract*—A novel superjunction MOSFET (SJ-MOSFET) for ultralow reverse recovery charge ($Q_{RR}$) and low switching loss is proposed and investigated. This device features a P-type Schottky diode and a source field-plate. The P-type Schottky diode consists of Schottky contact and P-base, which is reverse series-connected with body P-N junction diode. And the source field-plate is formed by implementing a polysilicon field-plate electrically coupled to the source, which is on the top of N-pillar. During the reverse conduction state, the P-type Schottky diode is reverse biased, which dramatically suppresses minority carriers injecting into the drift region. Simultaneously, electron accumulation layer formed under the source field-plate, which provides a path for the reverse current. Consequently, compared with the conventional SJ-MOSFET (Conv-SJ-MOSFET), the proposed SJ-MOSFET achieves an 84.0% lower $Q_{RR}$ with almost no sacrifice in other characteristics. Moreover, the proposed device also exhibits 47.4% and 66.0% lower gate charge ($Q_G$) and gate to drain charge ($Q_{GD}$), respectively. The significantly reduced $Q_G$, $Q_{GD}$, and $Q_{RR}$ contribute to an overall improvement in switching losses and resultant over 54.8% decrease in total power losses with operation frequency higher than 50 kHz, demonstrating great potential of the proposed SJ-MOSFET used in power conversion systems.

Keywords—MOSFET, superjunction (SJ), reverse recovery, Schottky contact, field-plate.

## I. INTRODUCTION

The superjunction MOSFET (SJ-MOSFET) is now a dominator in power switch for the voltage range of 500 ~ 650 V [1-2]. By utilizing the charge balance concept, the SJ-MOSFET has broken through the well-known silicon limit for unipolar power devices [3]. However, because of the excess minority carriers in the drift region, its body P-N junction diode suffers from large reverse recovery charge ($Q_{RR}$). This causes high switching losses on the bridge circuit application where the body P-N junction diode is required to conduct in the freewheeling period [4-5]. Lifetime killing processes such as irradiation by electrons, protons or helium and heavy metal doping with gold or platinum are used in most commercial products to reduce $Q_{RR}$ [6-8]. Nevertheless, these methods tend to cause contamination and degrade both ON-resistance and leakage current. Integrating Schottky diode in parallel with body P-N junction diode is effective in reducing $Q_{RR}$ [9-12]. However, leakage current increases dramatically, and device long-term reliability is weakened. Integrating built-in MOS channel diode has been used to reduce the minority carrier injection of the body P-N junction diode of SJ-MOSFET [13-14]. Unfortunately, the thin oxide or the lowly doped P-base of the MOS channel diode causes an increase in leakage current and steps of fabrication process. Besides, a relatively high $Q_{RR}$ still exists to some extent due to the conduction of body P-N junction diode.

In this study, an ultralow reverse recovery charge and low switching loss SJ-MOSFET which features a P-type Schottky diode and a source field-plate is proposed. During the reverse conduction state, the conduction of the body P-N junction diode is dramatically suppressed by the reverse-biased P-type Schottky diode which is composed of Schottky contact and P-base. And an electron accumulation layer under the source field-plate is formed with the augment of reverse voltage, which provides a path for the reverse current. Consequently, the minority carrier injection is suppressed dramatically, leading to a superior reverse recovery performance. Furthermore, the introduction of source field-plate reduces the area of gate electrode, gate charge is thus decreased, resulting in an improved switching performance.

## II. STRUCTURE AND MECHANISM

The schematic cross-sectional structures of the conventional SJ-MOSFET (Conv-SJ-MOSFET) and the proposed SJ- MOSFET are shown in Fig. 1(a) and (b). The proposed SJ-MOSFET is distinguished from the Conv-SJ-MOSFET in the sense that a Schottky contact is introduced on the top of the P-base forming a P-type Schottky diode, and a polysilicon field-plate electrically coupled to the source is implemented forming a source field-plate. It's should be pointed out that the P-type Schottky diode is reverse series-connected with the body P-N junction diode, and the potential of P-base region is clamped by the P-type Schottky diode because the anode of the

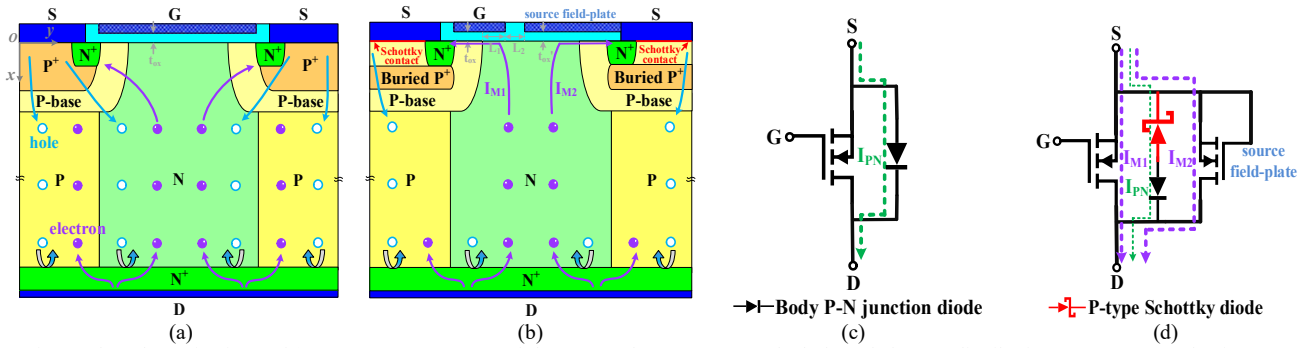



Fig. 1. The schematic views of (a) Conv-SJ-MOSFET and (b) proposed SJ-MOSFET. The hole and electron distributions at reverse conduction state with $V_{GS}$ = 0 V are illustrated. The simplified circuits of (a) Conv-SJ-MOSFET and (b) proposed SJ-MOSFET. The dashed lines show the components of current in reverse conduction state with $V_{GS}$ = 0 V.

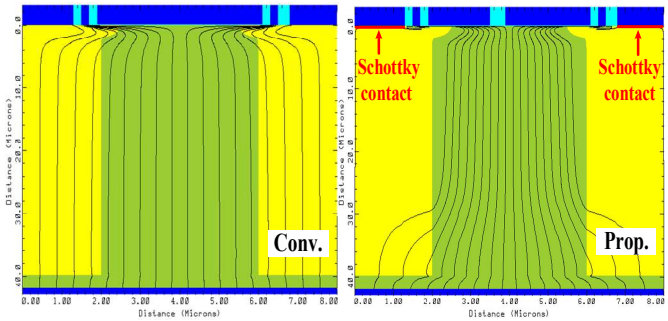



Fig. 2. The distributions of current at $I_{DS}$ = - 100 A/cm$^2$ and $V_{GS}$ = 0 V of (a) Conv-SJ-MOSFET and (b) proposed SJ-MOSFET. In the proposed SJ-MOSFET, electron accumulation layers are formed under both source field-plate and gate with $V_{GS}$ = 0 V.

P-type Schottky diode is connected to the source electrode. In the Conv-SJ-MOSFET, a highly doped $P^+$ region is used in the P-base region to suppress the conduction of parasitic NPN transistor ($N^+$ source/P-base/ N-pillar), while in the proposed SJ-MOSFET a buried $P^+$ layer is used as a replacement.

The simplified circuits of the two studied SJ-MOSFETs are shown in Fig. 1(c) and (d), and the distributions of current in reverse conduction state are shown in Fig. 2. As shown in Fig. 1(d), the P-type Schottky diode is reverse series-connected with the body P-N junction diode, thus the conduction current of body P-N junction diode ($I_{PN}$) is dramatically reduced by the reverse-biased P-type Schottky diode during the reverse conduction state, which suppresses the injection of minority carrier greatly. Simultaneously, electron accumulation layer under the source field-plate is formed with the augment of reverse voltage, providing a path for reverse current ($I_{M2}$). Besides, electron accumulation layer under the gate is also formed when $V_{GS}$ = 0 V, conducting partial reverse current ($I_{M1}$). Only a small part of the reverse current (i.e., $I_{PN}$) flows through the body P-N junction diode due to the leakage current induced by the reverse-biased P-type Schottky diode as revealed in Fig 2(b). While in the Conv-SJ-MOSFET, there is no electron accumulation layer formed during the reverse conduction state, coupled with a low turn-on voltage of the forward-biased body P-N junction diode, the reverse current is thus fully conducted by the body P-N junction diode (i.e., $I_{PN}$) as shown in Fig. 2(a). Because both $I_{M1}$ and $I_{M2}$ are majority carrier current, only $I_{PN}$ contains minority carrier current. Hence, compared with the Conv-SJ-MOSFET, ultralow minority carriers in the drift region of the proposed SJ-MOSFET are obtained as a result of the significantly reduced current component $I_{PN}$, which induces an ultralow $Q_{RR}$ and a resultant better reverse recovery performance. Besides, the introduction of source field-plate reduces the area of gate electrode, gate charge is thus reduced, resulting in an improved switching performance.

## III. Results and Discussion

The performance of the proposed SJ-MOSFET is investigated by both single device and mixed-mode simulations using MEDICI [15]. The optimized parameters as listed in Table 1. Unless otherwise specified, oxide thickness under the source field-plate ($t_{ox}'$) is set to 80 nm, which is the same as the thickness of gate oxide ($t_{ox}$), and the Schottky barrier height to P-base ($\Phi_{BP}$) is set to 0.5 eV, which can be realized by aluminum-silicon contact [16].

Table 1 Key Parameters for the studied SJ-MOSFETs

| Definitions | Conv. | Prop. | Units |
|---|---|---|---|
| N/P pillar doping | $6\times10^{15}$ | $6\times10^{15}$ | $cm^{-3}$ |
| N/P pillar width | 4 | 4 | μm |
| N/P pillar thickness | 40 | 40 | μm |
| $N^+$ (sub) doping | $1\times10^{19}$ | $1\times10^{19}$ | $cm^{-3}$ |
| $N^+$ (sub) thickness | 2 | 2 | μm |
| P-base doping | $1\times10^{17}$ | $1\times10^{17}$ | $cm^{-3}$ |
| P-base thickness | 2 | 2 | μm |
| Channel length | 0.6 | 0.6 | μm |
| Thickness of gate oxide ($t_{ox}$) | 80 | 80 | nm |
| Width of JFET region | 3 | 3 | μm |
| Hole/electron carrier lifetime (τ) | 1000 | 1000 | μs |
| Gate length in the top of JFET region ($L_1$) | / | 1 | μm |
| Distance between gate and source field-plate ($L_2$) | / | 0.4 | μm |
| $P^+$ source doping | $4\times10^{19}$ | / | $cm^{-3}$ |
| $P^+$ source thickness | 1.5 | / | μm |
| Buried $P^+$ layer doping | / | $1\times10^{19}$ | $cm^{-3}$ |
| Buried $P^+$ layer thickness | / | 1 | μm |

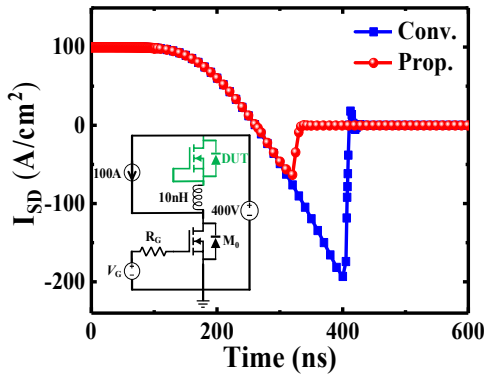



Fig. 3. Simulated reverse recovery characteristics. The inset is the test circuit configuration, where each device has an area of 1 $cm^2$, $V_G$ is 0 V to 10 V and the current communication rate di/dt is set to 1250 A/($cm^2$ • μs).

Fig. 3 shows the simulated reverse recovery characteristics. Due to excessively stored minority carriers in the drift region, peak reverse recovery current ($I_{RRM}$) of 194 A/$cm^2$, reverse recovery time ($t_{RR}$) of 147 ns and reverse recovery charge ($Q_{RR}$) of 14.79 μC/$cm^2$ are observed for Conv-SJ-MOSFET. The proposed SJ-MOSFET exhibits much reduced $I_{RRM}$ of 64 A/$cm^2$, $t_{RR}$ of 70 ns and $Q_{RR}$ of 2.36 μC/$cm^2$, counting for decreases of 67.0 %, 52.4 % and 84.0 %, respectively. This improvement stems from the decreased density of minority carriers in the drift region. Consequently, a superior reverse recovery performance of the proposed SJ-MOSFET is obtained.

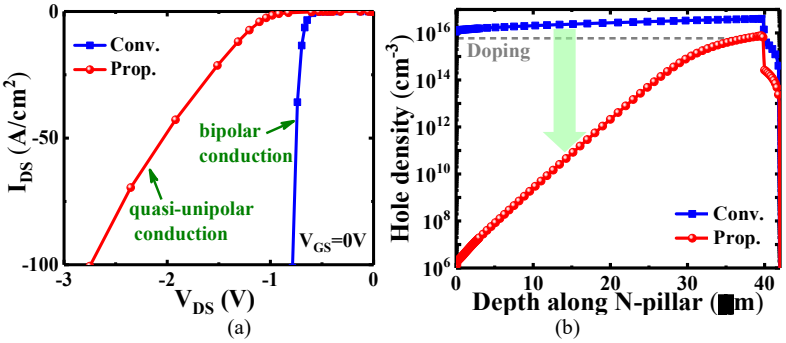
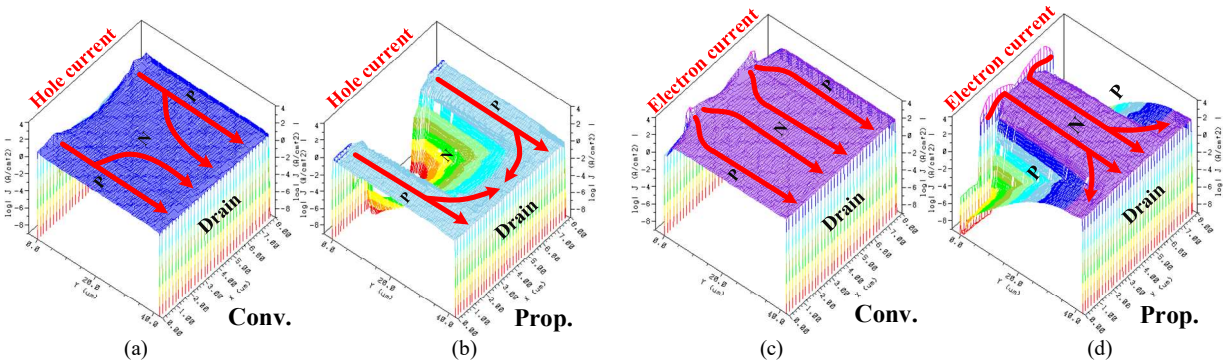



Fig. 4. (a) Reverse conduction curves with $V_{GS}$ = 0 V. (b) Minority carrier distributions along the depth of N-pillar at $I_{DS}$ = -100 A/$cm^2$ and $V_{GS}$ = 0 V.

Fig. 4(a) depicts the reverse conduction characteristics, where a higher reverse conduction voltage ($V_F$) at $I_{DS}$ = - 100 A/$cm^2$ and $V_{GS}$= 0 V is observed for the proposed SJ-MOSFET. This is firstly due to the high reverse turn-on voltage to form the electron accumulation layers. Secondly, the proposed device exhibits a quasi-unipolar conduction characteristic because nearly all of the reverse

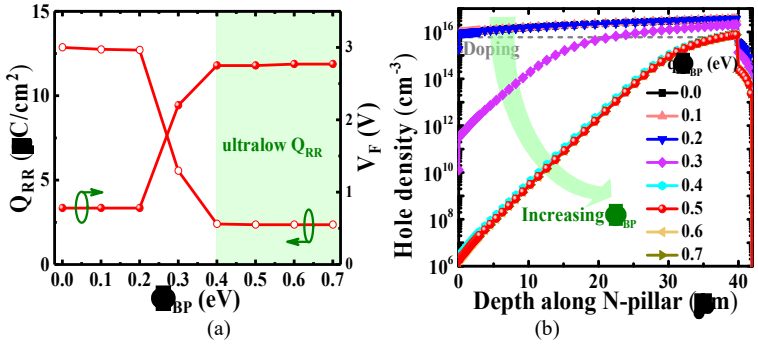



(a) (b) (c) (d)

Fig. 5. The 3D hole current density distributions in reverse conduction state of (a) Conv-SJ-MOSFET and (b) proposed SJ-MOSFET. The 3D electron current density distributions in reverse conduction state of (c) Conv-SJ-MOSFET and (d) proposed SJ-MOSFET.

current is conducted through the electron accumulation layers. While for the Conv-SJ-MOSFET, a large number of minority carriers are stored in the drift region owing to the conduction of the body P-N junction diode, which induces a lower $V_F$. The minority carrier distributions in Fig. 4(b) indicate that the proposed SJ-MOSFET exhibits much lower minority carrier density than the Conv-SJ-MOSFET, thus an ultralow $Q_{RR}$ is obtained.

Fig. 5 shows the three-dimensional hole current density and electron current density distributions at $I_{DS}$ = -100 A/cm$^2$ and $V_{GS}$ = 0 V of the two studied SJ-MOSFET. In the proposed SJ-MOSFET, the reverse-biased P-type Schottky diode clamps the potential difference between P-pillar and N-pillar to below 0.7 V at the top of drift region, the conduction of P-pillar/N-pillar junction at the top of drift region is thus prohibited, resulting in an ultralow hole current density in the top of N-pillar and an ultralow electron current density in the top of P-pillar. However, owing to the leakage current of P-type Schottky diode, P-pillar/N-pillar junction turns on near the bottom of drift region, as depicted in Fig. 5(b) and (d). Nevertheless, compared with the Conv-SJ-MOSFET, hole current density of the proposed SJ-MOSFET is dramatically reduced since the injection of hole carrier is suppressed by the reverse-biased P-type Schottky diode as shown in Fig. 5(a) and(b), and all the electron current is conducted through the electron accumulation layers, leading to significantly reduced minority carrier density in the drift region.

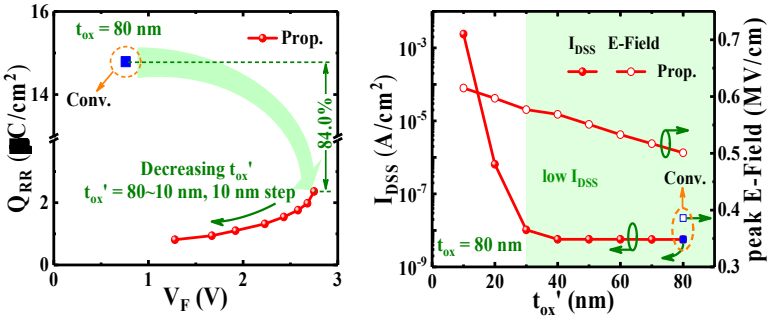



(a) (b)

Fig. 6. (a) Dependences of $Q_{RR}$ and $V_F$ on $\Phi_{BP}$. (b) Dependences of minority carrier distributions on $\Phi_{BP}$ along depth of N-pillar ($x$ = 4 μm) at $I_{DS}$ = -100 A/cm$^2$ and $V_{GS}$ = 0 V.

The Schottky barrier height to P-base ($\Phi_{BP}$) is critical to reverse recovery performance. Fig. 6(a) shows that ultralow $Q_{RR}$ and relatively high $V_F$ are obtained when $\Phi_{BP}$ is higher than 0.4 eV. A higher $\Phi_{BP}$ is more effective to reduce the current component $I_{PN}$ by lowering the leakage current of the reverse-biased P-type Schottky diode, and consequently leads to a better reverse recovery. Fig. 6(b) depicts the dependences of minority carrier distributions on $\Phi_{BP}$. The minority carrier density along the depth of N-pillar is sufficiently low when $\Phi_{BP}$ is higher than 0.4 eV, leading to an ultralow $Q_{RR}$. An optimized 0.5 eV is used in this study due to its excellent reverse recovery characteristic and process feasibility [16].

Fig. 7(a) shows the tradeoff relationship between $V_F$ and $Q_{RR}$ with varying oxide thickness of the source field-plate $t_{ox}'$. A smaller $t_{ox}'$ induces a lower reverse turn-on voltage, which increases the current component $I_{M2}$ and decreases the current components $I_{PN}$, leading to both lower $V_F$ and $Q_{RR}$. Thus, the tradeoff relationship between $V_F$ and $Q_{RR}$ in the proposed SJ-MOSFET could be significantly improved by decreasing $t_{ox}'$. On the other hand, Fig. 7(b) shows that a smaller $t_{ox}'$ induces a higher peak electric field in the oxide and a larger forward leakage current ($I_{DSS}$), which is detrimental to the long-term reliability of the device. With $t_{ox}'$ larger




(a) (b)

Fig. 7. (a) Tradeoff relationships between $Q_{RR}$ and $V_F$ with varying $t_{ox}'$. (b) $I_{DSS}$ and peak electric field (E-Field) in the oxide with varying $t_{ox}'$ at $V_{DS}$ = 400 V and $V_{GS}$ = 0 V.

than 30 nm, the $I_{DSS}$ and peak electric field in the oxide of the proposed SJ-MOSFET is close to those of the Conv-SJ-MOSFET, so $t_{ox}'$ larger than 30 nm is preferred. Additional process steps need to be introduced if $t_{ox}'$ is different from $t_{ox}$, thus in this study, the proposed SJ-MOSFET has identical $t_{ox}'$ and $t_{ox}$ of 80 nm, whose $Q_{RR}$ is still 84.0% lower than that of the Conv-SJ-MOSFET as labeled in Fig. 7(a).

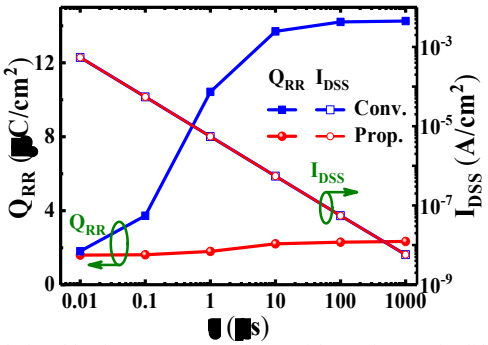
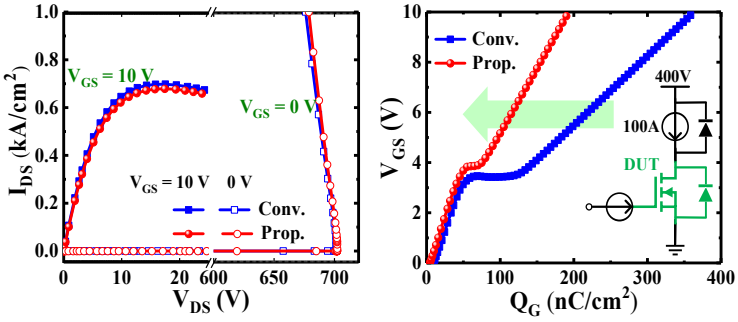



Fig. 8. Tradeoff relationships between $Q_{RR}$ and $I_{DSS}$ with varying carrier lifetime (τ).

The influence of carrier lifetime (τ) on $Q_{RR}$ and $I_{DSS}$ is depicted in Fig. 8. Obviously, the reduced τ leads to a decreased $Q_{RR}$. Nevertheless, the reduced τ also results in the augment of the $I_{DSS}$. Hence, there is a trade-off between $Q_{RR}$ and $I_{DSS}$. Besides, lifetime killing process causes the degradation of ON-resistance, contamination and aging problems [6-8]. Thus, the proposed SJ-MOSFET with ultralow $Q_{RR}$ and no additional carrier lifetime killing process is a candidate for replacement.




(a) (b)

Fig. 9. (a) Forward I-V characteristics. (b) Gate charge characteristics and the inset is test circuit, where each device has an area of 1 cm².

The forward I-V characteristics are shown in Fig. 9(a). Similar static avalanche breakdown characteristics are observed between the two studied devices. Since the forward voltage is supported by the PN junction in the drift region, the introduction of P-base Schottky contact has no impact on the forward leakage current. The specific ON-resistance ($R_{ON}$) of the proposed SJ-MOSFET is 8.55 mΩ•cm² (at $I_{DS}$ = 100 A/cm² and $V_{GS}$ = 10 V). Since the channel resistance plays a small part on the $R_{ON}$ for 600 V class MOSFET [1], the decreased channel density accounts for 5.3% increases in $R_{ON}$ compared to that of Conv-SJ-MOSFET (8.12 mΩ•cm²). The slight degradation of $R_{ON}$ is justified by the significant benefits obtained in other characteristics. Better gate charge characteristics of the proposed SJ-MOSFET can be achieved as depicted in Fig. 10(b). Gate charge ($Q_G$) and gate to drain charge ($Q_{GD}$) of the proposed SJ-MOSFET are 185 nC/cm² and 18 nC/cm², respectively, which are much superior to those of the Conv-SJ-MOSFET ($Q_G$ = 352

nC/cm$^2$ and $Q_{GD}$ = 53 nC/cm$^2$), reducing by 47.4% and 66.0%, respectively. The reduced gate electrode area accounts for this improvement [17-19]. Consequently, compared with the Conv-SJ-MOSFET, the proposed SJ-MOSFET achieves much better figures of merit including 44.7% lower $Q_G$ • $R_{ON}$ and 64.2% lower $Q_{GD}$ • $R_{ON}$, which is conducive to improving the switching performance.

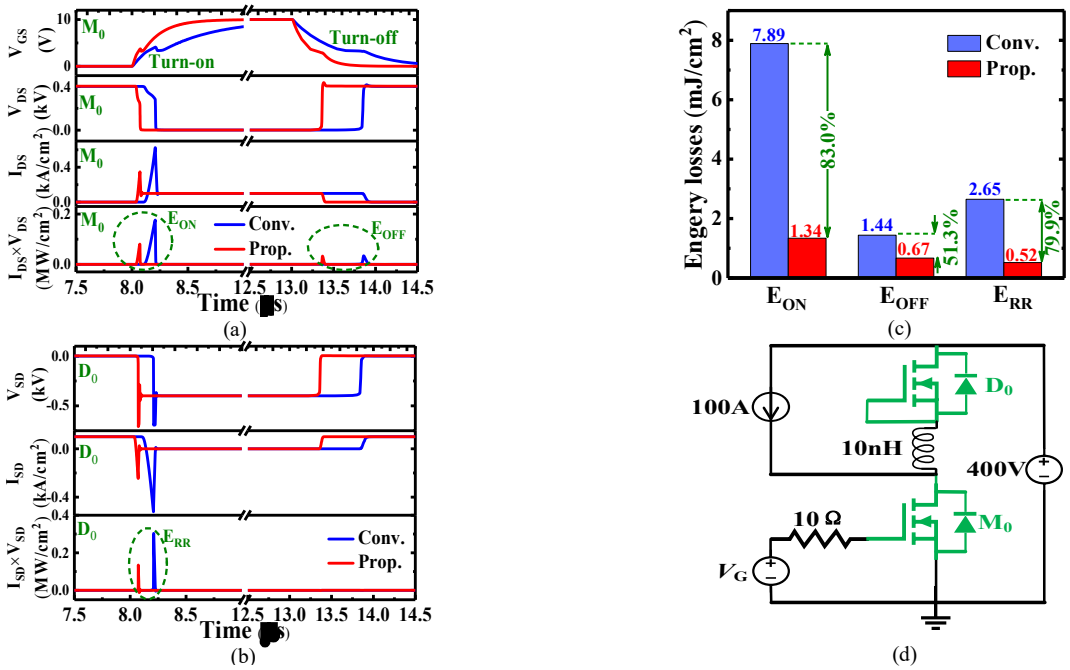



Fig. 10. Switching waveforms of (a) $M_0$ and (b) $D_0$, and the equivalent (c) switching losses and (d) test circuit configuration, where two Conv-SJ-MOSFETs or proposed SJ-MOSFETs are used as both bottom switch $M_0$ and top switch $D_0$.

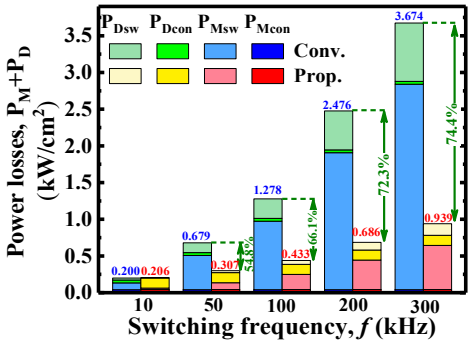



Fig. 11. Dependences of total power losses on the switching frequency ($f$), where duty cycle ($d$) of 0.5 is assumed, $P_{Dsw}$ and $P_{Msw}$ are the switching losses of $D_0$ and $M_0$, respectively, and $P_{Dcon}$ and $P_{Mcon}$ are the conduction losses of $D_0$ and $M_0$, respectively.

The switching characteristics of the two studied devices in the half-bridge circuit application are investigated as shown in Fig. 10(a) and (b), the equivalent switching losses are shown in Fig. 10(c) and the test circuit is shown in Fig. 10(d). It is clearly shown that, compared with the Conv-SJ-MOSFET, the turn-on ($E_{ON}$), turn-off ($E_{OFF}$) and reverse recovery ($E_{RR}$) losses of the proposed SJ-MOSFET are reducing by 83.0%, 51.3% and 79.9%, respectively, benefiting from its lower $Q_G$, $Q_{GD}$ and $Q_{RR}$ as shown in Fig. 10(a) and (b). The total power losses of the devices $M_0$ and $D_0$ are composed of the conduction losses and the switching losses, and can be calculated by $P_M = d \times R_{ON} I_D^2 + f \times (E_{ON} + E_{OFF})$ and $P_D = d \times V_F I_D + f \times E_{RR}$, respectively, where $d$ is the duty cycle and $f$ is the switching frequency. The comparison of the total power losses as a function of $f$ between the studied devices is shown in Fig. 11. Owing to the relatively large conduction losses, the total power losses of the proposed SJ-MOSFET are higher than Conv-SJ-MOSFET when $f \leq 10$ kHz. The outstanding switching performance of the proposed SJ-MOSFET becomes appreciable with the augment of $f$. When operating under higher $f$, the total losses of the proposed SJ-MOSFET decreases significantly, reducing by 54.8% ~ 74.4% at 50 kHz ~ 300 kHz with comparison to the Conv-SJ-MOSFET, demonstrating its great potential to boost the operation frequency in power conversion systems, such as uninterruptible power supply (UPS), solar and server [20].

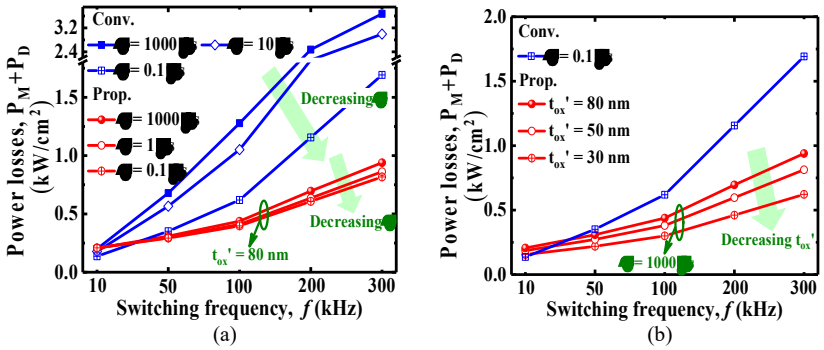



Fig. 12. (a) Dependences of total power losses on the switching frequency with varying τ. (b) Dependences of total power losses on the switching frequency with varying $t_{ox}'$ for the proposed SJ-MOSFET.

By decreasing carrier lifetime τ, the improved reverse recovery performance of both studied SJ-MOSFETs leads to lower power losses, as depicted in Fig. 12(a). The decreased τ results in significant improvement of the Conv-SJ-MOSFET, nevertheless, its total power losses is still higher than that of the proposed SJ-MOSFET at high *f*. For the proposed SJ-MOSFET, decreasing $t_{ox}'$ is a better choice to achieve lower power losses. The decreased $t_{ox}'$ results in both lower $Q_{RR}$ and $V_F$, thus the improvement is more pronounced as shown in Fig. 12(b).

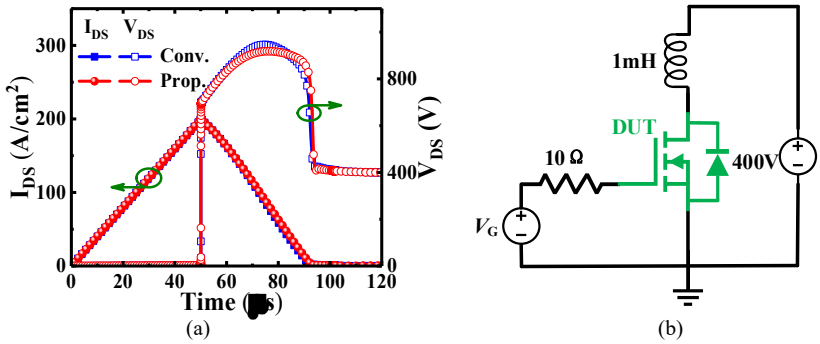



Fig.13. (a) Simulated current and voltage waveforms during the UIS state. (b) Test circuit configuration for the UIS characteristics, where $V_G$ is 10 V to 0 V.

During the operation of SJ-MOSFET, the conduction of the parasitic NPN transistor ($N^+$ source/P-base/ N-pillar) should be completely suppressed. The parasitic NPN transistor may turn on in reverse recovery state or unclamped inductive switching (UIS) state. In the proposed SJ-MOSFET, the reverse recovery current is dramatically reduced, and nearly all of it is majority carrier current, thus it is difficult for the parasitic NPN transistor to be triggered in the reverse recovery state. Besides, with the implementation of a highly doped buried $P^+$ layer in the P-base of the proposed SJ-MOSFET, a similar static avalanche breakdown current between the two studied SJ-MOSFETs is obtained as shown in Fig. 9(a). This results in a similar UIS characteristic between the two studied SJ-MOSFETs as shown in Fig. 13, where the parasitic NPN transistor is not triggered when the avalanche current is up to 200 A/cm$^2$.

## IV. Conclusion

An ultralow reverse recovery charge and low switching loss SJ-MOSFET with P-type Schottky diode and source field-plate is proposed and demonstrated by numerical simulations. The simulation results show that the introduction of P-type Schottky diode is effective in preventing the conduction of body P-N junction diode, simultaneously, the electron accumulation layer formed under the source field-plate providing a path for reverse current. As a result, compared with the Conv-SJ-MOSFET, the injection of minority carrier is dramatically reduced and up to 84.0% reduction in the $Q_{RR}$ is achieved. Besides, the introduction of source field-plate accounts for the significantly reduced gate charge of the proposed SJ-MOSFET. Hence, benefiting from its lower $Q_{RR}$, $Q_G$ and $Q_{GD}$, the proposed SJ-MOSFET shows an overall improvement in switching losses. The proposed device also exhibits similar specific ON-resistance, static breakdown voltage and dynamic avalanche breakdown. As a result, the proposed SJ-MOSFET shows its great potential used in power conversion systems.

## DECLATATIONS

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# Figures

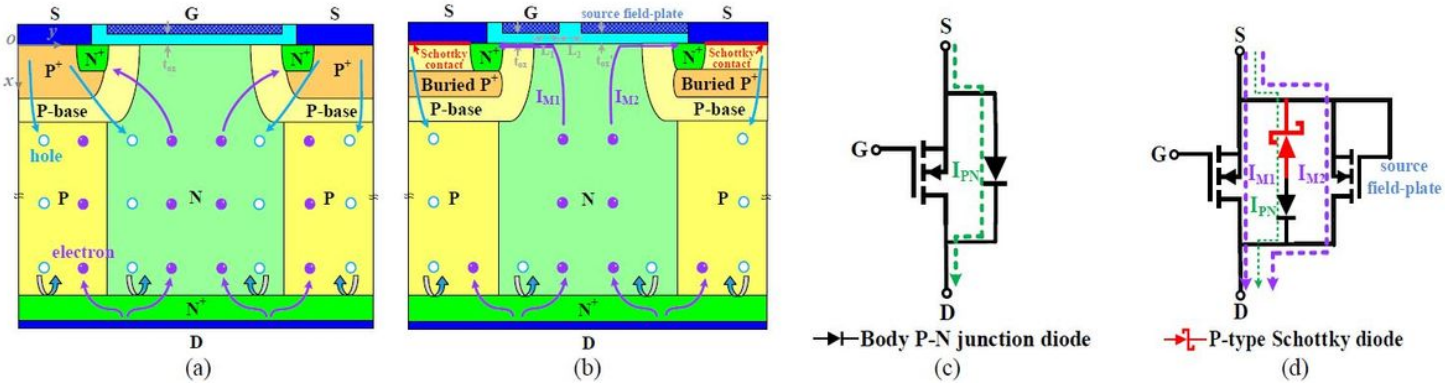



**Figure 1**

The schematic views of (a) Conv-SJ-MOSFET and (b) proposed SJ-MOSFET. The hole and electron distributions at reverse conduction state with VGS = 0 V are illustrated. The simplified circuits of (a) Conv-SJ-MOSFET and (b) proposed SJ-MOSFET. The dashed lines show the components of current in reverse conduction state with VGS = 0 V.

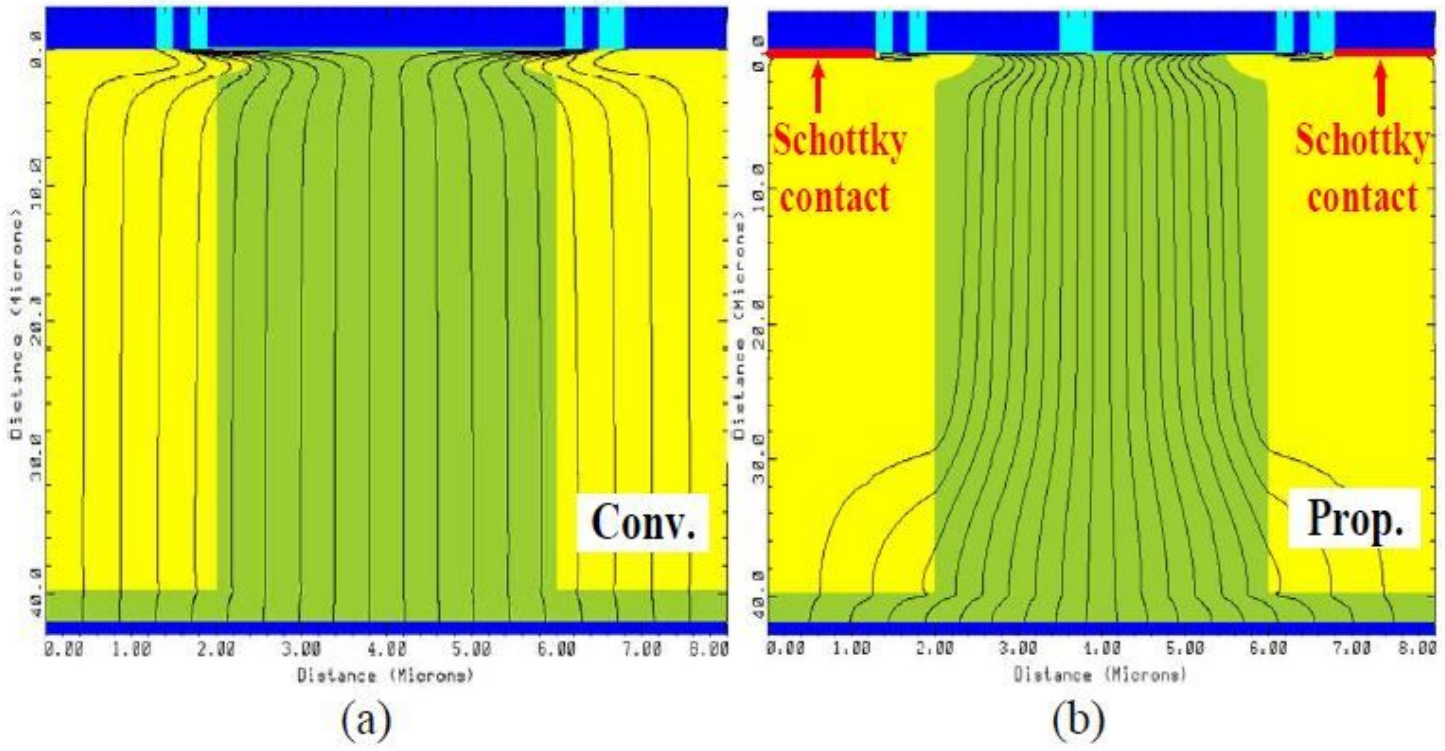



**Figure 2**

The distributions of current at IDS = - 100 A/cm2 and VGS = 0 V of (a) Conv-SJ-MOSFET and (b) proposed SJ-MOSFET. In the proposed SJMOSFET, electron accumulation layers are formed under both source field-plate and gate with VGS = 0 V.

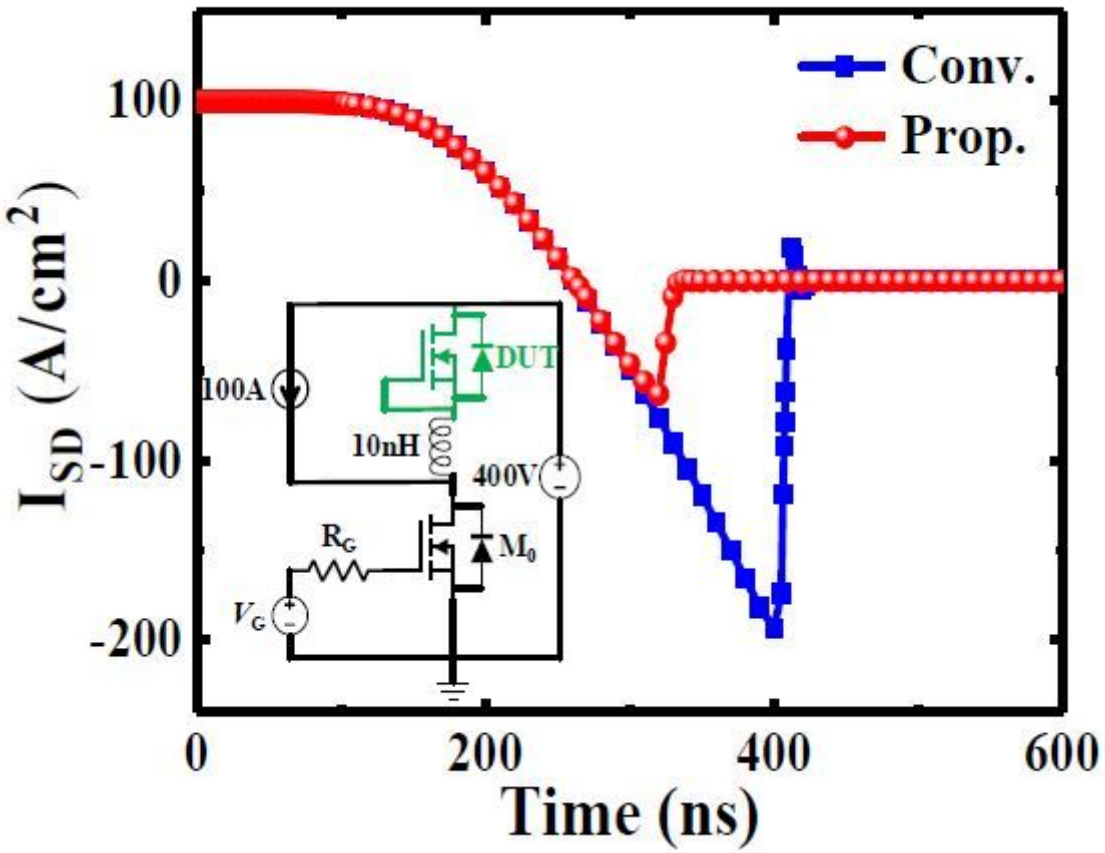



Figure 3

Simulated reverse recovery characteristics. The inset is the test circuit configuration, where each device has an area of 1 cm2, VG is 0 V to 10 V and the current communication rate di/dt is set to 1250 A/(cm2 • μs).

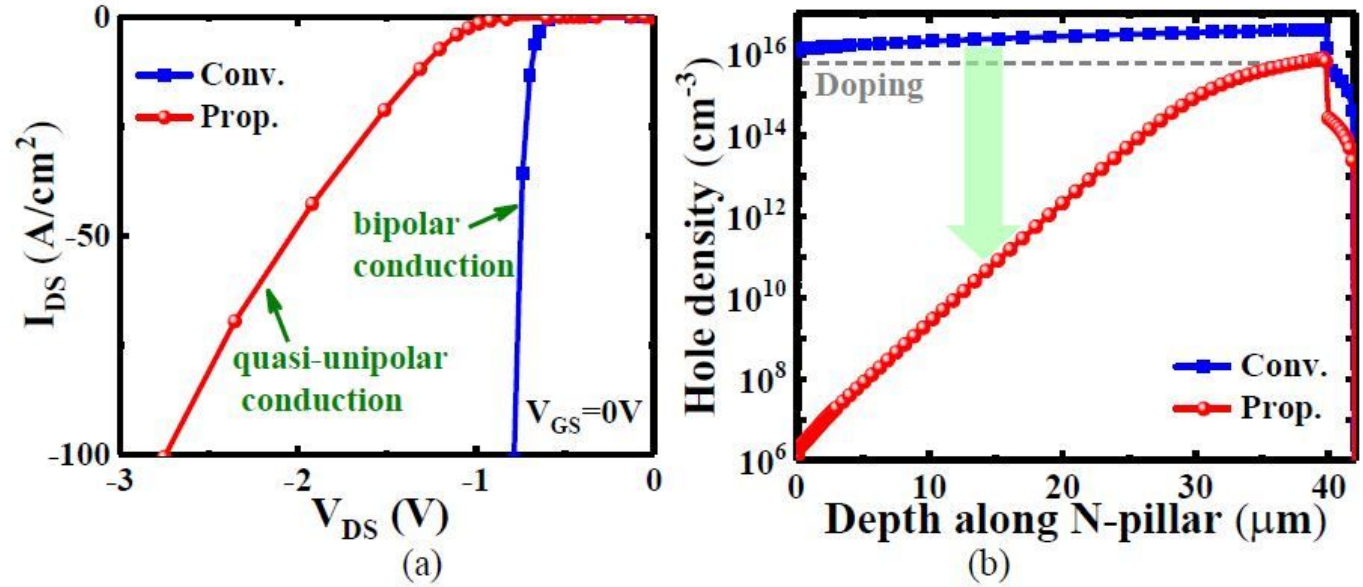



Figure 4

(a) Reverse conduction curves with VGS = 0 V. (b) Minority carrier distributions along the depth of N-pillar at IDS = -100 A/cm2 and VGS = 0 V.

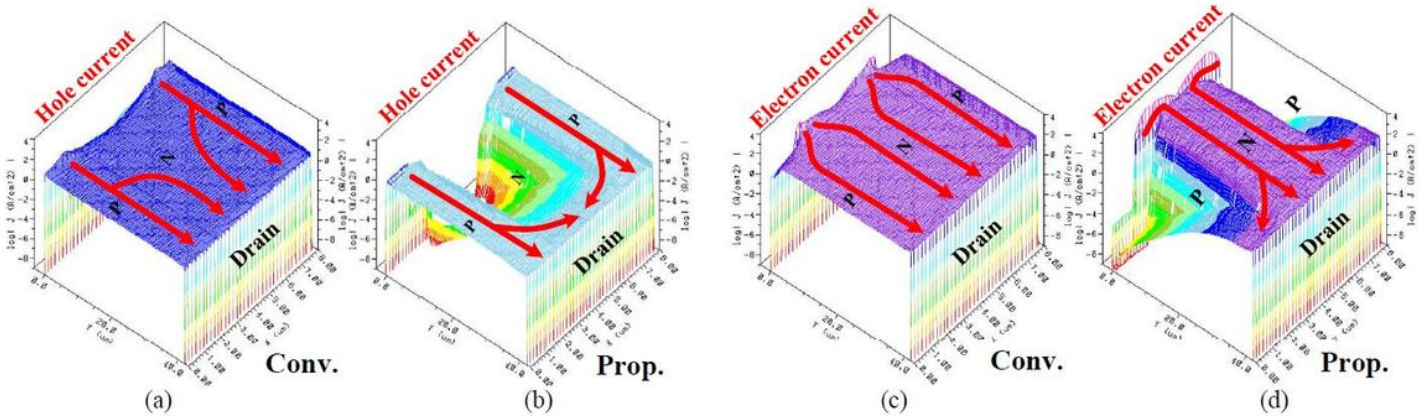



**Figure 5**

The 3D hole current density distributions in reverse conduction state of (a) Conv-SJ-MOSFET and (b) proposed SJ-MOSFET. The 3D electron current density distributions in reverse conduction state of (c) Conv-SJ-MOSFET and (d) proposed SJ-MOSFET.

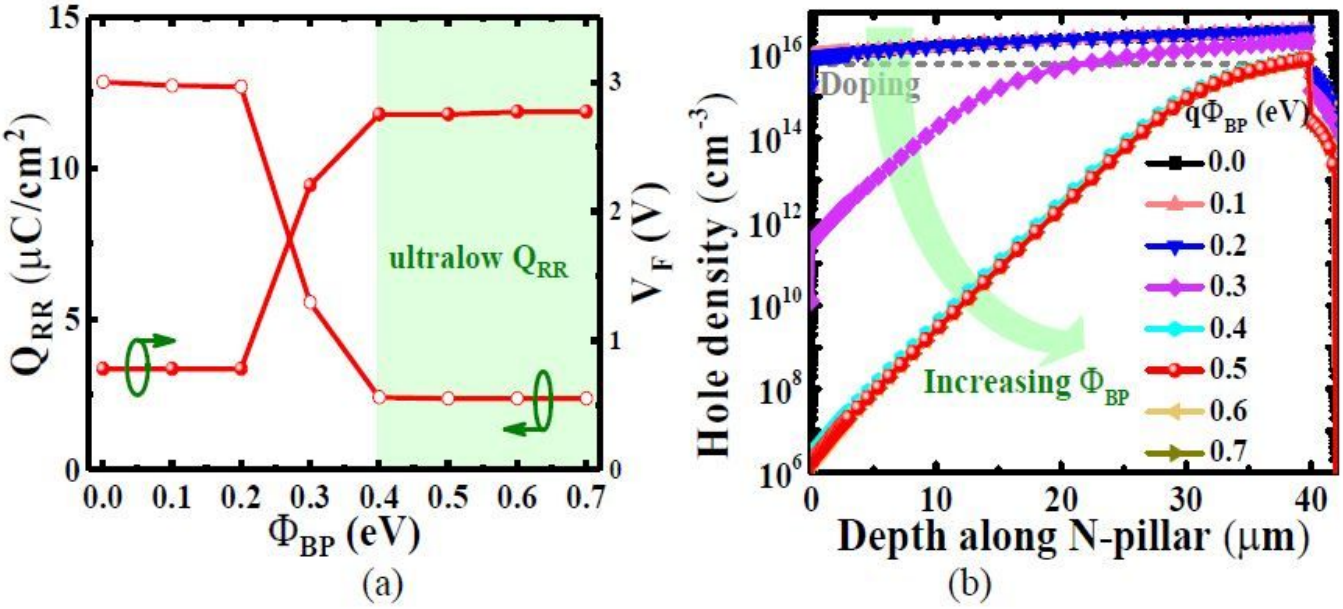



**Figure 6**

(a) Dependences of QRR and VF on ΦBP. (b) Dependences of minority carrier distributions on ΦBP along depth of N-pillar (x = 4 □m) at IDS = - 100 A/cm2 and VGS = 0 V.

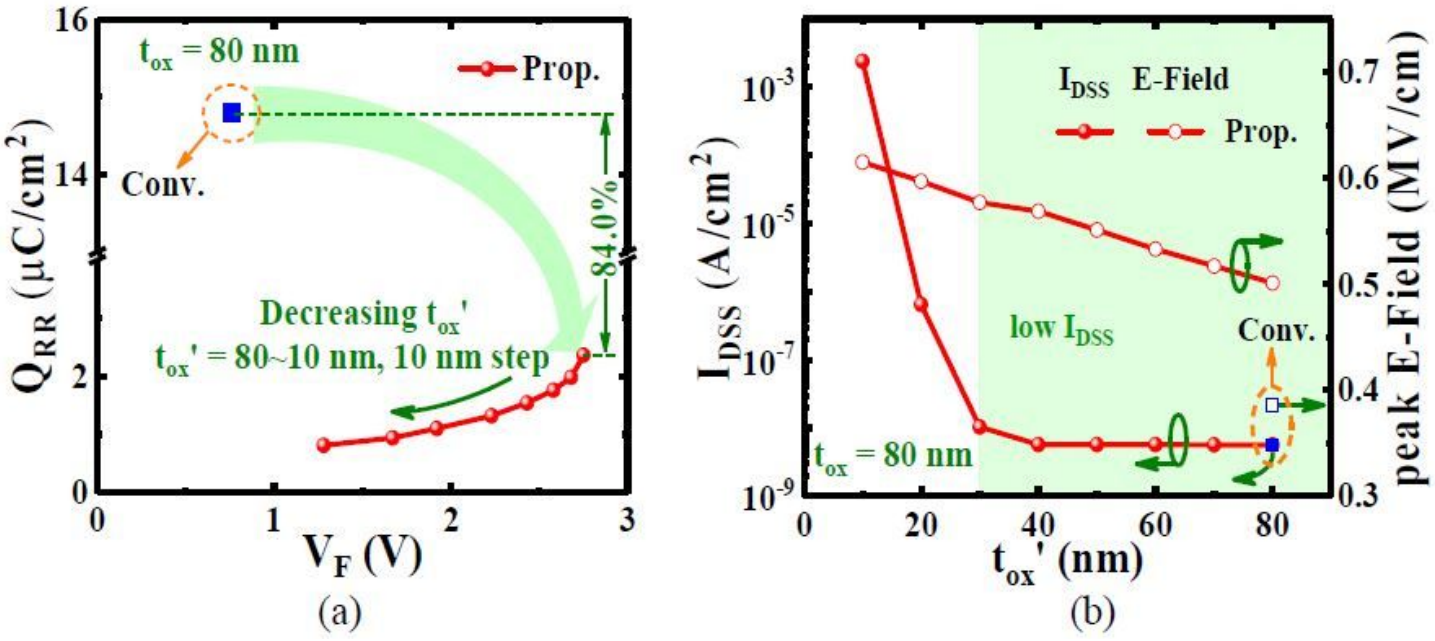



Figure 7

(a) Tradeoff relationships between QRR and VF with varying tox'. (b) IDSS and peak electric field (E-Field) in the oxide with varying tox' at VDS = 400 V and VGS = 0 V.

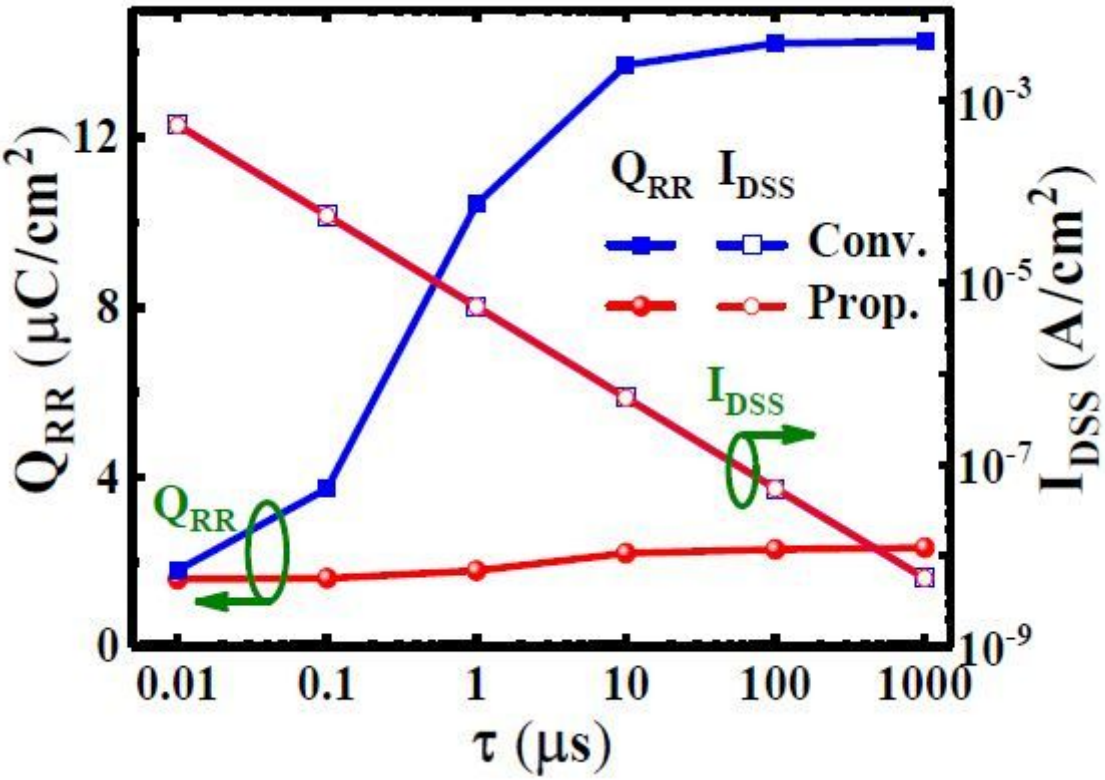



Figure 8

Tradeoff relationships between QRR and IDSS with varying carrier lifetime (τ).

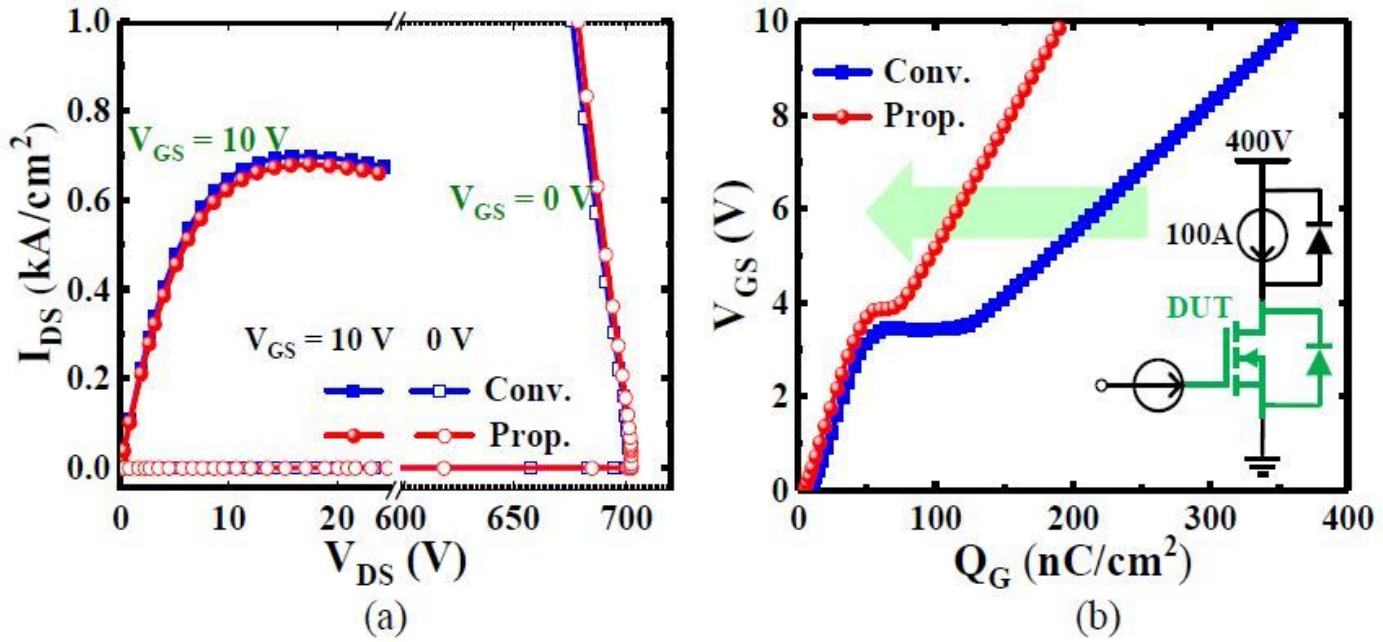



Figure 9

(a) Forward I-V characteristics. (b) Gate charge characteristics and the inset is test circuit, where each device has an area of 1 cm2.

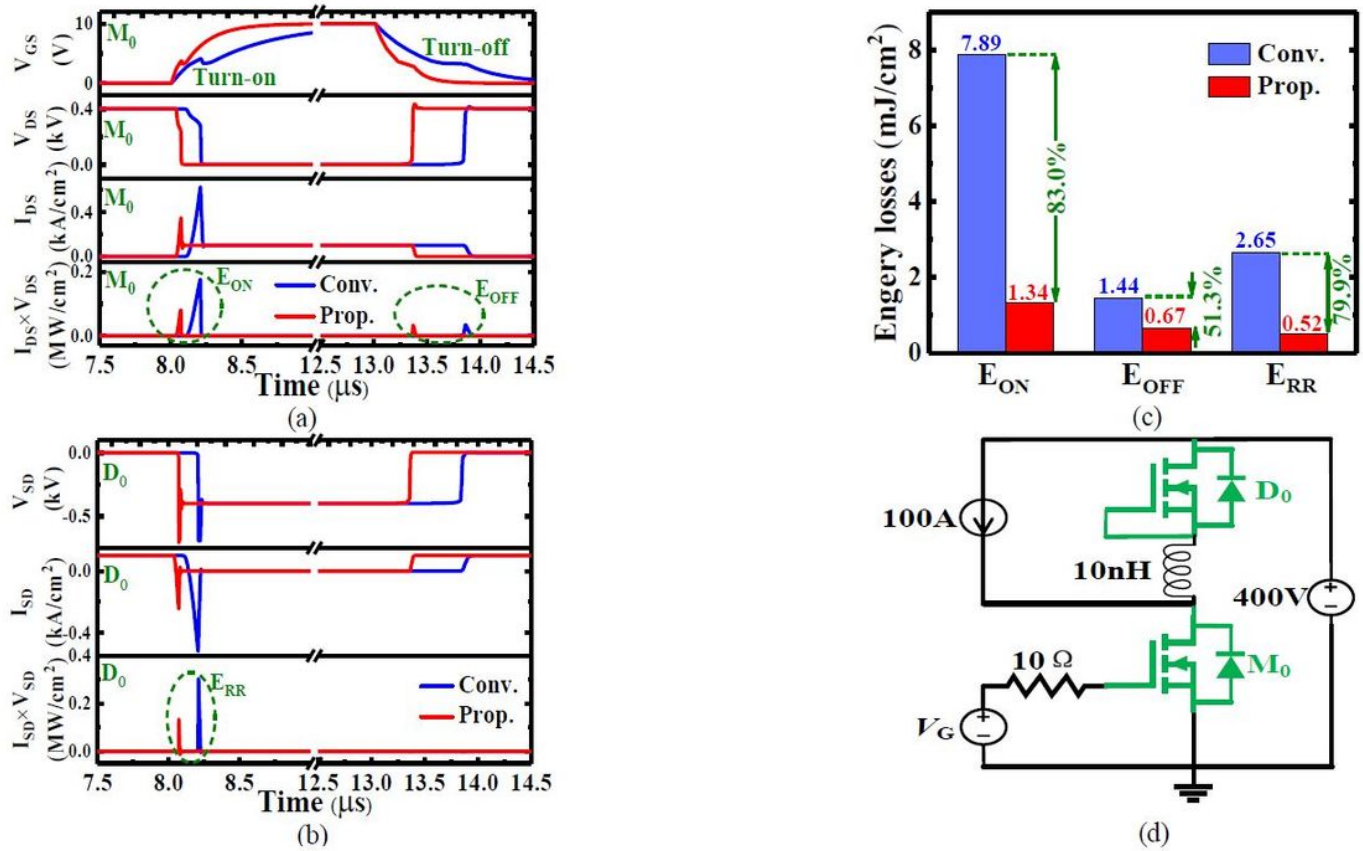



Figure 10

Switching waveforms of (a) M0 and (b) D0, and the equivalent (c) switching losses and (d) test circuit configuration, where two Conv-SJMOSFETs or proposed SJ-MOSFETs are used as both bottom switch M0 and top switch D0.

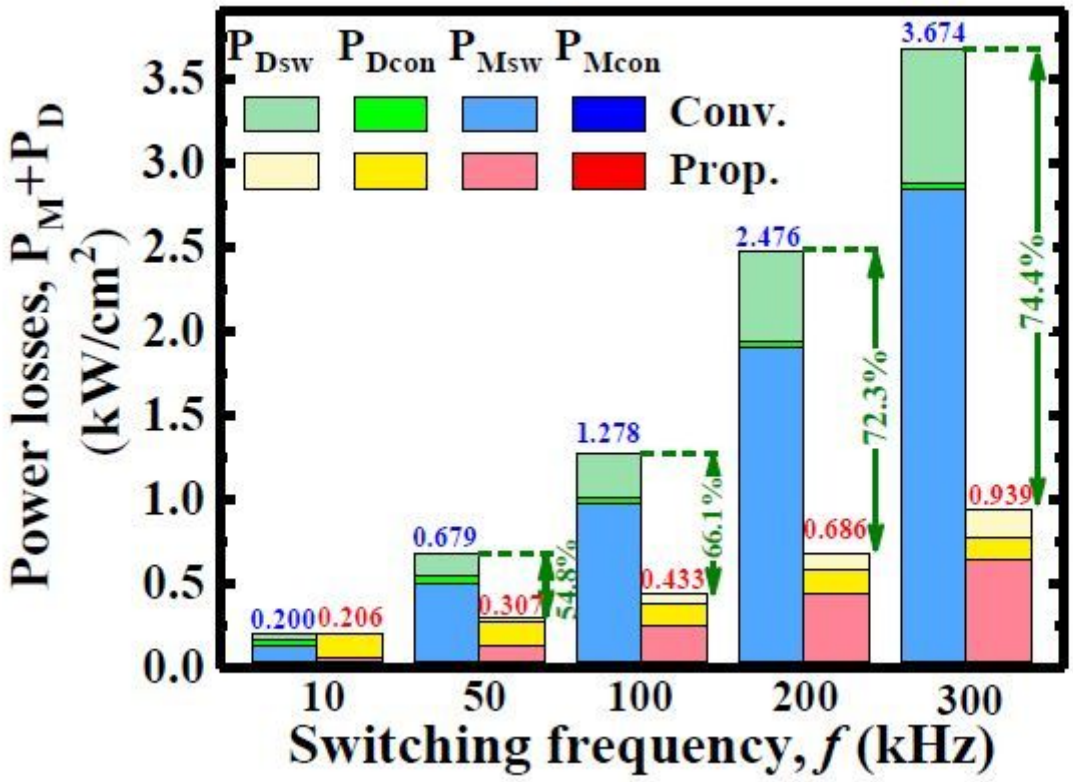
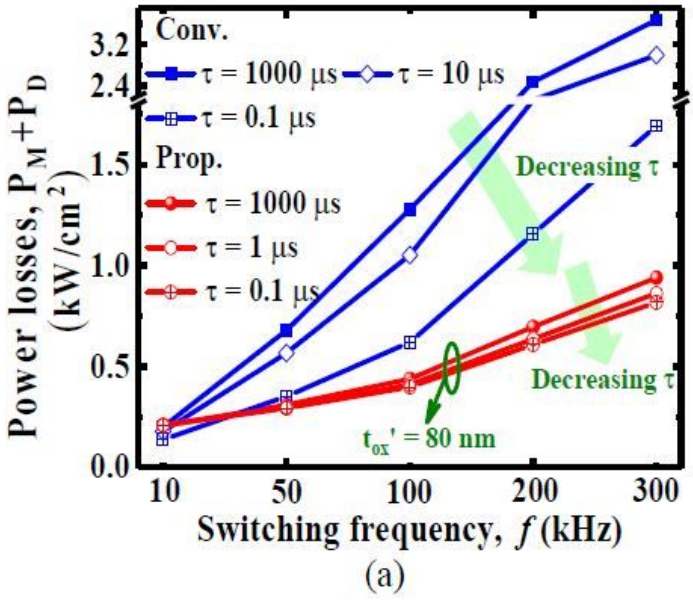



Figure 11

Dependences of total power losses on the switching frequency (f), where duty cycle (d) of 0.5 is assumed, PDsw and PMsw are the switching losses of D0 and M0, respectively, and PDcon and PMcon are the conduction losses of D0 and M0, respectively.



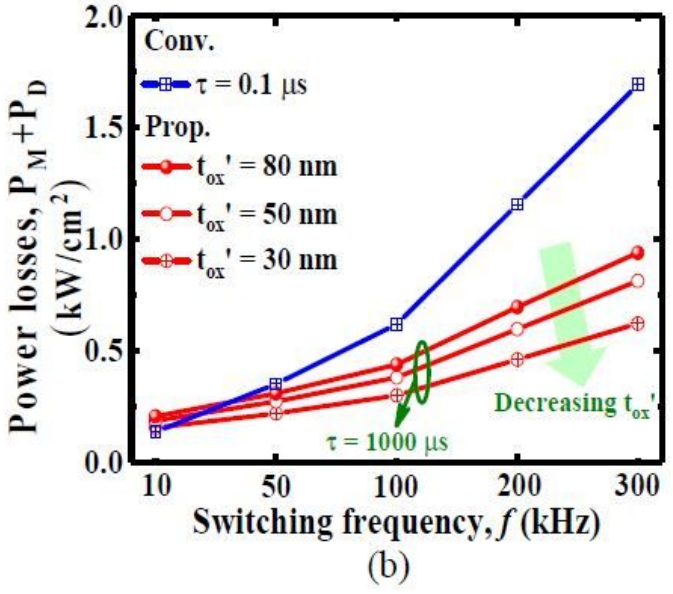



Figure 12

(a) Dependences of total power losses on the switching frequency with varying τ. (b) Dependences of total power losses on the switching frequency with varying tox' for the proposed SJ-MOSFET.

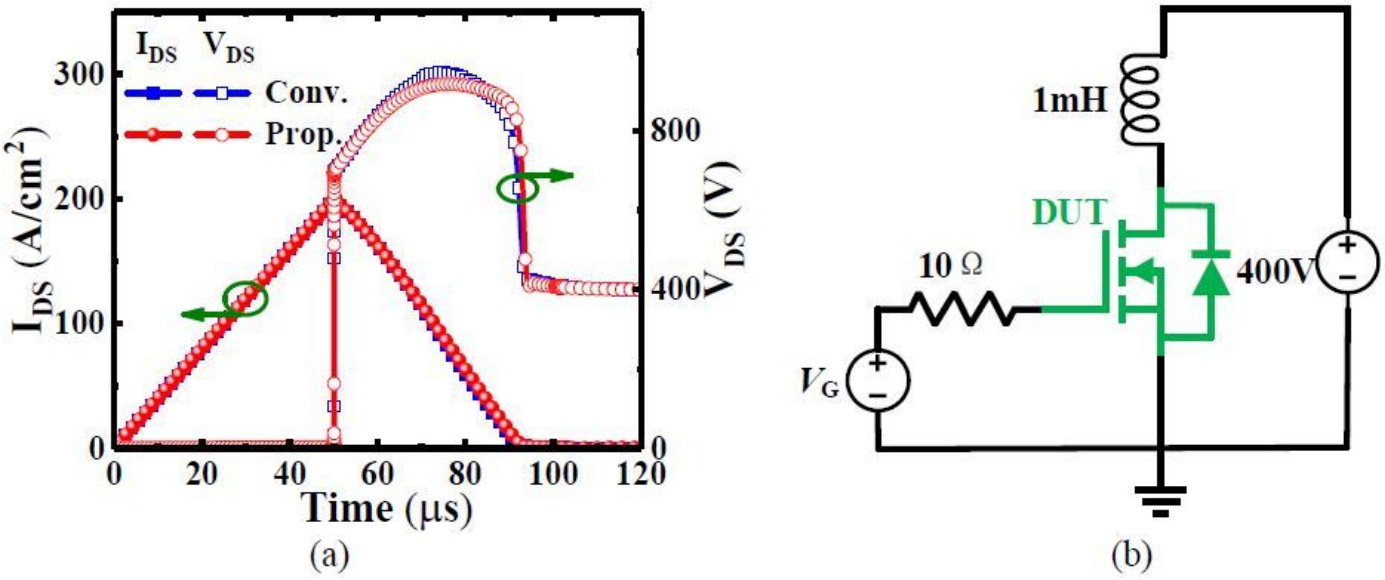



Figure 13

(a) Simulated current and voltage waveforms during the UIS state. (b) Test circuit configuration for the UIS characteristics, where VG is 10 V to 0 V.