Implementation of Low Voltage MOSFET and Power LDMOS on InGaAs

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Research Article

Abstract

In this paper, a new low voltage MOSFET (LV MOSFET) and high voltage dual-gate MOSFET (HV DG MOSFET) have been proposed with concept of integration based on trench technology on InGaAs material. Junction isolation technique is used for the implementation of a low voltage MOSFET and a high power dual gate MOSFET in same InGaAs epitaxial layer side by side. The HV DG MOSFET consists of dual gate that are placed in drift region under the oxide-filled trenches. The proposed structure minimize on-resistance (R_{on}) along with increased breakdown voltage (V_{br}) due to enhanced RESURF effect, the creation of dual channels, and due to folding technique of drift region in vertical direction. In the HV DG MOSFET, the drain current (I_D) increases leading to enhanced transconductance (gm) by simultaneous conduction of channels with improved maximum oscillation frequency (f_{max}) and cut-off frequency (f_t). On the other side, the low voltage MOSFET consists of a gate placed in a centre of the structure within an oxide trench to create two n-channels in the p-base. The two channels are conducting in parallel and give substantial enhancement in peak g_m, I_D, f_{max} and f_t with more control over the short channel parameters. The design and performance analysis of low voltage MOSFET (LV MOSFET) and high voltage dual-gate MOSFET (HV DG MOSFET) are carried out on 2-D ATLAS device simulator.

1. Introduction

The low voltage analog and digital circuits are integrated with power devices results in the development of smart power integrated circuits (PICs). The smart PICs are used in various applications such as, automotive electronics, industrial control circuits, personal communication systems programmable logic circuits, portable power management systems, etc. Nowadays, the energy resources are limited so that the requirement of such PICs which consumes less energy, and fulfilled the manufacturing and economic constraints with efficient, rugged and reliable features. However, to fulfil the demand of energy efficiency, there is a requirement of effective power MOSFETs which delivers the enormous amount of power without consuming a substantial part of it [1–3]. Among several possible options, a discrete power device with trench gate structure is more effective suitable for low voltage analog/digital and RF applications due to lower value of on-state resistance as compared to any other architecture with same specifications [4, 5].

A trench gate MOSFET is having a unique feature it conducts the current vertically from one surface to another surface in order to attain a high drive capability which is considerable for making a complete chip [6–9]. A trench based MOS cell consists of body, source, gate, drain, and the channel regions while it exhibits current flow in vertical direction. MOS cells are connected in such a fashion to minimize the value of on-resistance. The design parameters for consideration of a trench based MOSFET are improvement in transconductance, on-state resistance and breakdown voltage [10, 11].

Presently, silicon-on-insulator (SOI) technology is dominantly used for making the RF power integrated circuits (PICs) due to its mature fabrication process with well-studied native oxide in order to get advantage of better reliability, improved performance, low power consumption, and reduction in size,

weight and cost [12-14]. As the silicon (Si) based power electronic devices are approaching their physical limits, new materials are needed to overcome the challenges faced by the mature Si technology [15]. The III-V group compound semiconductors are emerging as the promising channel material for LDMOS due to their outstanding transport properties. High electron mobility material InGaAs is attractive as alternative channel material than Si which can replace silicon in power devices [2, 15, 16]. Therefore, the motive of this paper is to propose the integration of low voltage MOSFET and high power dual-gate MOSFET on emerging InGaAs semiconductor material using trench technology for better performance of the device.

2. Device Structure

Figure 1 illustrates the integration of junction isolated low voltage MOSFET (LV MOSFET) and high voltage dual-gate MOSFET (HV-DG MOSFET). Both the devices are implemented in n-type III-V semiconductor material (i. e. $In_{0.53}Ga_{0.47}As$) using p-type substrate (InP). The proposed junction isolated HV DG MOSFET and LV MOSFET is isolated by using p^+ trench with -1 V reverse bias. In both low voltage as well as high voltage dual-gate MOSFETs, n-channels are formed in p-region vertically and drain electrode is separately connected with source/p-region by oxide (Al_2O_3) filled trenches. The I_D flows through all the channels simultaneously from drain electrode to source electrode.

The HV DG MOSFET consists of stepped-gate structure with unequal oxide thickness t_{ox2} = 0.1 μm, t_{ox1} = 0.85 μm, and t_{ox} = 0.3 μm. The HV DG MOSFET gate length is 0.5 μm and the length of cell pitch is 3 μm with other mentioned lengths are L_1 = 1.35 μm, L_2 = 0.45 μm, L_3 = 0.60 μm. The n-drift region doping (N_d) is 8 x 10^{16} and p-body doping 1.5 x 10^{16} cm^3. The trench depth (t_D) and epitaxial thickness (t_e) are kept 1.6 μm and 2.2 μm, respectively. A positive V_{gs} forms dual channels in p-region with side walls of gate trenches leading to flow of current (I_D). The conduction of channels through both the gates enhances I_D and g_m. The high g_m results in increase of f_{max} and f_t of the HV DG MOSFET.

On the other side of the structure, the LV MOSFET is made with a 1920 nm thick n-type layer ($In_{0.53}Ga_{0.47}As$) and doping concentration of 10^{19} cm^{-3} over p-type substrate. The p-base thickness is 60 nm $In_{0.53}Ga_{0.47}As$ has doping 2 x 10^{18} cm^{-3}, and the thickness of n^+-cap layer is 20 nm $In_{0.53}Ga_{0.47}As$ with doping of 10^{19} cm^{-3}. The n^+-cap layer is used as ohmic source contacts. The gate (TaN) is placed at the centre of structure in an Al_2O_3 trench. There are two channels are formed near to both side walls of the gate when the value of V_{gs} is greater than the threshold voltage. Due to conduction of current in parallel mechanism improves the I_D and g_m.

3. Results And Discussion

The 2-D simulations of proposed structure as junction isolated LV MOSFET and HV DG MOSFET are carried out by choosing CVT Lombardi and Fermi-Dirac models with the help of ATLAS device simulator [17]. The simulations accuracy is determined by comparing the results obtained with existing literature of a MOSFET [18]. Figure 2 describes a good agreement of simulation results with experimental data. In this

study at the interface of InGaAs/Al_2O_3 the incorporated value of an interface trap-charge is 1×10^{12} $eV^{-1}cm^{-2}$. The V-I characteristics of HV DG MOSFET are obtained at various V_{GS} (gate to source voltages) are depicted in Figure 3. The observed value of I_D is 0.086 mA/μm in HV DG MOSFET at V_{DS} (drain to source voltage) of 10 V and V_{GS} of 2 V. At L_G of 60 nm, the V-I characteristics of LV MOSFET at different V_{GS} are shown in Figure 4. At V_{GS}=1 V and V_{DS}=1.6 V, the I_D of LV MOSFET is 0.50 mA/μm due to creation of two channels in p-body.

Figure 5 explains the g_m versus V_{GS} characteristic of the HV DG MOSFET. The transconductance (g_m) basically represents the gain of the MOSFET. The peak value of the g_m for the proposed HV DG MOSFET is 0.102 mS/μm at V_{GS} of 2.5 V due to simultaneous control of I_D by dual gate. On the other side, for LV MOSFET, the maximum value of gm is obtained as 0.998 mS/μm at V_{GS} of 1.25 V as described in Figure 6. The device structure consists of high value of g_m represents their suitability for RF amplifier applications.

The frequency/microwave characteristics (f_{max} and f_t) of the HV DG MOSFET are shown in Figure 7. In the proposed HV DG MOSFET the value of f_t obtained is 3.8 GHz, while f_{max} is found to be 9.75 GHz.

For the LV MOSFET, the frequency characteristics are shown in Figure 8. The value of ft of the low voltage MOSFET is found to be 41 GHz at 0 dB current gain. This is due to the effect of enhanced g_m of the device. The f_{max} value of the proposed LV MOSFET is 132 GHz.

Moreover, at V_{GS} of 0 V, figure 9 shows the breakdown characteristics of the HV DG MOSFET. In this study, the V_{br} is extracted at which I_D exceeds 10^{-9} mA/μm. This characteristic exhibits a high V_{br} of 62 V. This is due to the reduction in the peak value of electric field in the proposed structure.

The dependence of $R_{on,sp}$ and V_{br} on N_d for the HV DG MOSFET is shown in Figure 10. Figure 10 depicted the HV DG MOSFET gives maximum V_{br} (i. e. 62 V) for N_d = 1.5 x 10^{16} cm^{-3} due to RESURF effect (i. e. reduces the peak electric field inside the device). As increases the value of N_d beyond 1.5 x 10^{16} cm^{-3}, the V_{br} decreases due to increases the field lines inside drift region. From figure 11, as the value of N_d increases the $R_{on,sp}$ decreases due to enhancement in drift current. Table 1 shows a performance evaluation of various MOSFETs.

Table 1

A performance comparison of various MOSFETs.

		I_D (mA/µm)	BV (V)	R_{on-sp} (mΩ-mm^2)	g_m (mS/µm)	f_t (GHz)	f_{max} (GHz)	SS (mV/dec)	DIBL (mV/V)
This work	HV DTG MOSFET	0.086	62	51	0.102	3.8	9.75	-	-
	LV MOSFET	0.50	-	-	0.998	41	132	76	115
PICs [19]	HV DTG MOS	0.074	52	51	0.106	4	10.8	-	-
	LV MOS	0.53	-	-	1.03	44	138	78	118
PICs [12]	HV DTDG MOS	-	91	51	-	-	-	-	-
	LV IC	-	-	-	-	-	-	-	-
PICs [11]	HV DT MOS	-	92	36	-	-	-	-	-
	LV IC	-	-	-	-	-	-	-	-

4. Conclusion

In this work, a new integration technique is proposed based on junction isolation of LV MOSFET and HV DG MOSFET for making smart IC on III-V semiconductor material i. e. InGaAs. The architecture of proposed device is based on trench gates form multiple channels conduction in the p-body to obtained higher output current and lower on-state resistance. The enhancement in I_D due to more control of gate also enhances the peak transconductance which improves the microwave characteristics of the proposed structure. In the HV DG MOSFET the obtained value of I_D =0.086 mA/µm, BV=62 V, R_{on-sp}=51 mΩ-mm^2, g_m = 0.102 mS/µm, f_t = 3.8 GHz, and f_{max} = 9.75 GHz. For LV MOSFET the observed value of I_D =0.50 mA/µm, g_m = 0.998 mS/µm, f_t = 41 GHz, f_{max} = 132 GHz with SS=76 mV/dec, and DIBL=115 mV/V. With the help of 2-D analysis in the device simulator, the performance of LV MOSFET and HV DG MOSFET are evaluated and observed that both the devices exhibits better static and dynamic behavior. The proposed integration concept with trench gate technology can be used for making power ICs, high frequency communication systems also used in analog, digital and mixed signal applications.

Declarations

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The authors declare that there is no conflict of interest.

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Yes

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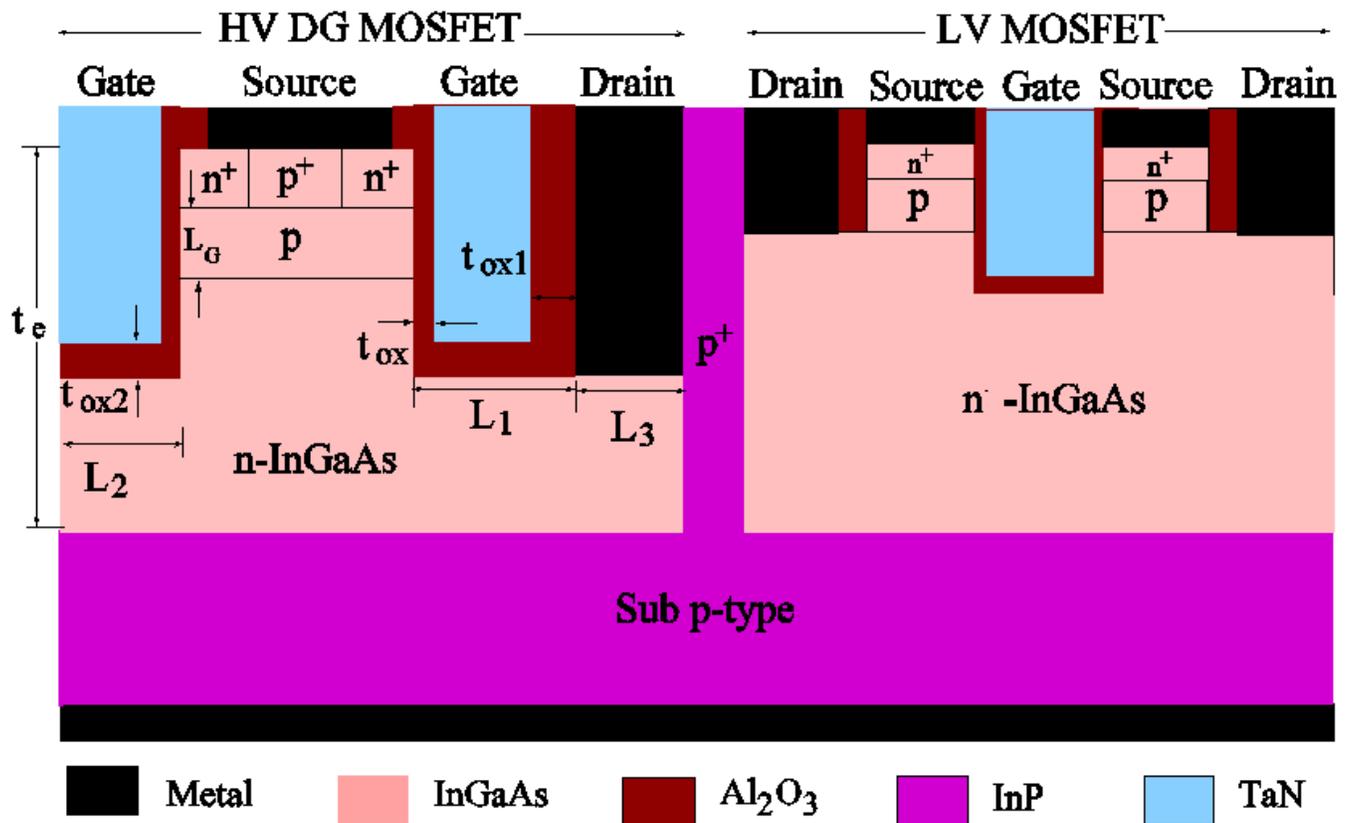
Figures

Figure 1

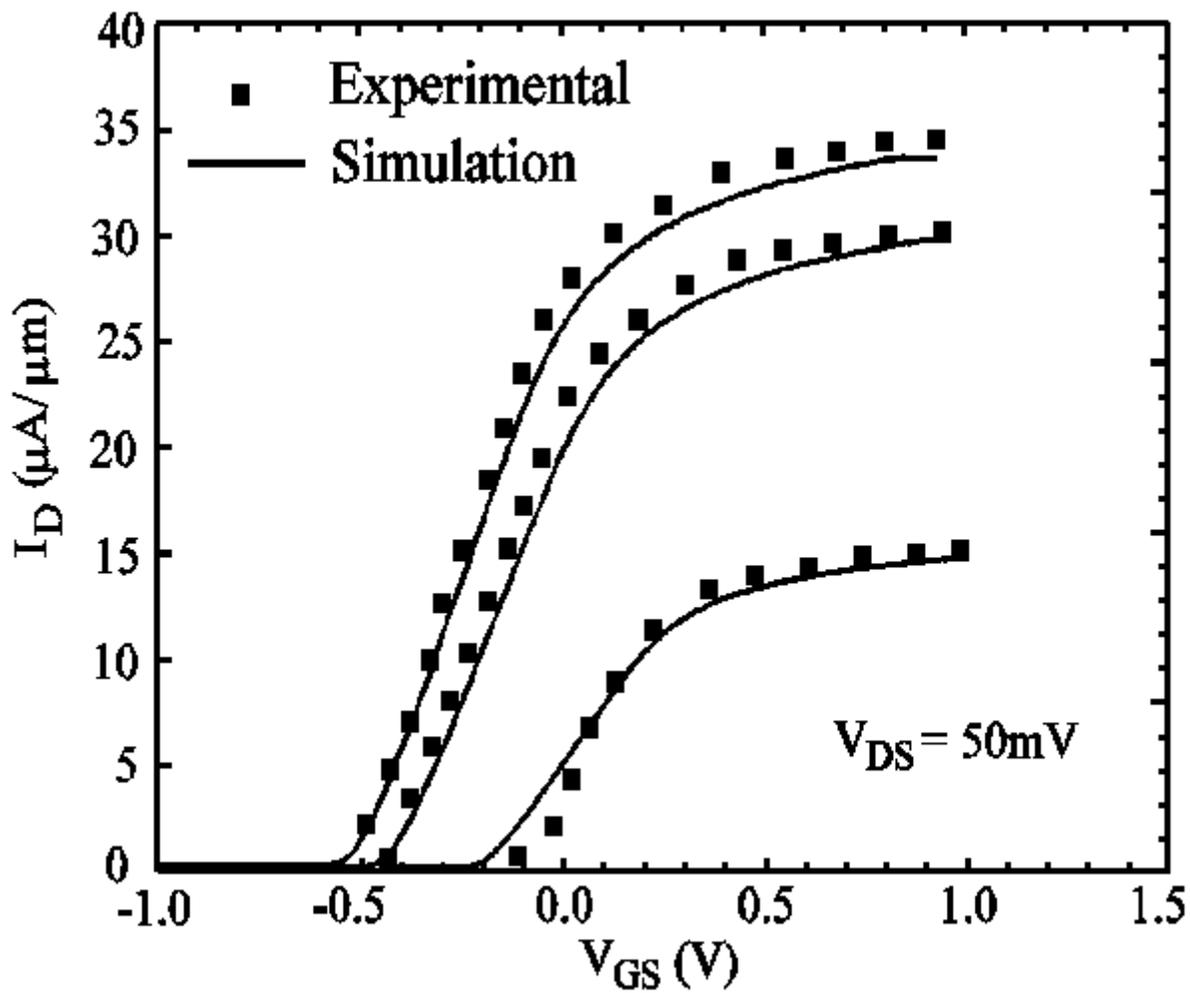Schematic view of the junction isolated HV DG MOSFET and LV MOSFET.
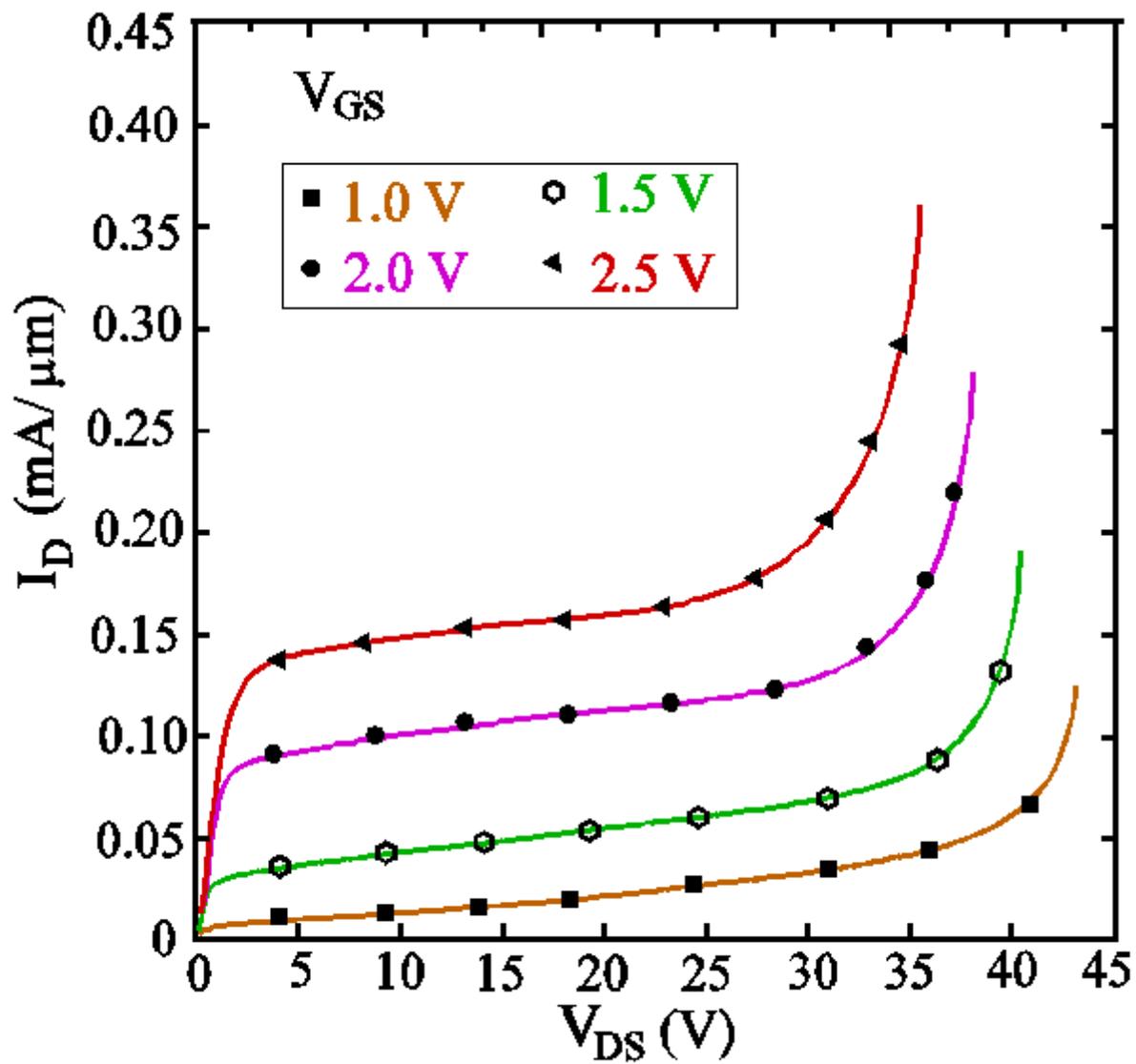
Figure 2

Comparison of transfer characteristics.

Figure 3

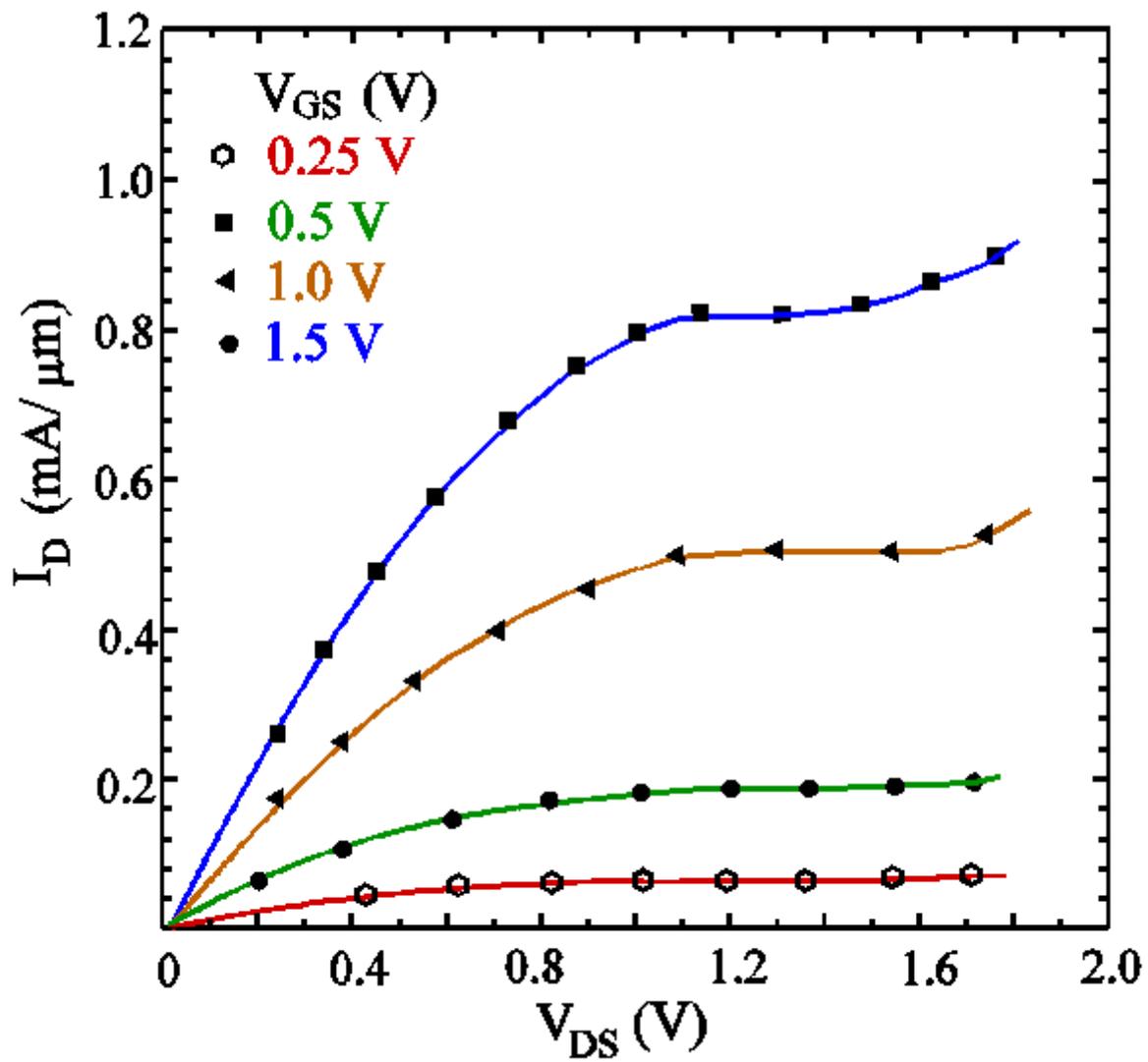ID versus VDS characteristics of the HV DG MOSFET.

Figure 4

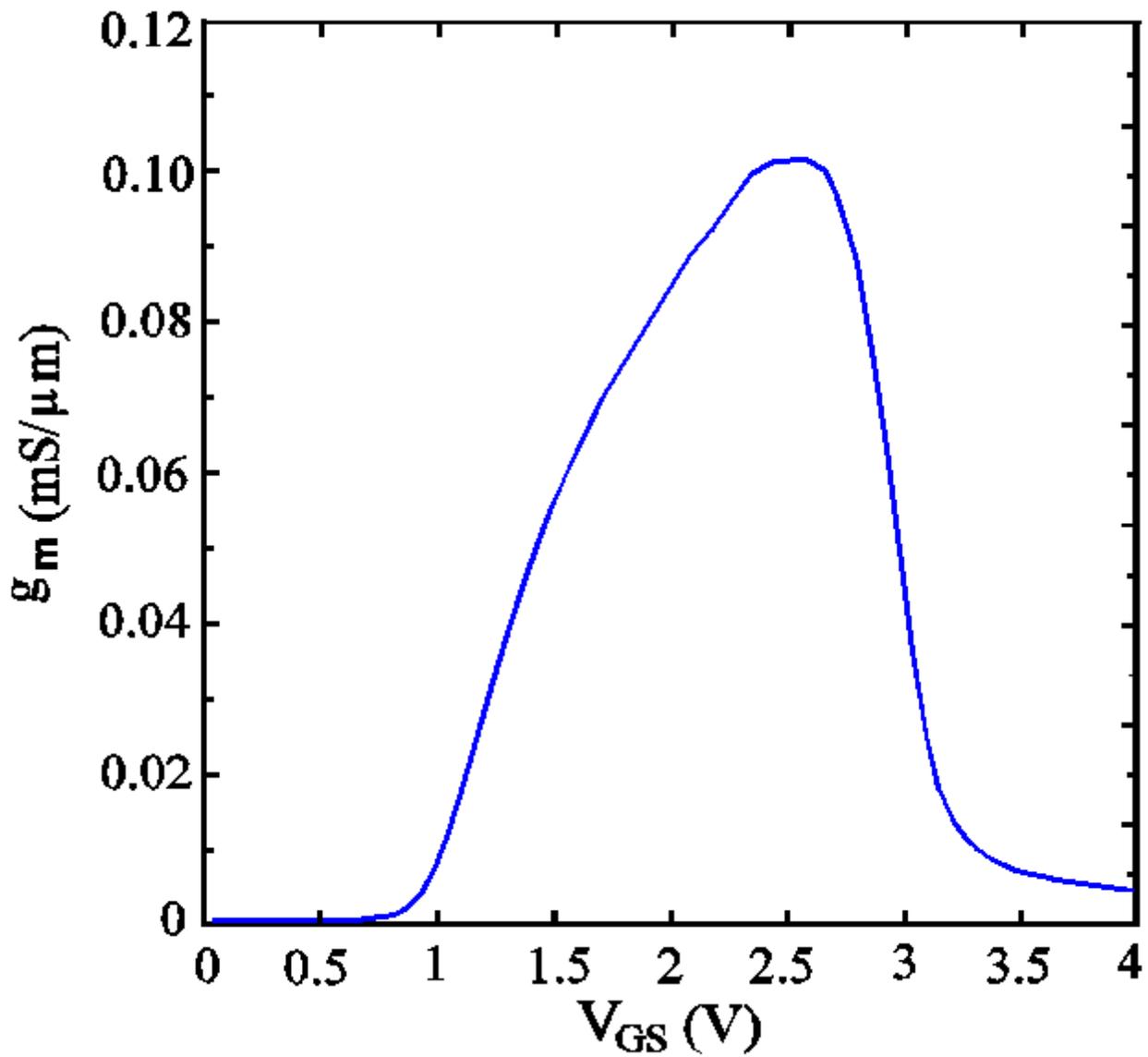ID versus VDS characteristics of the LV MOSFET.

Figure 5

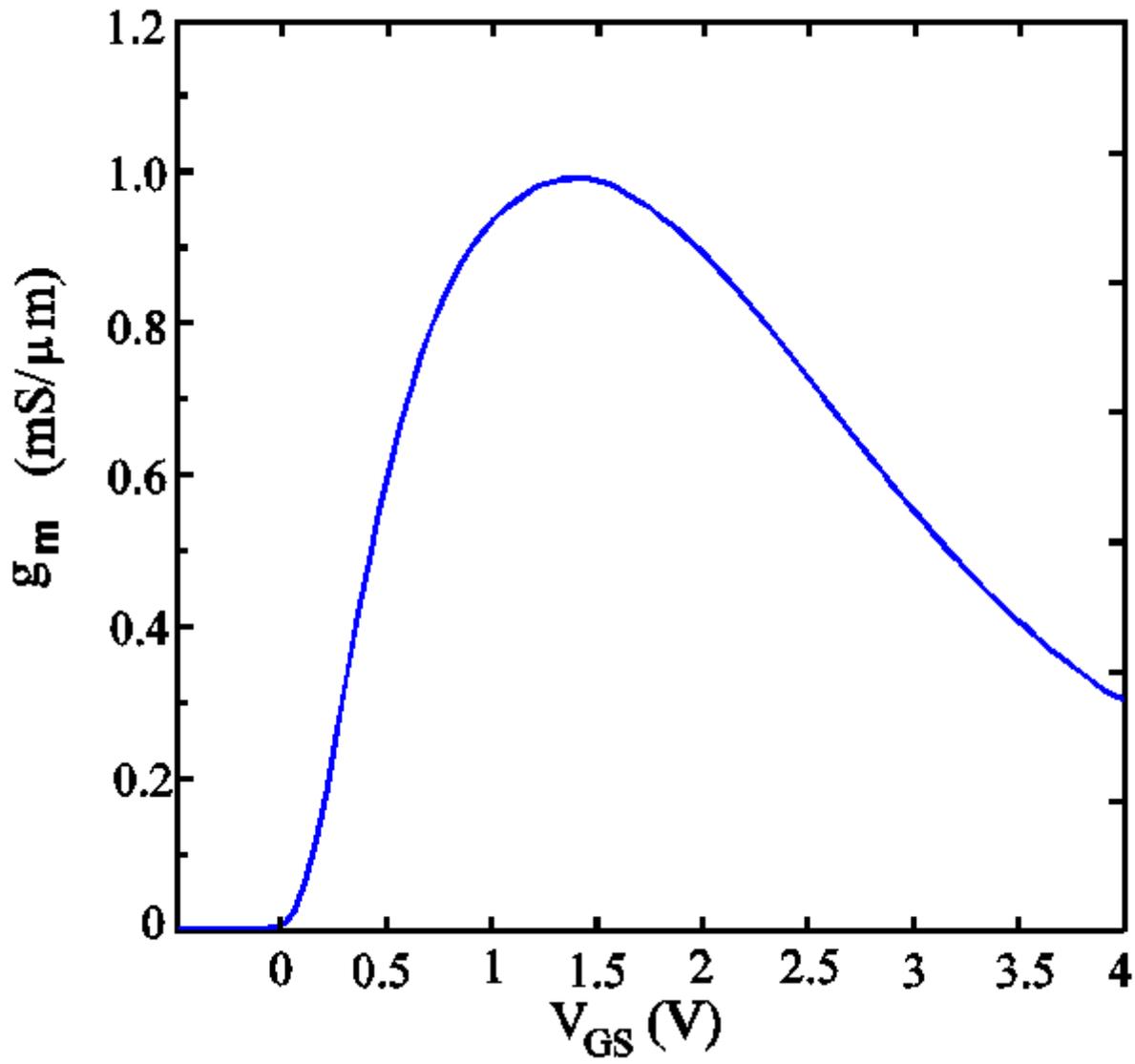Transconductance characteristics of the HV DG MOSFET.

Figure 6
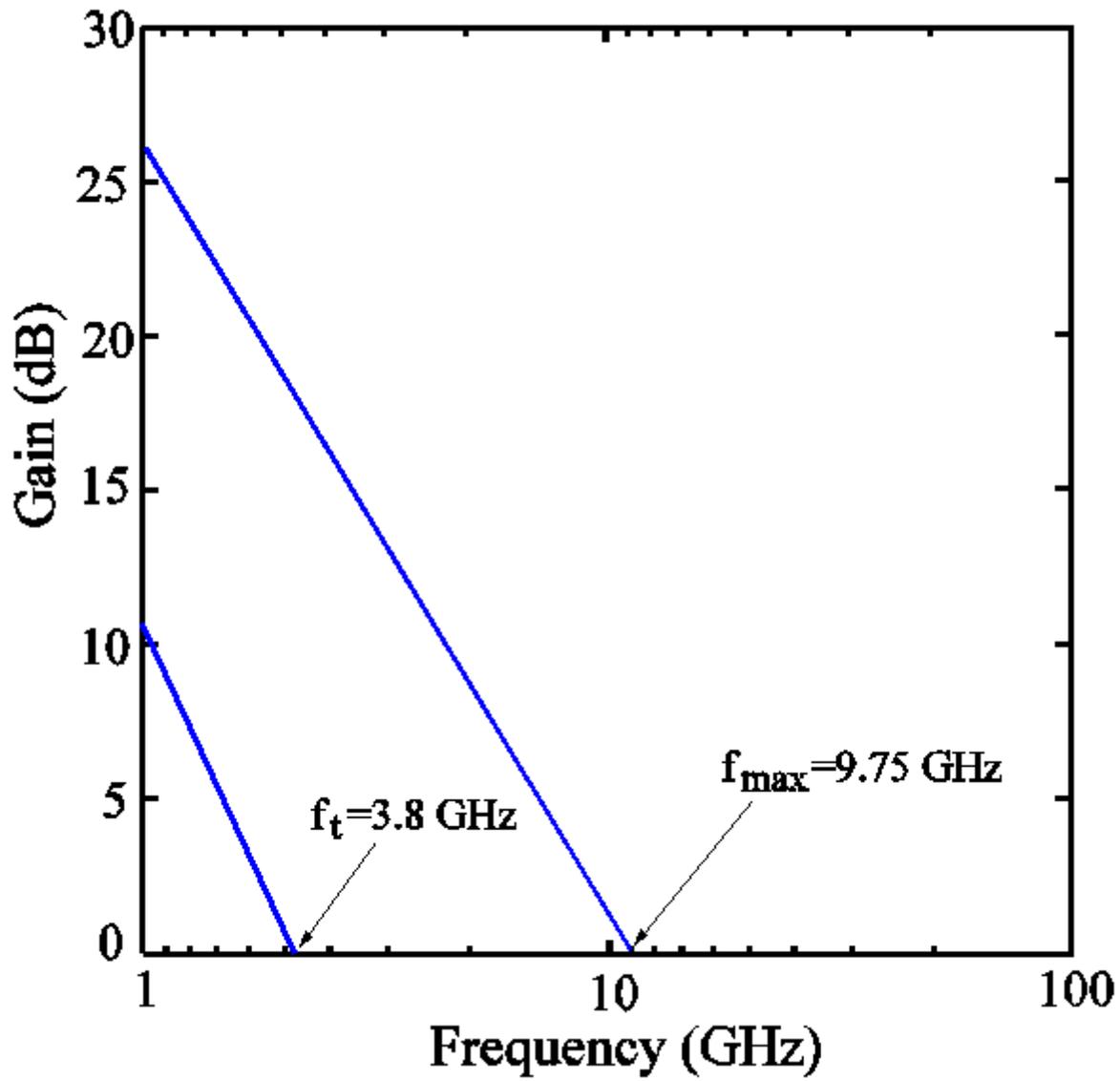
Transconductance characteristics of the LV MOSFET.
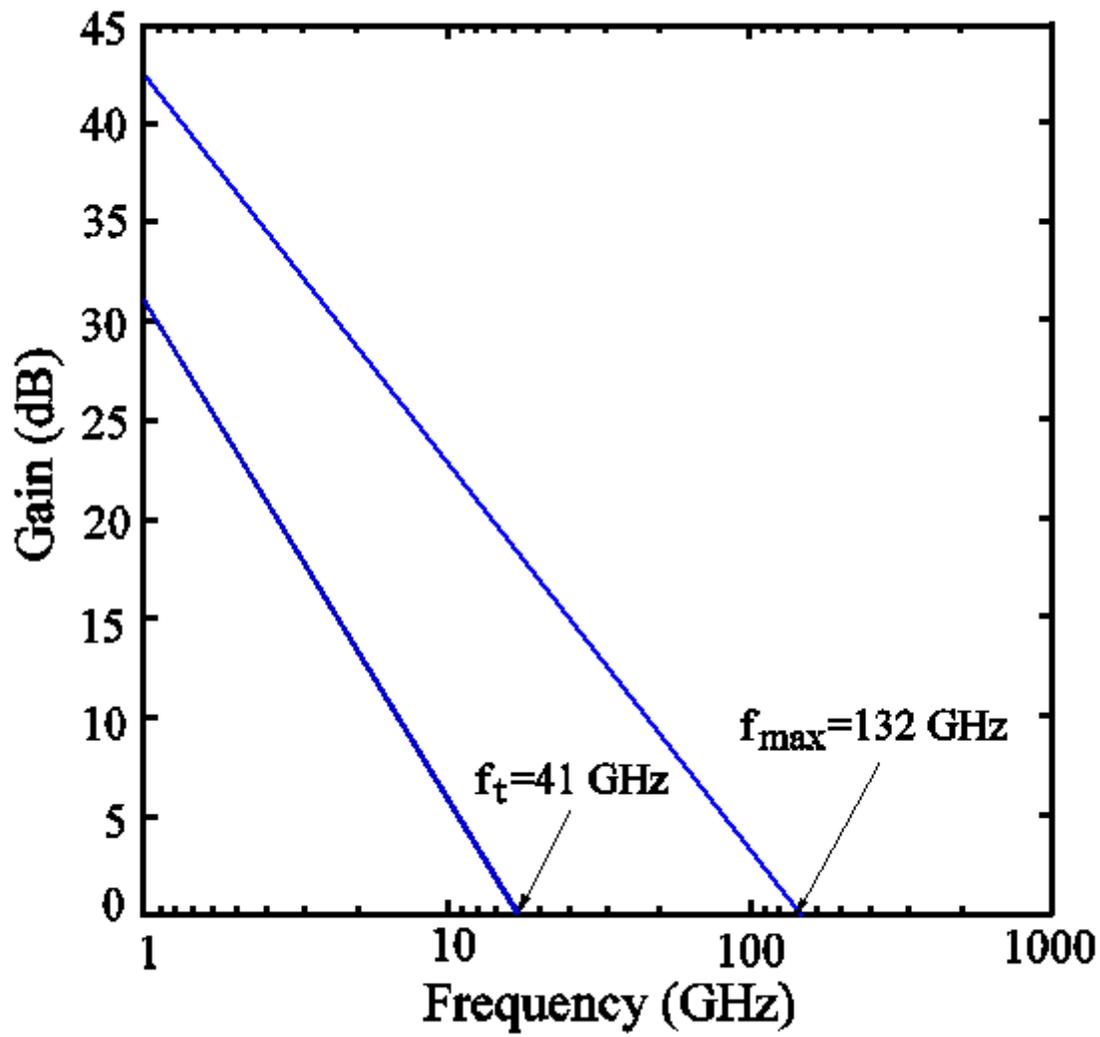
Figure 7

Frequency response of the HV DG MOSFET.

Figure 8
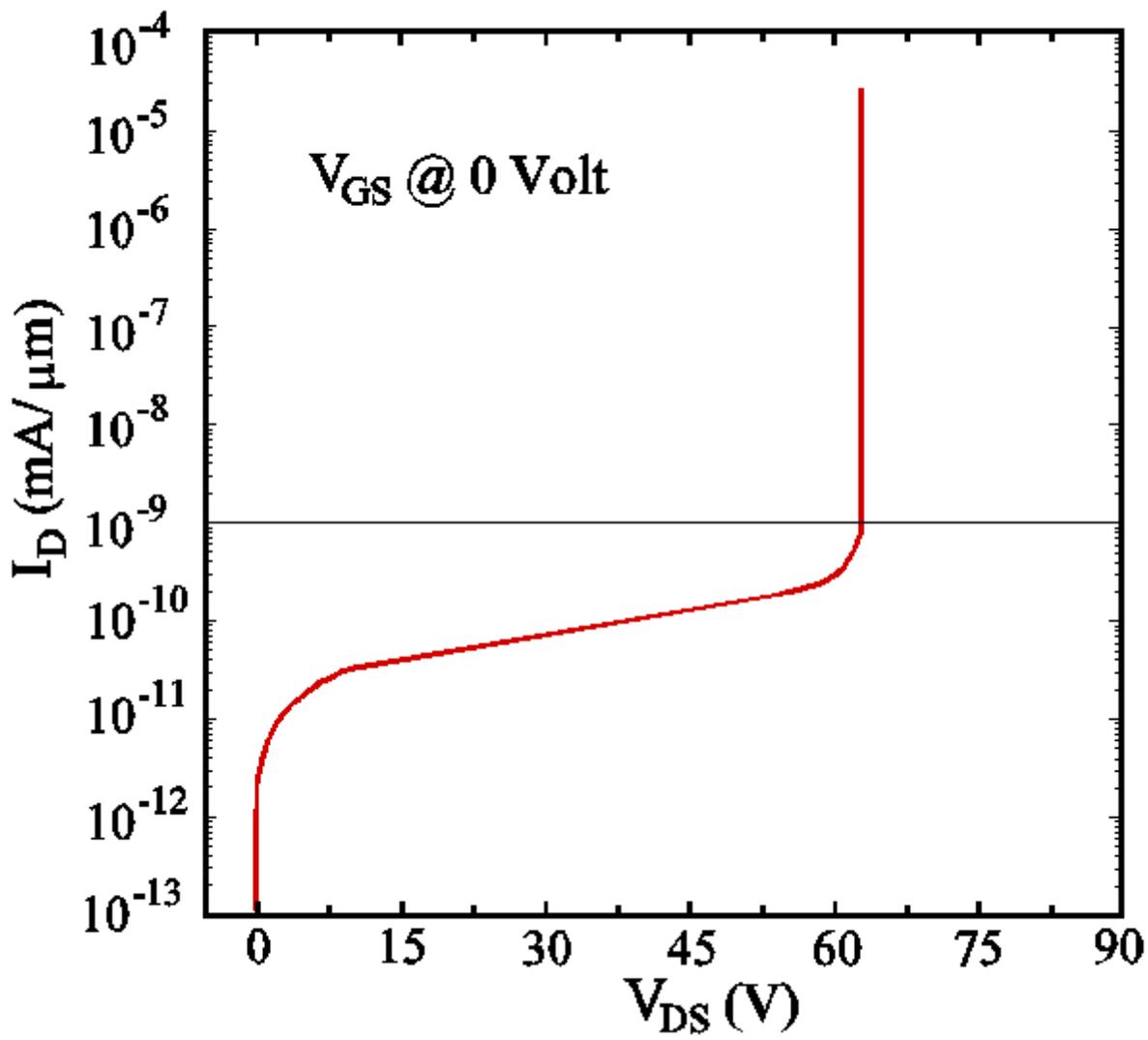
Frequency response of the LV MOSFET

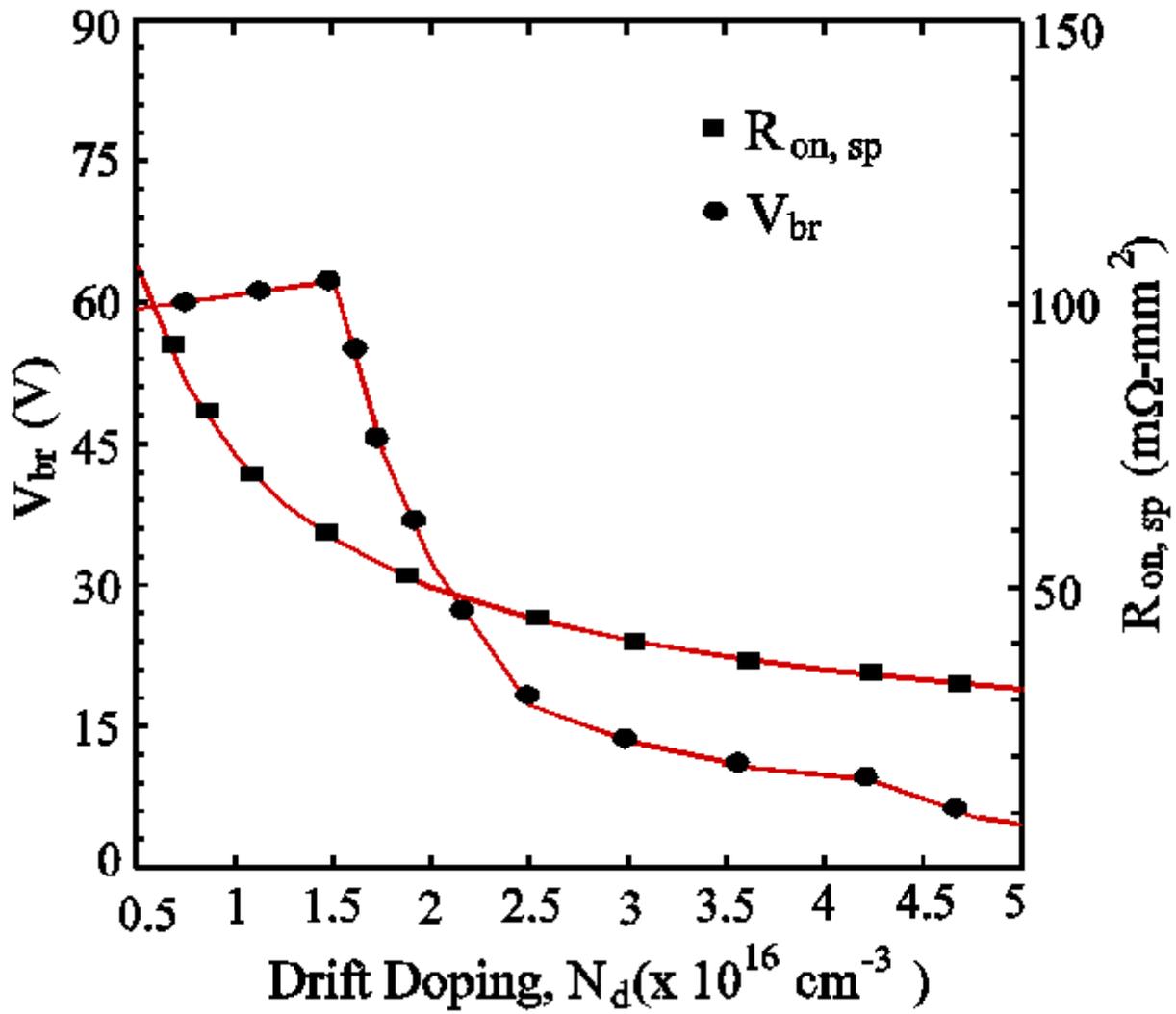**Figure 9**

Breakdown characteristics of the HV DG MOSFET
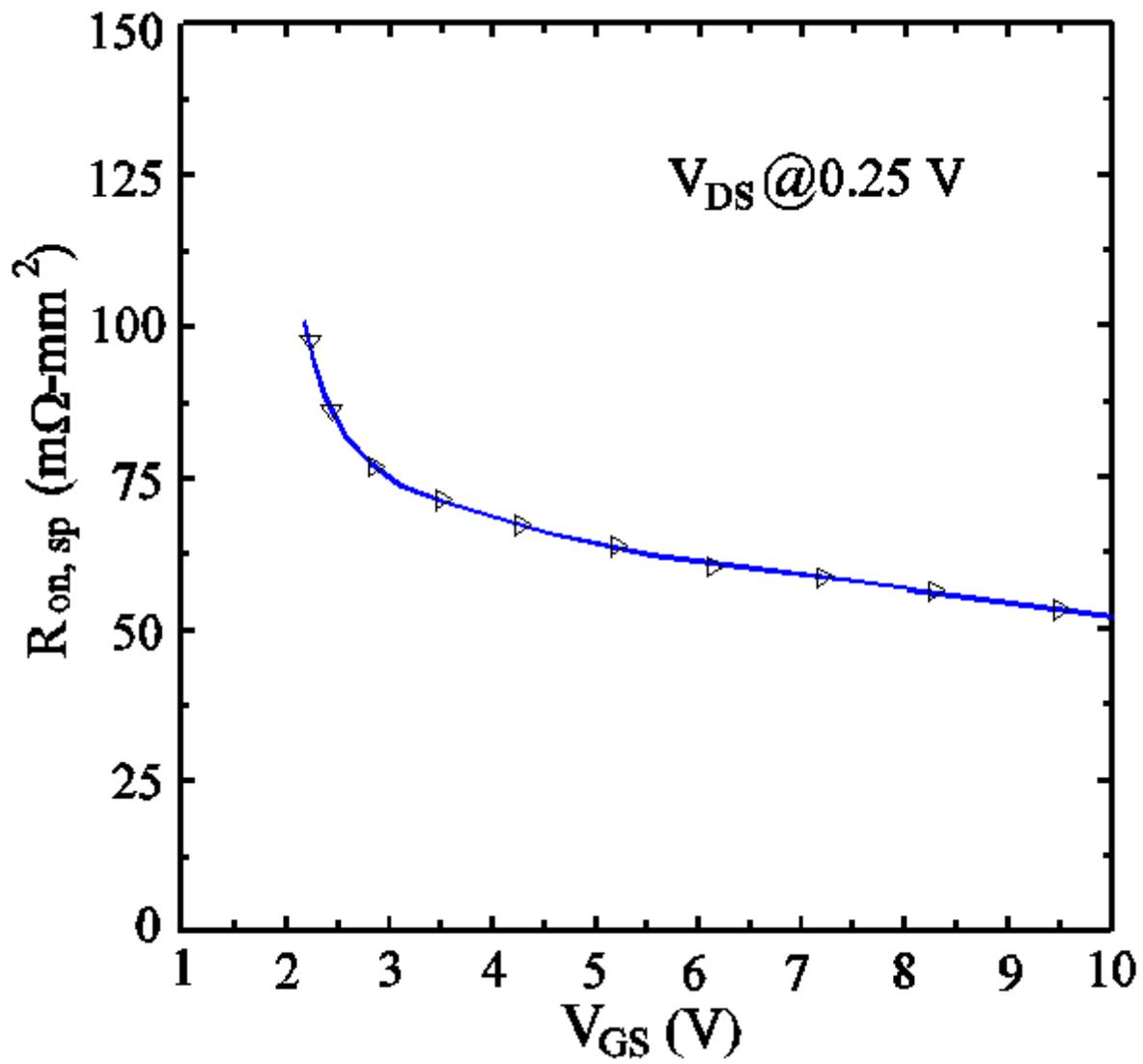
Figure 10

Vbr and Ron,sp as a function of Nd of the HV DG MOSFET

Figure 11

Specific on-resistance @ VGS of the HV DG MOSFET