

# Design and Investigation of Gate Stacked Vertical TFET with N<sup>+</sup> SiGe pocket doped heterojunction for performance enhancement

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**Abstract**—In this paper, a novel delta-doped N<sup>+</sup> Silicon-Germanium Gate Stacked Triple Metal Gate Vertical TFET (Delta doped N<sup>+</sup> GS TMG VTFET) is proposed and investigated using the Silvaco TCAD simulation tool. Four different combinations were presented and compared with and without the gate stacking method and Si<sub>0.2</sub>Ge<sub>0.8</sub> N<sup>+</sup> pocket delta-doped layer to render the optimized results. Among all, Delta doped N<sup>+</sup> GS TMG VTFET structure comes out with a very steep sub-threshold slope (9.75 mV/dec), 40 % lower than the first configuration of TMG VTFET. The inclusion of the N<sup>+</sup> delta-doped layer between the source and channel and gate will enhance the ON-state drive current performance by reducing the OFF-state leakage current. This happens due to the lower bandgap of the N<sup>+</sup> delta-doped layer cause narrow BTBT, which results in a high drive current. The Triple metal gate is designed to mitigate the ambipolar conduction by modulating the optimized work function at 4.15, 4.3, and 4.15 eV. The distribution of the source channel in the vertical structure will enhance the device's scalability due to the electron tunneling moves in the vertical electric field direction. The optimally constructed structure demonstrates improved performance, such as a high I<sub>ON</sub>/I<sub>OFF</sub> current ratio (~10<sup>13</sup>) and sub-threshold voltage (0.33 V). The results obtained from the proposed device make it suitable for the ultra-low-power device application.

**Keywords**— Triple Metal Gate (TMG), Gate stack (GS), Band to band Tunneling (BTBT), Subthreshold slope (SS), Vertical Tunnel Field Effect (VTFET).

## I. INTRODUCTION

Over the past decade, CMOS has been found as a continuous scaled device in nanometer regimes to improve the integrated density, speed, and efficiency [1]. However, in the era of miniaturization, CMOS devices were continuously facing the problem of fundamental limits due to various short channel effects (SCE) such as hot-electron carrier, high subthreshold slope (SS) with the Boltzmann limit of 60 mV/decade [2,3]. To overcome all these technical issues, tunnel field effect transistors (TFET) are found to promise the candidate for the next-generation low power devices. TFET uses a band-to-band tunneling mechanism instead of thermionic emission [4,5]. This device can easily overcome the SS fundamental limit of 60 mV/decade with a low OFF state current [6]. In the TFET device, the tunneling probability T(E) is directly proportional to the ON-state current via quantum band to band tunneling mechanism using equation (1), given as:

$$T(E) \approx \exp\left(-\frac{4\sqrt{2m^*} E_g^{\frac{3}{2}}}{3|e|h(\Delta\Phi + E_g)}\right) \quad (1)$$

$$\approx \exp\left(-\frac{4\sqrt{2m^*} E_g^{\frac{3}{2}}}{3|e|h(\Delta\Phi + E_g)} \sqrt{\frac{\epsilon_{Si}}{\epsilon_{ox}}} t_{ox} t_{Si}\right) \quad (2)$$

Where m<sup>\*</sup>, Δφ, E<sub>g</sub>, t<sub>ox</sub>, t<sub>si</sub>, and ε<sub>ox</sub> are the effective mass of the charge carrier, energy range, energy bandgap, gate oxide, silicon film thickness, and dielectric constant [6,7]. From the above equation (1) & (2), it can be concluded that the high dielectric constant and reducing bandgap optimize the implementation of TFET drive current.

However, conventional silicon-based TFET has various drawbacks, which include low ON state drive current (I<sub>ON</sub>), a high threshold voltage (V<sub>th</sub>), and ambipolar conduction with drain, induced current due to large silicon bandgap material [8-10]. Therefore, it is necessary to remove these constraints and further enhance the current of the ON-state as well as suppress the ambipolar behavior to allow it for different applications.

Multiple methods and devices to solve these problems structures to enhance the unit's efficiency have been suggested [10-12]. Since these techniques mitigate the ambipolar currents, they are known only at the cost of complexity in the fabrication method [13,14]. However, in the proposed device, we can overcome ambipolar by introducing the triple metal gate with optimized work functions.

To conquer these technological obstacles, the implementation of heterojunction TFET structures and source areas consist of new materials, such as germanium, silicon Germanium, or low bandgap Group III-V [15-18]. This will achieve a higher I<sub>ON</sub> current and steeper subthreshold slope (SS). The use of high-k gate oxide in the stack with SiO<sub>2</sub> is a significant way to improve further the SS of the short-channel TFETs [19-20]. The gate stacking process can be observed using high-k gate oxide like HfO<sub>2</sub> in the stack with SiO<sub>2</sub> is a significant way to improve further the SS of the short-channel TFETs [21-22]. The ratio of the width used of SiO<sub>2</sub> with high-k gate oxide can be calculated using the Equivalent Oxide Thickness (EOT) equation (3).

$$t_{EOT} = \frac{\epsilon_{high-k}}{\epsilon_{SiO_2}} t_{ox} \quad (3)$$

It has also been experimentally demonstrated the utilization of vertical TFET (V-TFET) will remove the scaling constraints of the TFETs. This happens due to the mechanism under which the BTBT takes place parallel with the gate electric field that

will significantly boost the tunneling current density as it is not directly dependent on the device's channel thickness [23-25]. To improve the current ratio, it has also been reported that by introducing the delta-doped or pocket layer in the middle of the source channel area of the low bandgap of  $\text{Si}_{0.2}\text{Ge}_{0.8}$  material will improve the current ratio and the subthreshold slope, which was earlier restricted to the range of 30-50 mV/dec [26,27]. However, individually, these methods effectively work to the system but not efficient when it comes to the high-performance requirement of densely packed circuits.

In this paper, a combined effect of gate stacking and delta-doped SiGe heterojunction layer between the source-channel interface in the triple metal gate vertical Tunnel FET has been implemented for the first time to TFET structures. Also, to suppress the ambipolar current with ON-state current's unintended performance, a vertical TFET with the triple metal gate is introduced and optimized by the work function engineering method through the TCAD simulation tool [28]. Finally, the proposed device, Delta doped N+ GS-TMG-VTFET (Gate stacked triple metal gate Vertical TFET) with N+ delta-doped structure, gives a detailed analysis of how the device design varies with the different parameter to optimize the performance and the characteristics of the device. This paper has been divided into three sections. The first part of the article contains the system's parameters, and in the second segment, simulation effects are discussed, while in the last segment, findings are concluded.

## II. DEVICE STRUCTURE AND SIMULATION FRAMEWORK

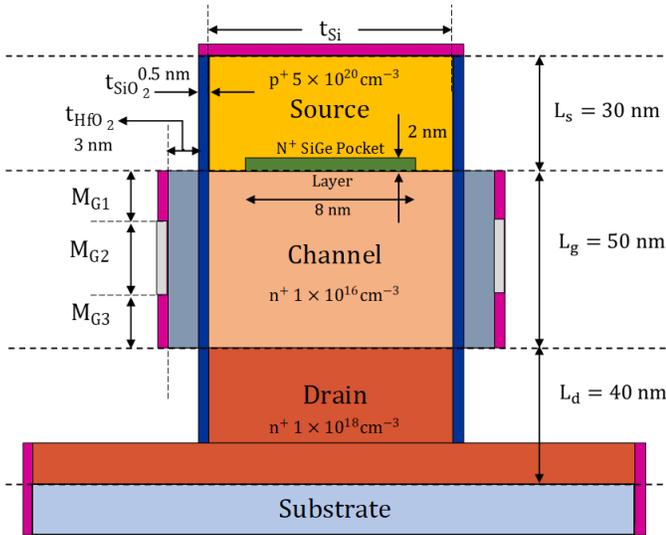


Fig. 1. Schematic diagram of an n-channel Delta doped N+ Gate stacked Triple Metal Gate Vertical Tunnel Field Effect Transistor (Delta doped N+ GS TMG VTFET).

Fig. 1 shows the schematic diagram of the Delta doped N+ Gate stacked Triple Metal Gate Vertical Tunnel Field Effect Transistor (Delta doped N+ GS TMG VTFET). The Gate electrode has been divided into three sections with optimized work function  $M_{G1}$ ,  $M_{G2}$ ,  $M_{G3}$  at 4.15, 4.30, and 4.15 eV for auxiliary, control, and tunneling gate mitigate the ambipolar characteristics. An N+ delta-doped layer is introduced to minimize the tunneling path with a low bandgap. The ON-state

current is highest with  $I_{ON}/I_{OFF}$   $10^{-4}/10^{-17}$  among the four-combination discussed in the next Figure. The design parameter used for simulation of the Delta doped N+ GS TMG VTFET is given in table I.

TABLE I: SELECTED DEVICE DESIGN SPECIFICATION USED FOR SIMULATION WORK

Parameter Used	Specification (Delta doped N+ GS TMG VTFET)
Channel Length ( $L_g$ )/doping concentration	50 nm/ $1 \times 10^{16} \text{ cm}^{-3}$ (n-type)
Source Length ( $L_s$ )/doping concentration	30 nm/ $5 \times 10^{20} \text{ cm}^{-3}$ (p-type)
Drain Length ( $L_d$ )/doping concentration	40 nm/ $1 \times 10^{18} \text{ cm}^{-3}$ (n-type)
Work function-Tunneling Gate ( $M_{G1}$ )	4.15 eV
Work function-Control Gate ( $M_{G2}$ )	4.30 eV
Work function-Auxiliary Gate ( $M_{G3}$ )	4.15 eV
Gate Oxide thickness- $\text{SiO}_2$ / $\text{HfO}_2$	0.5 nm/ 3 nm
N+ SiGe Delta doped Layer	2 nm / 8nm

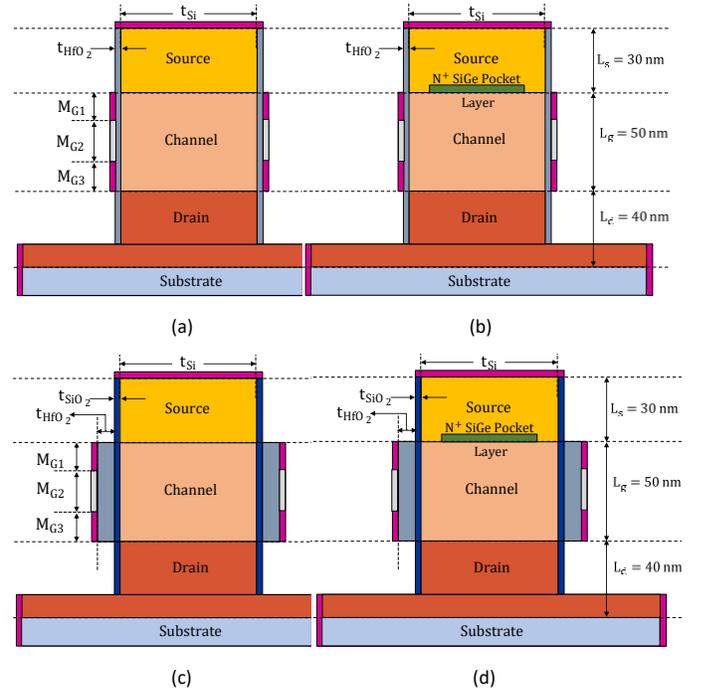


Fig. 2. Four different Schematic diagram combination with similar doping concentration and optimized triple metal work function (a) TMG VTFET (b) GS TMG VTFET (c) Delta doped N+ TMG VTFET (d) Delta doped N+ GS TMG VTFET

Initially, we compare and simulate four types of a different Vertical TFET structure configuration to achieve the device's optimized result, as shown in Fig.2. The first Triple metal Gate Vertical TFET device comprises silicon material using  $\text{HfO}_2$  as high dielectric material of gate oxide. A permittivity of 22 is shown in Fig.2(a). Here the electrode material is divided into three metal gates, namely  $M_{G1}$ ,  $M_{G2}$ , and  $M_{G3}$ , where  $M_{G1}$  is near the source side,  $M_{G3}$  near the drain side, and  $M_{G2}$  between the source and drain, respectively. A metal gate work function  $M_{G2}$  was used with the value of 4.30 eV, while the other two optimized with the value 4.15 eV. The device channel length, source, and drain length are 50, 30, and 40 nm. The n channel

region is lightly doped ( $1 \times 10^{16} \text{ cm}^{-3}$ ), the p+ drain region is heavily doped ( $5 \times 10^{20} \text{ cm}^{-3}$ ), while the n+ drain region is moderately doped ( $1 \times 10^{18} \text{ cm}^{-3}$ ) to mitigate the ambipolarity.

In Fig. 2(b), the second configuration, a delta-doped n+ pocked with  $\text{Si}_{0.2}\text{Ge}_{0.8}$ , has been introduced to the first structure of TMG Vertical TFET with the dimension of 8 nm to 2 nm as length vs. height. This is done due to the lower bandgap range of the germanium material, which will boost the ON-state current by varying the mole fraction  $x$ . As the source of p+, Ge material consisting of a lower bandgap of 0.66 eV than that of Si (1.1 eV) is used. In contrast, the channel and drain regions use more extensive silicon bandgap material to maintain a low leakage current. A higher electron BTBT (e-BTBT) efficiency is achieved in this way, which significantly improves the ON-state current. In the third case, a layer of a 0.5 nm  $\text{SiO}_2$  layer is stacked with a 3 nm  $\text{HfO}_2$  layer, as shown in Fig. 2(c). Rest all the configuration will remain the same as that we have considered in the first one.

Finally, all the configurations jointly collaborated to form the fourth vertical structure for optimized results, as shown in Fig. 2(d). The value chosen for the device design parameter is summarized in given table I. To estimate the device performance, a TCAD 2D-ATLAS Silvaco device simulator has been used [28]. However, the simulated device is first calibrated with the reported work of Vertical TFET with the help of plot digitizer software.

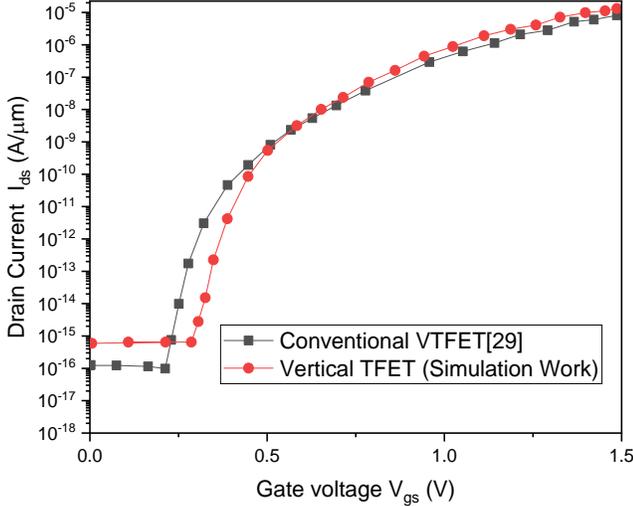


Fig. 3. Calibrated drain device ( $I_{ds}$ - $V_{gs}$ ) characteristics of the implemented Vertical TFET simulation work with conventional TFET.

Figure 3 represents the conventional calibrated Vertical TFET structure compared to the simulated device's drain characteristics curve [29]. The charge carriers' generations and their recombination at the Semiconductor-semiconductor and insulator-semiconductor interface are modeled on SRH (Shockley-Read-Hall) Model. For better carrier transport simulation, we used the recombination model with doping-dependent mobility. However, the electrons' tunneling is estimated via the non-local band model to band tunneling [30,31]. This model will consider the point-to-point tunneling at the energy band gradient.

Additionally, this model also supports the abrupt heterojunction with any arbitrary tunneling barriers, a non-

uniform electric field. It calls the results of direct tunneling and phono-assisted tunneling, so that accurate simulation results based on the models of both Kane and Keldysh [32,33] retrieved. The newton trap method is eventually invoked as a solution method. For the nonlocal path BTBT model, table 2 gives the comprehensive A and B parameters of both silicon and germanium.

TABLE II: PARAMETERS A AND B USED FOR NON-LOCAL BTBT MODEL

Material Used	Parameters	
	A	B
Silicon	$3.29 \times 10^{15} \text{ cm}^{-3}\text{s}^{-1}$	$23.8 \times 10^6 \text{ Vcm}^{-1}$
Germanium	$1.67 \times 10^{15} \text{ cm}^{-3}\text{s}^{-1}$	$6.55 \times 10^6 \text{ Vcm}^{-1}$

### III. RESULTS AND DISCUSSION

This section deals with the result and its descriptive analysis. To optimize the device design parameters, a detailed investigation and discussion of the variation in the drain current characteristics, energy band diagram, metal gate work function, drain doping concentration, electric field, and surface potential are included in this section. The delta-doped layer bandgap  $\text{Si}_{0.2}\text{Ge}_{0.8}$  heterojunction with gate stacking method has compared drain current characteristics with the silicon-based Vertical structure without delta doping layer gate stacking. This has been done to justify the various parameters individually. In addition to this, many of the different constraints like recombination rate, electron and hole concentrations, and band to band tunneling rate, transconductance, gate capacitance with its electric field and surface potential are graphed and compared for all four kind of configuration. The name of four types of different structure are:

- 1: TMG VTFET
2. Delta doped N+ TMG VTFET
3. GS TMG VTFET
4. Delta doped N+ GS TMG VTFET

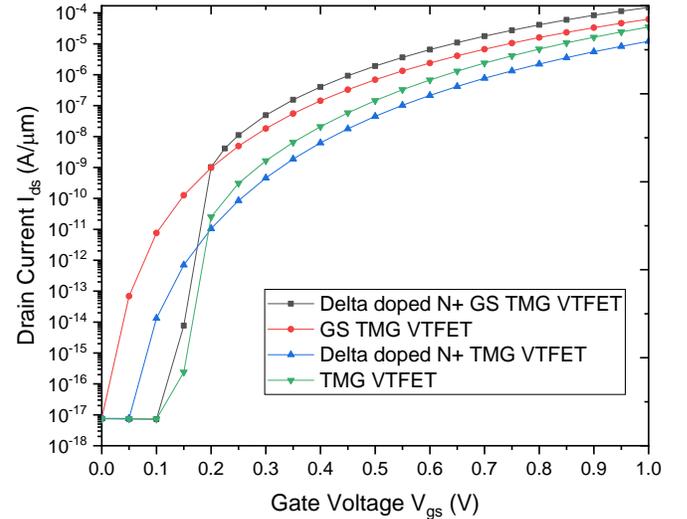


Fig. 4. Comparison of drain current ( $I_{ds}$ - $V_{gs}$ ) characteristics for all the proposed structures TMG VTFET, GS TMG VTFET, Delta doped N+ TMG VTFET, and Delta doped N+ GS TMG VTFET.

Initially, the  $I_d$ - $V_{gs}$  characteristics will be compared for all the different device structures TMG VTFET, GS TMS VTFET,

Delta doped N+ TMG VTFET, and Delta doped N+ GS TMG VTFET. Fig. 4 shows that the drain drive current is continuously improved by one order when introducing gate stacking and n+ delta-doped layer at the source-channel interface. In addition to the SS, 40-45 % of the improvement shown that to the TMG VFET. The mole-fraction value  $x$  of delta doping layer N+  $\text{Si}_{(1-x)}\text{Ge}_x$  layer will decide the germanium percentage added to the device. For the proposed device, we have taken the value of mole fraction  $x$  as 0.8. As a result, the continuous lowering in the band gap between source to channel region, which boots the tunneling current, will increase the device drain current. The impact of Gate stacking improves the SS by 20-25 % because the work function increases the band's slope bends along with the bands' narrowing. Molecular beam epitaxy (epitaxial growth technique) and chemical vapor deposition will allow the growth of these kinds of heterojunctions. The overall performance of the Delta doped N+ GS TMG VTFET design was found to be the best without affecting the OFF-state current. A comparison chart of threshold voltage ( $V_{th}$ ) and SS for different configurations is shown in table 3.

TABLE III: COMPARISON TABLE OF SS AND  $V_{th}$  FOR ALL THE FOUR CONFIGURATIONS

Configuration	Parameters	
	Threshold Voltage (V)	Subthreshold slope (SS)
TMG VTFET	0.54 V	37.69 mV/dec
Delta doped N+ TMG VTFET	0.47 V	32.68 mV/dec
GS TMG VTFET	0.38 V	12.67 mV/dec
Delta doped N+ GS TMG VTFET	0.33 V	9.75 mV/dec

The subthreshold slope is defined as the change in drain current per decade with respect to the change in gate-source  $V_{gs}$  voltage. However, the threshold voltage of the TFET is derived from the constant current method at the value of  $V_{gs}$ , for which the drain current cut the line at  $10^{-7}$  A/ $\mu\text{m}$ . It can also be defined as the minimum energy barrier for which the charge carriers start tunneling from the source valance band to the channel conduction band. In simple words, “the applied gate voltage for which the energy barriers narrowing start to saturate”[34].

Figure 5 shows the variation of energy band diagram for all the different device structures TMG VTFET, GS TMS VTFET, Delta doped N+ TMG VTFET, and Delta doped N+ GS TMG VTFET, respectively. It is noted from the figure that tunneling is maximum narrower for the Delta doped N+ GS TMG VTFET concerning other device designs. This happens because of the lower bandgap material introduced between the tunneling barrier to reduce the overall path and resulting in high electron tunneling.

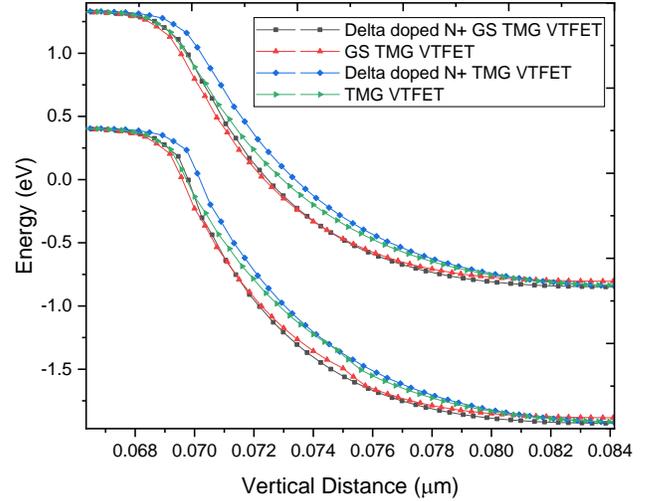


Fig. 5. Simulation analysis of Energy band diagram for all the proposed structure TMG VTFET, GS TMG VTFET, Delta doped N+ TMG VTFET, and Delta doped N+ GS TMG VTFET for ON-state mode at  $V_{gs}$  and  $V_{ds} = 1$  V.

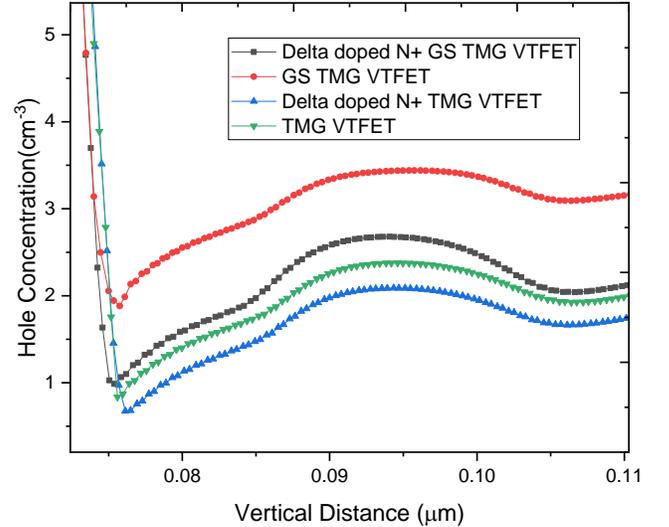


Fig. 6 (a). Distribution of hole charge carrier concentration for all the proposed structure TMG VTFET, GS TMG VTFET, Delta doped N+ TMG VTFET, and Delta doped N+ GS TMG VTFET.

Fig. 6 shows the distribution of the charge carriers' concentration of (a) hole and (b) electrons, respectively. Both the carrier concentration distributed in a vertical direction from source to drain. Figure 6(a) observed that the concentration of the holes will start decreasing suddenly at the initial level of the channel length (i.e 50 nm). Moreover, the holes concentration will more deteriorate for the configuration of N+ TMG VTFET and N+ GS TMG VTFET. This happens due to the addition of N+ delta doped layer at the source-channel interface will increase the electron concentration.

In the next Fig. 6(b) distribution of the electron charge carrier concentration with respect to the vertical position of the device and case is the vice-versa condition of the holes charge carrier concentration.

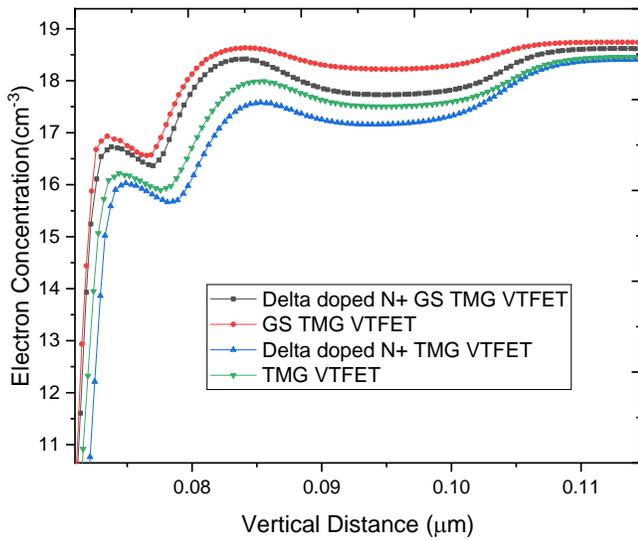


Fig. 6(b). Distribution of electrons charges carrier concentration for all the proposed structure TMG VTFET, GS TMG VTFET, Delta doped N+ TMG VTFET, and Delta doped N+ GS TMG VTFET.

It will compare the Delta doped N+ GS TMG VTFET configuration having the highest graph variation compared to the TMG VTFET, GS TMS VTFET, Delta doped N+ TMG VTFET structures, respectively. This happens due to the increase in the number of electrons that will proportionality increase in the tunneling current and also improve the drain drive current.

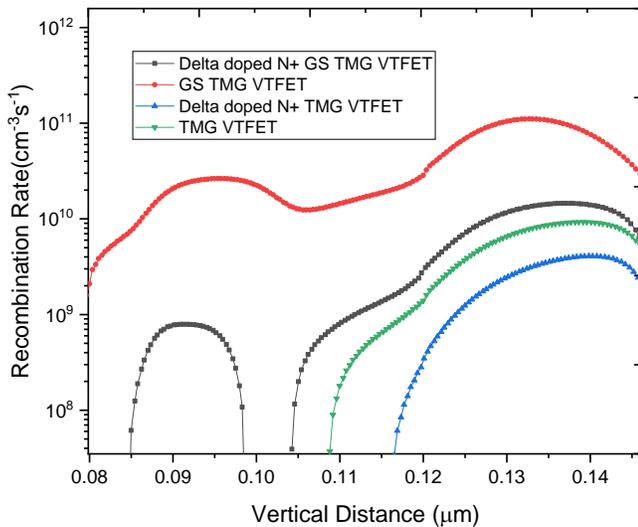


Fig. 7. Recombination rate analysis of the charge carriers for all the proposed structure TMG VTFET, GS TMG VTFET, Delta doped N+ TMG VTFET, and Delta doped N+ GS TMG VTFET.

Recombination rate and band to band tunneling rate for the electron and the holes are plotted and validated for all four structures. From Fig. 7, it is depicted that the structure which consists of the N+ delta doping layer will have a negligible recombination rate with respect to the vertical dimension of the device design. It happens due to the lower bandgap material (N+ delta doping) introduce in between the tunneling path will

mitigate the minority charge carriers to accelerate the overall process.

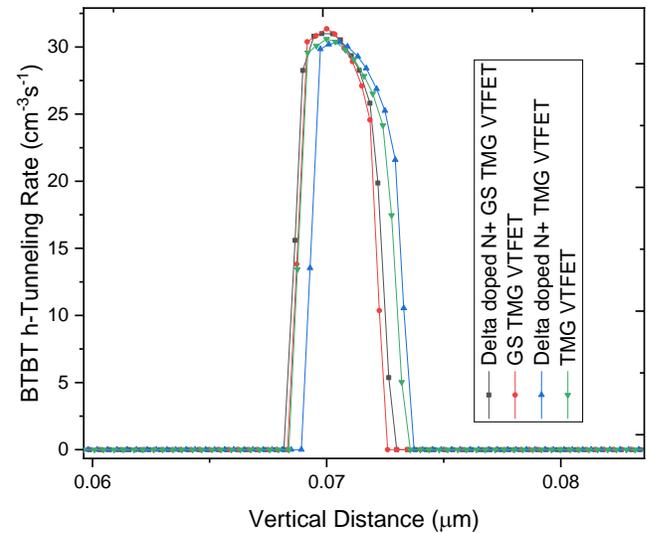
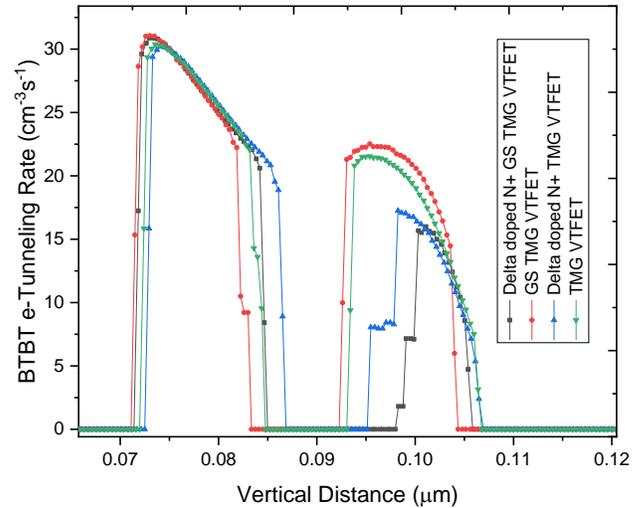


Fig.8 Analysis of BTBT rate (a) e-electron (b) h-holes for all the proposed structure TMG VTFET, GS TMG VTFET, Delta doped N+ TMG VTFET and Delta doped N+ GS TMG VTFET.

Figure 8 (a) show the e-band to band tunneling rate with respect to the vertical distance of the device design. The maximum electron tunneling rate can be differentiate from the non-delta doped structure. Due to N+ delta doping the band gap between valance to the conduction band will become narrower at source-channel inter junctions that will allow to flow high tunneling rate. Now in Figure 8(b) holes band to band tunneling rate for all the four configurations into order to find the determine the holes impact on the tunneling rate. However, the it is observed form the figure that the hole tuning is almost same for all the four different structures i.e. very smaller variation in graph analyzed.

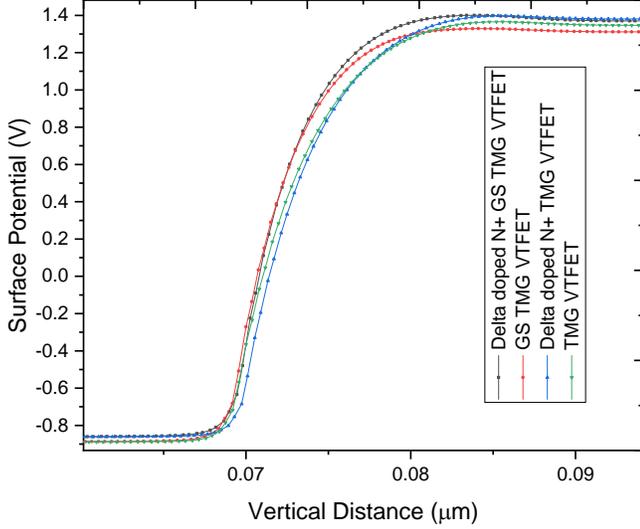


Fig. 9. Surface Potential profile variation for all the proposed structure TMG VTFET, GS TMG VTFET, Delta doped N+ TMG VTFET and Delta doped N+ GS TMG VTFET at  $V_{ds}= 1V$ .

Fig. 9 demonstrates the surface potential characteristics for all four different structures. It can be observed from the figure that with the rise in the percentage of germanium in SiGe composition, they will reduce the energy bandgap [35]. As a result, the Delta doped N+ TMG VTFET structures have the highest rise in the surface potential than other configurations.

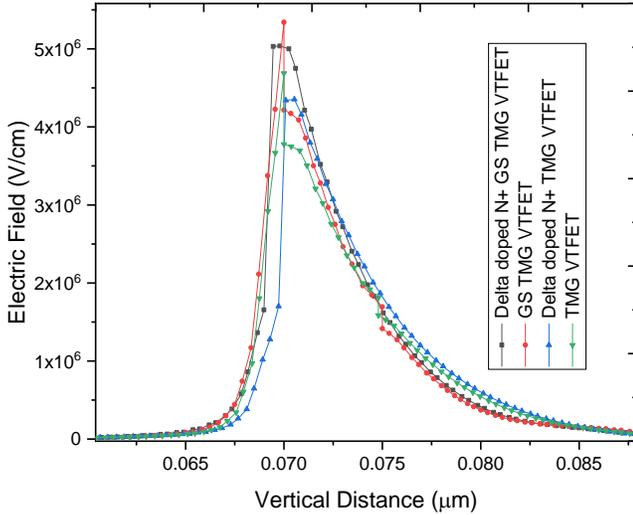


Fig. 10. Electric field variation for all the proposed structure TMG VTFET, GS TMG VTFET, Delta doped N+ TMG VTFET and Delta doped N+ GS TMG VTFET at  $V_{ds}= 1V$ .

In Figure 10, we will discuss the electric field validation for all four structures. It can be analyzed from the figure that the electric field is high for the configure of Delta doped N+ TMG VTFET and Delta doped N+ GS TMG VTFET rather than TMG VTFET and GS TMS VTFET. This is because of the linear relation between the surface potential and the electric field. As a result, the electric field also high before the source-channel interface, which causes more tunneling phenomenon when the barrier will suppress.

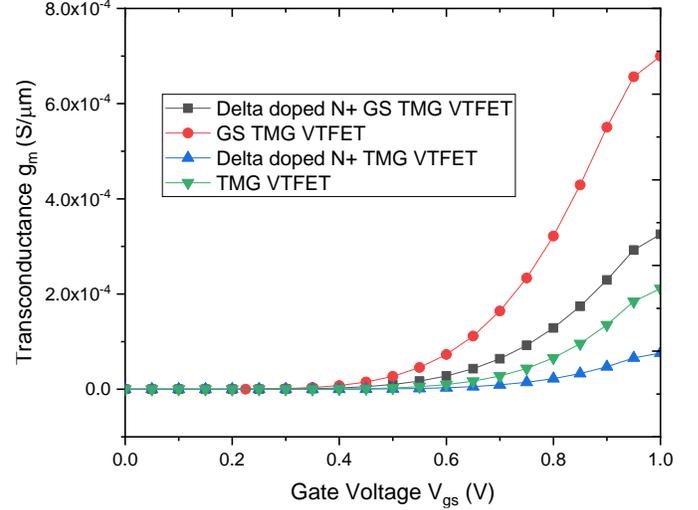


Fig. 11. Transconductance ( $g_m$ ) parameter variation for all the proposed structure TMG VTFET, GS TMG VTFET, Delta doped N+ TMG VTFET and Delta doped N+ GS TMG VTFET at  $V_{ds}= 1V$ .

Fig. 11 demonstrates the variation in the transconductance with respect to the gate voltage. The analysis of the transconductance characteristics is the key to determining the device analog performance. Additionally, it also measures the capability of the transistor in transforming the voltage into the current. It can observe from Fig. 11 that Delta doped N+ GS TMG VTFET is found to be maximum (1 order higher) trans conducting for the ON state condition at  $V_{gs} = 1V$  and  $V_{ds} = 1V$ .

$$\frac{1}{SS} = \frac{\Delta \log_{10} I_{ds}}{\Delta V_{gs}} \quad (4)$$

$$\frac{1}{\log_{10}} \frac{\partial \log_{10}(I_{ds})}{\partial V_{gs}} = \frac{1}{\log_{10}} \frac{1}{I_{ds}} \frac{\partial I_{ds}}{\partial V_{gs}} \quad (5)$$

$$\frac{1}{SS} = \frac{1}{\log_{10}} \frac{1}{\partial I_{ds}} g_m \quad (6)$$

$$\frac{g_m}{I_{ds}} = \frac{\log_{10}}{SS} \quad (7)$$

Using equation (4) to (7), we can find out the relation between transconductance and Subthreshold Slope [26]. Form equation (7), the transconductance value inversely dependent upon the SS value. Since Delta doped N+ GS TMG VTFET holds the lowest SS value, it comes with the highest transconductance value, as can be justified from Fig. 11.

#### IV. CONCLUSION

An N+ delta-doped SiGe layer Gate Stacked Triple Metal Gate Vertical TFET (Delta doped N+ GS TMG VTFET) is employed in this paper. Four of the different configurations: 1. TMG VTFET 2. Delta doped N+ TMG VTFET 3. GS TMG VTFET 4. Delta doped N+ GS TMG VTFET has been analyzed and compared with different electrical parameters using the 2D Silvaco TCAD simulation tool. The proposed structure takes advantage of a triple metal gate to mitigate the ambipolarity, and gate staking with the high k dielectric constant will improve

the On-state current. The gate stacking combination of SiO<sub>2</sub> and HfO<sub>2</sub> will improve the controllability of the device tunneling current. The N<sup>+</sup> SiGe delta-doped layer will narrow the tunneling path due to the lower bandgap of germanium and enhance the band to band tunneling drive current. The vertical structure shows the advantage of having the source-channel distribution in the vertical direction, directly proportional to the vertical electrical field. The optimized structure simulation result will show a very high I<sub>ON</sub>/I<sub>OFF</sub> ratio (~10<sup>13</sup>). The ON-state and OFF-state current reported to be 1.4 × 10<sup>-4</sup> A/μm and 7.45 × 10<sup>-18</sup> A/μm with 0.33 V as sub-threshold voltage. In the case of short channel Effect, the sub-threshold slope is rendered as (9.75 mV). These results show the superiority of the proposed device in terms of SS and drive current. Therefore, with these results, it can be concluded that the proposed device (Delta doped N<sup>+</sup> GS TMG VTFET) is a promising candidate for power device technology application.

**Data Availability:** Not applicable.

#### Author contributions:

**Shilpi Gupta:** Conceptualization, TCAD Software, Writing-Original draft preparation, Investigation, Software, Validation, Writing and Editing.

**Subodh Wairya:** Supervision and Reviewing.

**Shailendra Singh:** Methodology, Data curation, Visualization.

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**Consent to participate:** Not applicable

**Consent for Publication:** The Author transfers his copyrights to the publisher.

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