

Investigation of the impact of mole-fraction on the digital benchmarking parameters as well as sensitivity in GaXIn_{1-X}As/GaYIn_{1-Y}Sb vertical heterojunctionless tunneling field effect transistor

Behzad Rajabi

Rasht Branch, Islamic Azad University, Rasht, Iran

Mahdi Vadizadeh (✉ vadizadeh@gmail.com)

Department of Electrical Engineering, Abhar Branch, Islamic Azad University, Abhar, Iran

<https://orcid.org/0000-0001-7557-0620>

Research Article

Keywords: Junctionless Tunnel FET, mole fraction, tunneling effective mass, sensitivity analysis

Posted Date: March 30th, 2021

DOI: <https://doi.org/10.21203/rs.3.rs-254477/v1>

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Investigation of the impact of mole-fraction on the digital benchmarking parameters as well as sensitivity in $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ vertical heterojunctionless tunneling field effect transistor

Behzad Rajabi ^a, Mahdi Vadizadeh ^{b*}

a) Department of Electrical Engineering, Rasht Branch, Islamic Azad University, Rasht, Iran

b) Department of Electrical Engineering, Abhar Branch, Islamic Azad University, Abhar, Iran*

Abstract

$\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ vertical heterojunctionless tunneling field effect transistor (VHJL-TFET) has been suggested to optimize the digital benchmarking parameters. In the proposed VHJL-TFET with type II heterostructure (i.e. $X=0.8$, $Y=0.85$), slight changes in gate voltage cause switching from OFF-state to ON-state. As a result, the electrical properties of $\text{Ga}_{0.8}\text{In}_{0.2}\text{As}/\text{Ga}_{0.85}\text{In}_{0.15}\text{Sb}$ VHJL-TFET are excellent in the sub-threshold region. The heterostructure with III-V semiconductors in the source-channel region increases the ON-state current (I_{ON}) of the VHJL-TFET. Comparing the results of $\text{Ga}_{0.8}\text{In}_{0.2}\text{As}/\text{Ga}_{0.85}\text{In}_{0.15}\text{Sb}$ VHJL-TFET with the simulated devices with type I heterostructure (i.e. $X=0.9$, $Y=0.1$) and type III heterostructure (i.e. $X=0.1$, $Y=0.4$) shows the improvement by 26% and 15% in the average subthreshold slope (SS). Sensitivity analysis for VHJL-TFET with the type II heterostructure shows that the sensitivity of OFF-state current (I_{OFF}) to the body thickness (T_b) and doping concentration (N_D) is more than the sensitivity of the other main electrical parameters. The $\text{Ga}_{0.8}\text{In}_{0.2}\text{As}/\text{Ga}_{0.85}\text{In}_{0.15}\text{Sb}$ VHJL-TFET with a channel length of 20 nm, $T_b=5$ nm, and $N_D=1\times 10^{18}\text{cm}^{-3}$ showed the $\text{SS}=4.4\text{mV/dec}$, $I_{\text{ON}}/I_{\text{OFF}}=4\text{E}14$, and $I_{\text{ON}}=8\text{mA}/\mu\text{m}$. As a result, $\text{Ga}_{0.8}\text{In}_{0.2}\text{As}/\text{Ga}_{0.85}\text{In}_{0.15}\text{Sb}$ VHJL-TFET can be a reasonable choice for digital applications.

Keywords: Junctionless Tunnel FET; mole fraction; tunneling effective mass; sensitivity analysis.

Declarations

Funding: Not applicable

Conflict of interest: Not applicable

Availability of data and material: Not applicable

Code availability: Not applicable

Authors' contributions: Not applicable

Ethics approval: Not applicable

Consent for publication: Not applicable

Consent for publication: Not applicable

* Corresponding author E-mail Addresses: vadizadeh@gmail.com

Acknowledgments: Not applicable

1. Introduction

Subthreshold slope (SS) of less than 60mV/dec and low leakage current of tunneling field effect transistor (TFET), respectively, causes an increase in switching speed and causes a reduction in static power consumption in digital circuits performance [1–3]. As a result, TFET device has attracted the attention of many researchers for digital applications [4, 5]. However, the ultra-sharp doping concentration gradient in the source/channel and the drain/channel junctions complicates the fabrication process of TFET device in nanometer regime [6, 7]. Recently, a junctionless TFET (JLTFET) has been proposed, in which issues caused by ultra-sharp doping concentration gradient in the source/channel and the drain/channel junctions are eliminated [6–12]. JLTFET is a heavy doped thin film semiconductor, in which the type and level of doping are unchanged throughout the device. In fact, in JLTFET device, the advantages of conventional TFET and junctionless field effect transistor are combined [7, 13].

Silicon-based JLTFET such as conventional silicon based TFET, is suffering from issues caused by low ON-state current (I_{ON}) due to tunneling mechanism [7, 14]. The reason is that the forbidden band width is so large that it reduces the electron tunneling probability in tunneling junction [6, 11]. With the recent progress, the low I_{ON} problem in JLTFET has been resolved by various strategies, such as using small band gap materials [15, 16] gate engineering [17, 18]. and hetero-gate dielectric [11, 19]. The use of III-V materials with staggered/broken bandgaps is suggested to increase I_{ON} in JLTFET [20–23]. III-V materials have improved the performance of the JLTFET device, due to high mobility as well as lower band gap [22, 24]. JLTFET device with hetero structure is called HJL-TFET. In previous works, HJL-TFET structures are presented horizontally [20–23]. It is very complex to create horizontal heterojunction structures in HJL-TFET device. Use of vertical heterojunction in HJL-TFET is feasible and can reduce the chip consumption level in integrated circuits [25].

In this paper, a vertical heterojunctionless tunneling field effect transistor with III-V materials is proposed, which is called VHJL-TFET. $Ga_xIn_{1-x}As$ and $Ga_yIn_{1-y}Sb$ are recommended as a drain-channel material and as the source material, respectively in the proposed structure. The main goal of this study is to optimize the digital benchmarking parameters of $Ga_xIn_{1-x}As/Ga_yIn_{1-y}Sb$ VHJL-TFET in terms of the I_{ON}/I_{OFF} ratio and SS by varying the mole fraction of X and Y.

The simulation results in the OFF-state show that, with changes in X and Y parameters, the type I, type II and type III hetero structures are formed in the source/channel interface. By choosing $X=0.8$ and $Y=0.85$ in the proposed VHJL-TFET device, the type II hetero structure is formed. As a result, with slight changes in gate voltage, the electron tunneling will occur from source valence band to channel conduction band, which can effectively improve the SS and I_{ON} . Our simulation results show that selecting a material with larger band gap in the drain-channel region as well as a material with smaller band gap in the source region in VHJL-TFET device drastically reduce the ambipolarity behavior. Based on the simulation results, the improvement of the SS and ON-state current to OFF-state current (I_{ON}/I_{OFF}) ratio of VHJL-TFET structure with $Y=0.85$ and $X=0.8$ is noticeable compared to the recently proposed structures [11, 12, 18, 21, 22, 26]. With changes in X and Y, in addition to energy band gap and electron affinity, the electron tunneling effective mass and hole tunneling effective mass are also changed [27]. We considered these changes in our simulations. In the VHJL-TFET structure with $Y=0.85$ and $X=0.8$, the effect of changes in structural parameters, such as doping concentration, body thickness, and spacer width between the auxiliary gate and control gate, is investigated on the main electrical parameters. Finally, the performance of the proposed VHJL-TFET device is compared with that of the recently proposed devices.

This article is organized in 4 Sections. The structure of the device and the simulation models are described in Section 2. In Section 3, the simulation results of the VHJL-TFET structure are presented. Finally, the conclusion is provided in Section 4.

2. Device structure and simulation setup

Figure 1 shows the structure of the simulated VHJL-TFET device in this paper. In the simulated structure to increase gate control over the channel, double gate technology is used. In the VHJL-TFET structure shown in Fig. 1, the source, channel, and drain doping is considered the same and of the donor type with value of $N_D=1 \times 10^{18} \text{cm}^{-3}$. $\text{Ga}_x\text{In}_{1-x}\text{As}$ is selected as a drain-channel material and the source is composed of $\text{Ga}_y\text{In}_{1-y}\text{As}$. As shown in Fig. 1, the channel length, body thickness (T_b), and gate dielectric thickness (T_{OX}) are 20nm, 5nm, and 2nm, respectively. Drain/source extension length is 20nm. HfO_2 is considered as a gate dielectric with $K=25$. In the proposed structure, SiO_2 acts between control gate (c-gate) and auxiliary gate (p-gate) as the isolation layer with the thickness of $W_{\text{SiO}_2}=2\text{nm}$. The p-gate work function is 5.9eV and is achieved by considering Pt as the gate electrode [28]. The c-gate work function is 4.3eV and can be obtained as metal using molybdenum with nitrogen implant dose [28]. The structural parameters of the VHJL-TFET device proposed in Fig. 1 are the same as those of HJL-TFET device proposed in [23] and [22]. VHJL-TFET device shown in Fig. 1 is called $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ VHJL-TFET.

In order to simulate the $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ VHJL-TFET, a commercial tool is used. The nonlocal band to band tunneling (BTBT) model is considered to determine the electrical properties of the proposed device. Nonlocal BTBT model considers spatial variations of energy bands and quasi-fermi levels in tunneling path [22, 29]. The Hansch

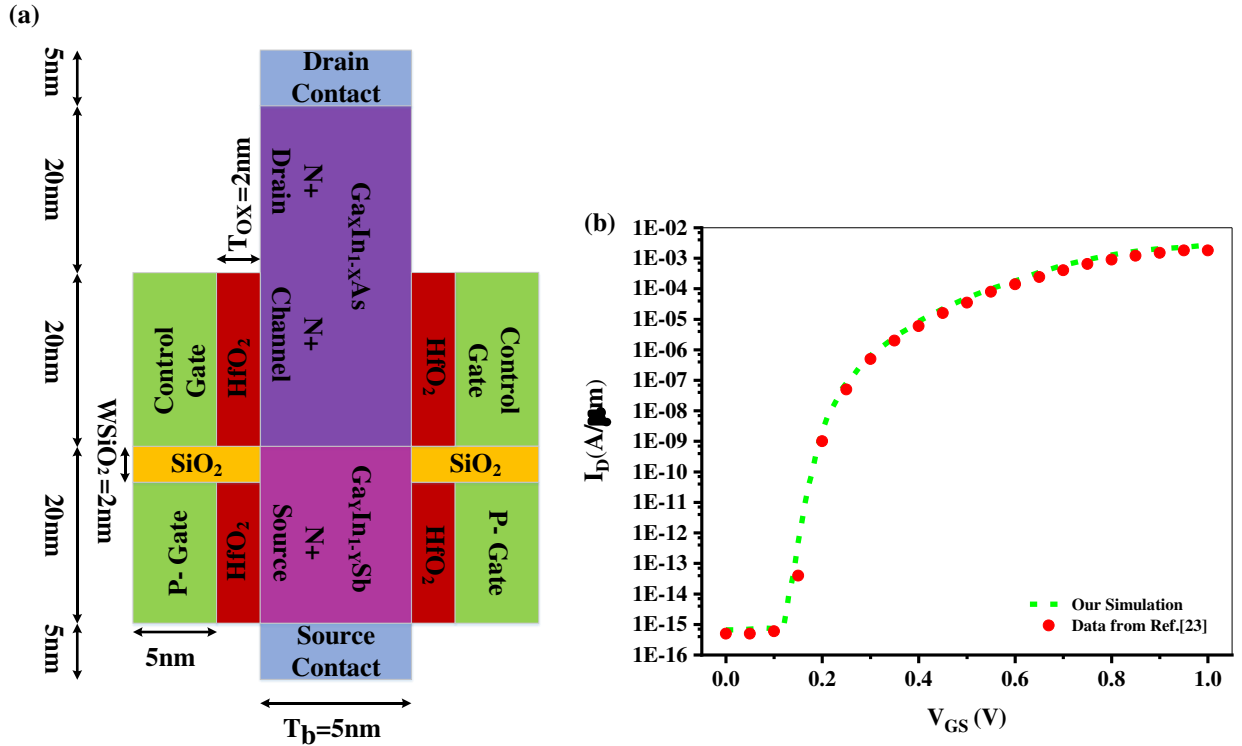


Fig. 1 (a) Device structure of a $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ VHJL-TFET (not to scale) and (b) Calibration with the published result, I_D - V_{GS} characteristics of 20 nm gate length HJL-TFET reported in Ref.[23].

model is used to consider the quantum confinement effect as well as interface defects of oxide/semiconductor [12, 29]. The dependence of the mobility on the vertical electric field, doping concentration, and temperature is considered using Lombardi model [22, 29]. The direct generation/recombination model as well as Shockley–Read–Hall (SRH) recombination model is considered to determine the accurate leakage current value in the simulated devices [22, 29]. Given the high doping density in the proposed device, the band gap narrowing model is used [29, 30]. With changes in X and Y, in addition to changing energy band gap and electron affinity, the electron tunneling effective mass and hole tunneling effective mass are varied [27]. These changes are calculated based on [27] and are

considered in the simulation. The effects of defects and nonsmoothness in the interfacial regions of $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ layers are neglected in our simulations. These effects in real devices flat the I_D - V_{GS} characteristics due to high electric field effects [30]. In $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ VHJL-TFET device, instead of doping junctions in regular TFET devices, there is a junction between two semiconductors with the same doping. Therefore, $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ VHJL-TFET is still categorized as a junctionless device

In order to show the accuracy of our simulations in this paper, we simulated the HJL-TFET with the structural parameters reported in [23]. The HJL-TFET device reported in [23] contains GaAs material in both drain and channel regions, and Ge material in the source region. Figure 1b shows a comparison between our numerical simulations and simulation reported in [23]. Our numerical simulations are performed under the same conditions reported in [23]. As can be seen, the results of our numerical simulations are reasonably consistent with the simulation results reported in [23]. Therefore, the models used in the simulation in this study are sufficiently accurate.

3. Results and Discussion

Equation 1 shows the probability of tunneling in a TFET device, in which Wentzel–Kramers–Brillouin approximation is used [12, 16].

$$T(E) = \exp\left(\frac{-4\lambda\sqrt{m^*}E_g^{\frac{3}{2}}}{3qh(\Delta\phi+E_g)}\sqrt{\frac{\varepsilon_{channel}}{\varepsilon_{oxide}}T_{ox}T_{ch}}\right) \quad (1)$$

Where E_g is energy band gap, h is Planck constant, q is electron charge, λ is screening length, T_{ox} is gate dielectric thickness, and T_{ch} is channel thickness. $\varepsilon_{channel}$ and ε_{oxide} are relative permittivity of channel and gate dielectric, respectively. $\Delta\phi$ is the energy difference between the valence band of the source and the conduction band of the channel, and m^* is tunneling effective mass [16]. In fact, Equation 1 shows that both parameters E_g and m^* play an important role in the performance of the TFET device.

One of the main motivations for this study is to improve performance of $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ VHJL-TFET device proposed with changes in X and Y mole fractions. By changing the X and Y parameters, the electron tunneling effective mass (m_e^*), hole tunneling effective mass (m_h^*), energy band gap and electron affinity (χ) in source, channel and drain regions of $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ VHJL-TFET device are affected, followed by changes in electrical properties of the simulated device.

Equations 2 and 3 show the electron tunneling effective mass and hole tunneling effective mass, respectively, in the drain-channel region ($\text{Ga}_x\text{In}_{1-x}\text{As}$) and source region ($\text{Ga}_y\text{In}_{1-y}\text{Sb}$) [27].

$$\begin{cases} m_e^* = (0.023 + 0.037x + 0.003x^2)m_0 & m_h^* = (m_{hh}^{3/2} + m_{lh}^{3/2})^{2/3} \\ m_{hh} = (0.41 + 0.1x)m_0 \\ m_{lh} = (0.026 + 0.056x)m_0 \end{cases} \quad (2)$$

$$\begin{cases} m_e^* = (0.014 + 0.0178y + 0.0092y^2)m_0 & m_h^* = (m_{hh}^{3/2} + m_{lh}^{3/2})^{2/3} \\ m_{hh} = 0.4m_0 \\ m_{lh} = (0.015 + 0.01y + 0.025y^2)m_0 \end{cases} \quad (3)$$

Where m_0 is the free electron mass, m_{hh} is heavy hole mass, and m_{lh} is light hole mass. In Equations 2 and 3, at various X and Y , $\text{Ga}_x\text{In}_{1-x}\text{As}$ and $\text{Ga}_y\text{In}_{1-y}\text{Sb}$ have direct band gap. Therefore, the electron effective mass is used at Γ valley in the simulation [27].

Equations 4 and 5 show the energy band gap (E_g) and electron affinity (χ), respectively, in the drain-channel region ($\text{Ga}_x\text{In}_{1-x}\text{As}$) and source region ($\text{Ga}_y\text{In}_{1-y}\text{Sb}$) [27].

$$\begin{cases} E_g = 0.36 + 0.63x + 0.43x^2 \\ \chi = 4.9 - 0.83x \end{cases} \quad (4)$$

$$\begin{cases} E_g = 0.172 + 0.139y + 0.415y^2 \\ \chi = 4.59 - 0.53y \end{cases} \quad (5)$$

Figure 2a shows the variations in the energy band gap and electron affinity, and Fig. 2b shows the variations in electron and hole tunneling effective mass in the drain-channel and source regions.

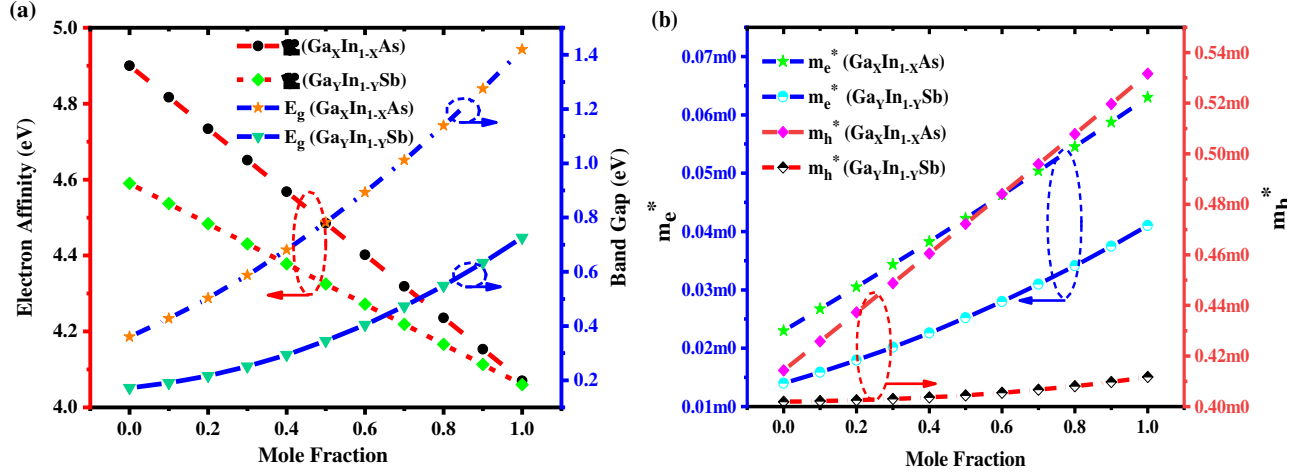


Fig.2 (a) Energy band gap and electron affinity as a function of X and Y mole fractions. (b) Electron tunneling effective mass and hole tunneling effective mass as a function of X and Y mole fractions.

As shown in Fig. 2a, for a given value of $X=Y$, the energy band gap in the source region ($\text{Ga}_y\text{In}_{1-y}\text{Sb}$) is lower than that in the channel region ($\text{Ga}_x\text{In}_{1-x}\text{As}$). Also, for a given value of $X=Y$, with the simultaneous increase in mole fractions, the difference in energy band gap between source ($\text{Ga}_y\text{In}_{1-y}\text{Sb}$) and channel ($\text{Ga}_x\text{In}_{1-x}\text{As}$) is increased. The difference in electron affinity between $\text{Ga}_y\text{In}_{1-y}\text{Sb}$ and $\text{Ga}_x\text{In}_{1-x}\text{As}$ is reduced for a given value $X=Y$ with an increase in mole fractions and, for $X=Y=1$, the electron affinity of the two materials overlaps. Figure 2b shows that for a given value of $X=Y$ with an increase in mole fractions, the tunneling effective mass of the electron and hole is increased for both materials and also the increased effective mass in $\text{Ga}_y\text{In}_{1-y}\text{Sb}$ is negligible.

3.1. Performance evaluation of the VHJL-TFET device for various mole fractions

In this section, for the proposed structure $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ VHJL-TFET, X mole fraction is increased from 0 to 1 with steps of 0.05; for each step of X, Y mole fraction is varied from 0 to 1. For various X and Y changes, the digital benchmarking parameters of $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ VHJL-TFET are investigated.

There are authoritative references [31] that considered I_{ON} as a drain current for bias conditions $V_{\text{GS}}=V_{\text{DS}}=V_{\text{DD}}$ and, I_{OFF} as a drain current for bias conditions $V_{\text{GS}}=0\text{V}$ and $V_{\text{DS}}=V_{\text{DD}}$. In this study, V_{DD} is considered to be 1V. Therefore, the drain current for bias conditions $V_{\text{GS}}=0\text{V}$ and $V_{\text{DS}}=1\text{V}$ is considered as I_{OFF} and the drain current for bias conditions $V_{\text{GS}}=V_{\text{DS}}=1\text{V}$ is considered as I_{ON} [31]. Also, the gate-source voltage for drain current $10^{-7}\text{A}/\mu\text{m}$ is considered as the threshold voltage [31]. Examinations in this study show that changes in X and Y parameters, in addition to changing electron tunneling effective mass and hole tunneling effective mass, would change the energy band profile in the source/channel interface. The changes in energy band profile are in a way that type I, type II, and type III hetero structures are created in the source/channel interface in the OFF-state (see Figure 3 to 6).

Figure 3a shows 2D matrix of I_{OFF} changes and Fig. 3b shows 2D matrix of I_{ON} changes with variations of X and Y parameters. As seen, with changes in X and Y parameters, I_{ON} changes are one order of magnitude and I_{OFF} changes are fourteen orders of magnitude. As a result, sensitivity of I_{OFF} to changes in X and Y parameters, is higher than that of I_{ON} . The regions of type I, type II and type III hetero structures in OFF-state are shown in Fig. 3a. Accordingly, for some X and Y values in the region related to type III hetero structure, I_{OFF} is larger than 10^{-7} A/μm. Therefore, in bias conditions $V_{\text{GS}}=0\text{V}$ and $V_{\text{DS}}=1\text{V}$, the device is not located in the sub-threshold region. Comparison of Fig. 3a and Fig. 2a shows that, with an increase in $X=Y$ in the region related to type II hetero

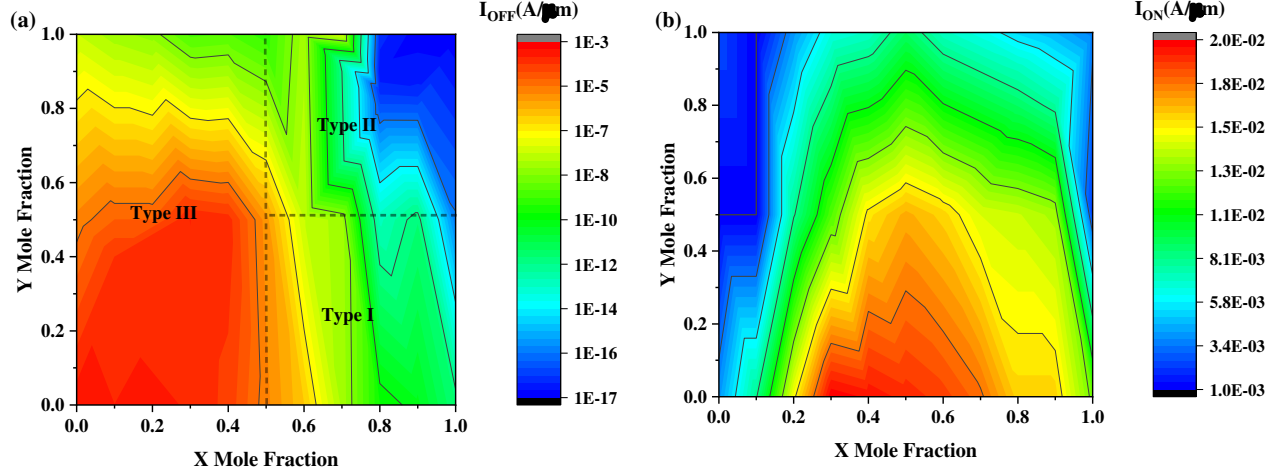


Fig. 3 2D variation matrix of (a) OFF-state current (I_{OFF}) and (b) ON-state current (I_{ON}) as a function of X and Y mole fractions. I_{ON} is measured at bias conditions of $V_{\text{GS}}=1\text{V}$, $V_{\text{DS}}=1\text{V}$. I_{OFF} is measured at bias conditions of $V_{\text{GS}}=0\text{V}$, $V_{\text{DS}}=1\text{V}$.

structure, the electron and hole tunneling effective mass increases. As a result, the probability of tunneling based on Equation 1 is reduced and, consequently, I_{OFF} is decreased. Our simulation results show that the tunneling width is reduced in ON-state for the values of X and Y in the red region in Fig. 3b. As a result, I_{ON} is increased in this region for the proposed $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ VHJL-TFET device.

Average SS in TFET is one of the most important parameters to evaluate switching performance from I_{OFF} to I_{ON} . In

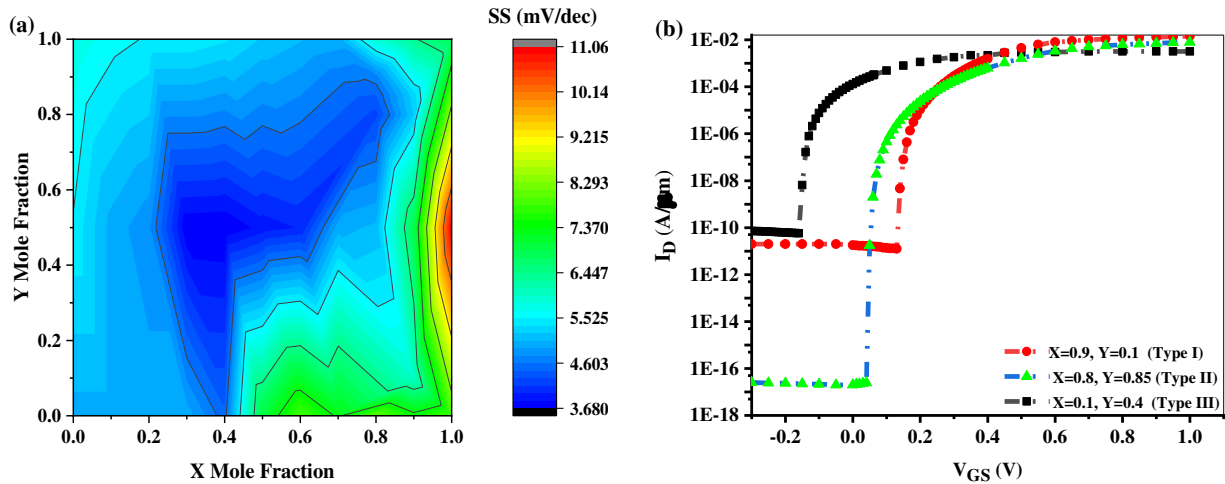


Fig.4 (a) 2D variation matrix of average subthreshold slope (SS) as a function of X and Y mole fractions. 1 V. Average SS of simulated structures has been calculated based on the method discussed in [22, 32]. (b) Input characteristics of $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ VHJL-TFET for type I ($X=0.9$, $Y=0.1$), type II ($X=0.8$, $Y=0.85$) and type III ($X=0.1$, $Y=0.4$), the bias condition is $V_{\text{DS}}=1\text{V}$.

this study, the average SS is considered between a point where the drain current is raised with an increase in gate voltage and threshold voltage [22, 32]. Figure 4a shows the contour of the changes in average SS by changing the X and Y parameters. The lower average SS in $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ VHJL-TFET indicates higher switching rate [15, 22, 32].

In this study, the optimal selection of X and Y values to improve the digital benchmarking parameters of $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ VHJL-TFET device are carried out by considering the following priorities:

1. I_{OFF} must be of the fA/um order or smaller, because in TFET devices, the I_{OFF} is expected to be of the fA/um order at the most [32].
2. Average SS must be smaller than 10mV/dec, because the TFET device with $\text{SS} < 10\text{mV/dec}$ is very suitable for sub-0.5V supply voltage applications [11, 33].
3. I_{ON} must be of the mA/um order, because in TFET devices with I_{ON} from mA/um order, it can be said that the problems caused by the decreased I_{ON} are eliminated [15–18, 22].

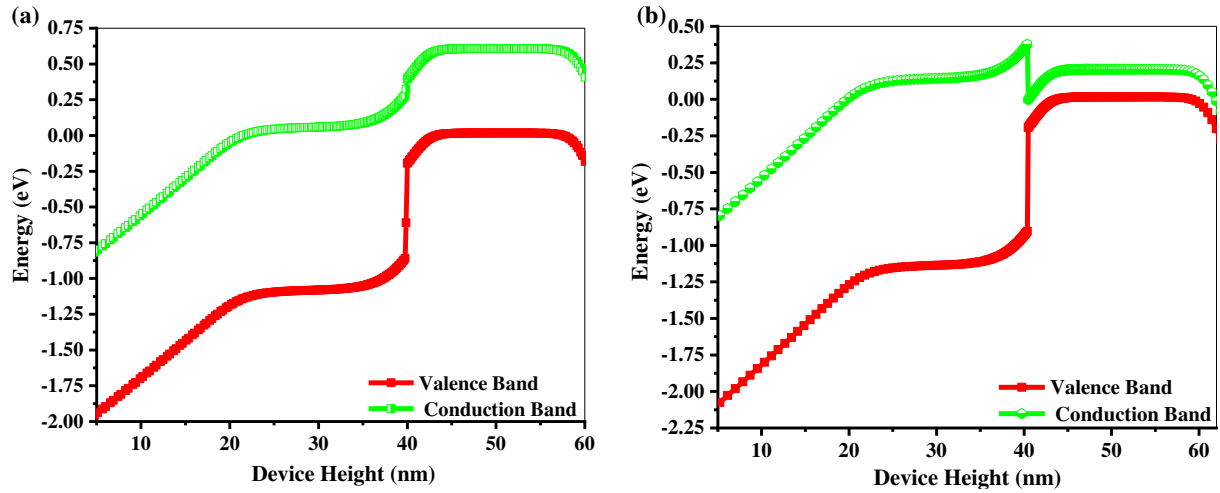


Fig.5 Energy band diagram, taken vertically across the $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ VHJL-TFET for (a) typeII (X=0.8, Y=0.85) and (b) typeI (X=0.9, Y=0.1). The bias conditions are as follows $V_{\text{GS}}=0\text{V}$, $V_{\text{DS}}=1\text{V}$.

According to the priorities mentioned above, the optimal mole fractions are selected equal to X=0.8 and Y=0.85 to improve the performance of the proposed $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ VHJL-TFET structure. In $\text{Ga}_{0.8}\text{In}_{0.2}\text{As}/\text{Ga}_{0.85}\text{In}_{0.15}\text{Sb}$ VHJL-TFET device shown in Fig. 1, we have $I_{\text{OFF}}=0.02\text{fA/um}$, $I_{\text{ON}}=8\text{mA/um}$, $\text{SS}=4.4\text{mV/dec}$. The contours of Fig. 3a show that, for X=0.8 and Y=0.85, the I_{OFF} is reduced compared to other values of X and Y. The contours of Fig. 3b also show that, for X=0.8 and Y=0.85, I_{ON} of the proposed device is reasonable compared to the other values of X and Y. As a result, in the proposed device for X=0.8 and Y=0.85, $I_{\text{ON}}/I_{\text{OFF}}$ ratio is increased. The contour of Fig. 4a also shows the average SS of $\text{Ga}_{0.8}\text{In}_{0.2}\text{As}/\text{Ga}_{0.85}\text{In}_{0.15}\text{Sb}$ VHJL-TFET device is smaller than 10mV/dec, and is improved compared to other values of X and Y.

For studying the band structure of the proposed $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ VHJL-TFET device, it is not possible to display the energy band profile for all X and Y values. In this study, X=0.9, Y=0.1 and X=0.8, Y=0.85, and X=0.1, Y=0.4 are considered for the hetero structure of type I, type II, and type III, respectively. Fig. 4b shows the current-voltage input characteristic of the simulated devices for different values of X and Y. As seen:

1. I_{OFF} of the simulated device with X=0.8, Y=0.85 is much lower than the other simulated devices.
2. $\text{Ga}_{0.8}\text{In}_{0.2}\text{As}/\text{Ga}_{0.85}\text{In}_{0.15}\text{Sb}$ VHJL-TFET device is turned ON for gate voltage of less than 0.1V.

3. I_{ON} of the simulated devices is approximately the same.
4. The simulated device with $X=0.1$ and $Y=0.4$ has the I_{OFF} larger than $7A/\mu m$. Therefore, it will not turn off at $V_{GS}=0V$.

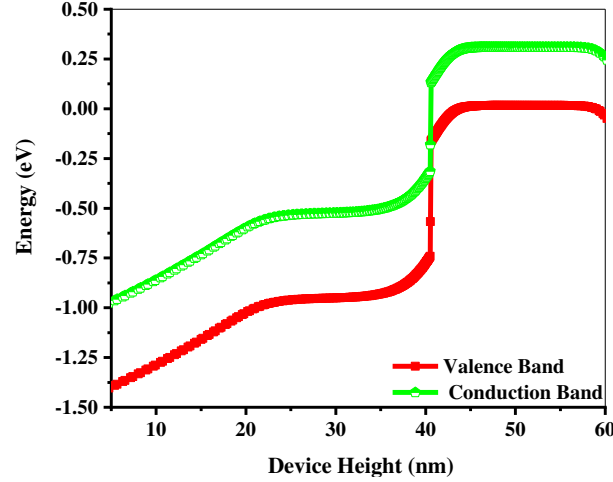


Fig. 6 Energy band diagram, taken vertically across the $Ga_{0.1}In_{0.9}As/Ga_{0.4}In_{0.6}Sb$ VHL-TFET (i.e. typeIII).

Figure 5a and Fig. 5b show the energy band profile for simulated structures with $X=0.8$ and $Y=0.85$ (type II hetero structure) and $X=0.9$ and $Y=0.1$ (type I hetero structure) in bias conditions of OFF-state. In addition, the energy band profile in bias conditions of OFF-state for $X=0.1$ and $Y=0.4$ (type III hetero structure) is shown in Fig. 6. Figure 7a compares the energy band diagram of type I, type II, and type III hetero structures in vicinity of the source/channel interface in OFF-state for the simulated structures.

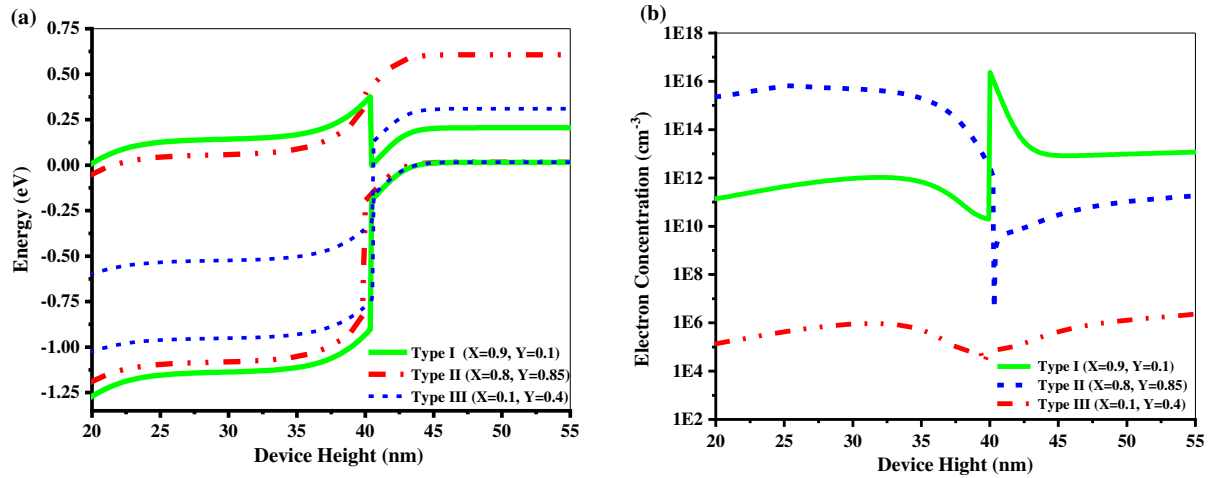


Fig. 7 (a) Energy band diagram comparison and (b) electron concentration comparison between type I, type II, and type III heterostructures at the vicinity of the source/channel interface. The bias conditions are as follows $V_{GS}=0V$, $V_{DS}=1V$.

Overlap of source valence band and channel conduction band for $X=0.8$ and $Y=0.85$ is small enough to not allow the electron tunneling from the source valence band to the channel conduction band (see Fig. 5a). Additionally, for $X=0.8$ and $Y=0.85$, electron tunneling effective mass and hole tunneling effective mass are increased (see Fig. 2b). As a result, in the OFF-state, the probability of electron tunneling from the source valence band to the channel conduction band based on Equation 1 is reduced, followed by significant degradation in I_{OFF} . Despite the increased

tunneling effective mass for $X=0.8$ and $Y=0.85$ compared to the other X and Y values, I_{ON} of the proposed device is reasonable. This is because for $X=0.8$ and $Y=0.85$ in ON-state, the increased tunneling effective mass is compensated for by reduced tunneling barrier width in source/channel interface. Given that $\text{Ga}_{0.8}\text{In}_{0.2}\text{As}/\text{Ga}_{0.85}\text{In}_{0.15}\text{Sb}$ VHJL-TFET is turned on for gate voltage below 0.1V.

In the OFF state, high overlap of source valence band and channel conduction band in the type III hetero structure allows electron tunneling (see Fig. 6). As a result, the I_{OFF} of $\text{Ga}_X\text{In}_{1-X}\text{As}/\text{Ga}_Y\text{In}_{1-Y}\text{Sb}$ VHJL-TFET is increased with $X=0.1$ and $Y=0.4$. The simulation results show that the quantum well formed in the conduction band in the source/channel interface for the type I hetero structure (see Fig. 5b). Accordingly, electron concentration is increased in the source/channel interface, see Fig. 7b. As a result, channel conductance is increased, followed by I_{OFF} increases. For simulated structures, I_{OFF} of type I is larger than that of type II and less than that of type III.

By examining energy band profile of $\text{Ga}_X\text{In}_{1-X}\text{As}/\text{Ga}_Y\text{In}_{1-Y}\text{Sb}$ VHJL-TFET with type II hetero structure ($X=0.8$, $Y=0.85$) in OFF-state, it can be said that with slight changes in gate voltage, the Zener breakdown occurs in source/channel interface. As a result, the device switches from I_{OFF} to I_{ON} . Moreover, the I_{OFF} in $\text{Ga}_X\text{In}_{1-X}\text{As}/\text{Ga}_Y\text{In}_{1-Y}\text{Sb}$ VHJL-TFET with type II hetero structure is from fA/ μm order.

Our simulation results show that using a material with a larger band gap in the drain-channel region and a material with a smaller band gap in the source region in proposed VHJL-TFET (i.e. $E_{g\text{GaXIn}_{1-X}\text{As}} > E_{g\text{GaYIn}_{1-Y}\text{Sb}}$) significantly reduces the ambipolarity behavior. This result is compatible with another study [23].

3.2.Importance of structural parameters in performance of VHJL-TFET device

Simulations carried out in this study show that the doping concentration (N_D), body thickness (T_b), and spacer width between PG and CG (W_{SiO_2}) are among the most important design parameters for the performance of VHJL-TFET

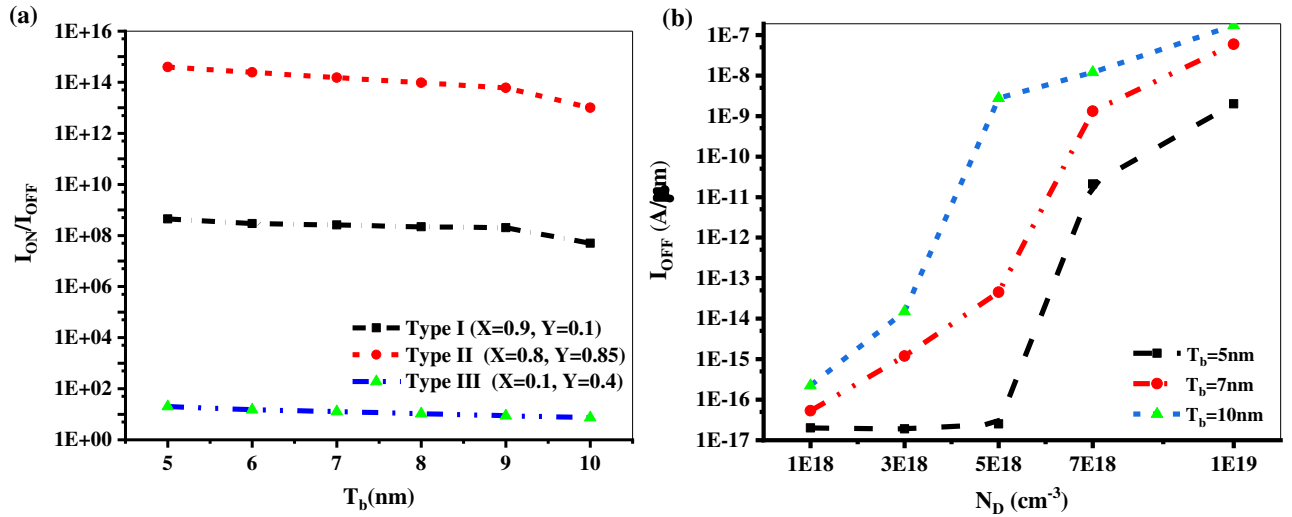


Fig. 8 (a) I_{ON}/I_{OFF} current ratio as a function of body thickness (T_b) of $\text{Ga}_X\text{In}_{1-X}\text{As}/\text{Ga}_Y\text{In}_{1-Y}\text{Sb}$ VHJL-TFET with $N_D=1 \times 10^{18} \text{cm}^{-3}$ for various mole fractions. (b) I_{OFF} as a function of doping concentration (N_D) of $\text{Ga}_{0.8}\text{In}_{0.2}\text{As}/\text{Ga}_{0.85}\text{In}_{0.15}\text{As}$ VHJL-TFET for various body thicknesses. I_{ON} is measured at bias conditions of $V_{GS}=1\text{V}$, $V_{DS}=1\text{V}$. I_{OFF} is measured at bias conditions of $V_{GS}=0\text{V}$, $V_{DS}=1\text{V}$.

device.

I_{ON}/I_{OFF} ratio as a function of T_b for different types of hetero structures is shown in Fig. 8a. As seen, the I_{ON}/I_{OFF} ratio for a given type is increased by reducing T_b . Simulation results show by reducing T_b , the CG ability to deplete

the channel is increased in the OFF-state. Consequently, channel resistance is increased by reducing T_b , and the I_{OFF} is significantly reduced. This is reflected in the increased I_{ON}/I_{OFF} ratio.

As shown in Section 3.1, the high overlap of the source valence band and channel conduction band in the simulated devices with type III hetero structure increases the I_{OFF} . As a result, the increased I_{ON}/I_{OFF} ratio by reducing T_b for $Ga_{0.1}In_{0.9}As/Ga_{0.4}In_{0.6}Sb$ VHJL-TFET is negligible (see Fig. 8a). Also, Fig. 8a shows the I_{ON}/I_{OFF} ratio for a given T_b for $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET is larger than the devices simulated with type I and type III hetero structures, because I_{OFF} of the simulated device with type II hetero structure is less than other simulated devices.

Our simulation results show that the sensitivity of the I_{OFF} to increased N_D is higher than the sensitivity of I_{ON} . In fact, the channel resistance depends on N_D , accordingly, N_D plays an important role in determining drain current. Channel resistance has been decreased due to positive control gate voltage in the ON-state, and its value is smaller than channel resistance in the OFF-state. As a result, the sensitivity of the I_{OFF} to increased N_D is higher than the sensitivity of I_{ON} .

We investigated the performance of $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET in OFF-state for different N_D s between $1E18$ and $1E19$. Figure 8b shows I_{OFF} as a function of N_D for different body thickness of $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET. Our simulation results for a given T_b show that, the channel resistance is reduced in OFF-state by increasing N_D . As a result, the I_{OFF} is increased (see Fig. 8b). Also, the CG ability to deplete the channel is increased by T_b reducing for a given N_D in OFF-state; therefore, I_{OFF} is decreased.

The slope of the I_{OFF} versus N_D curve increases by increasing N_D , and this is more pronounced for larger body thicknesses, see Fig. 8b. First, the curve slope increases slowly and, then, increases rapidly. The rapid increase of slope for larger T_b s begins at smaller N_D s. As a result, as T_b increases, the sensitivity of I_{OFF} to N_D increases. As

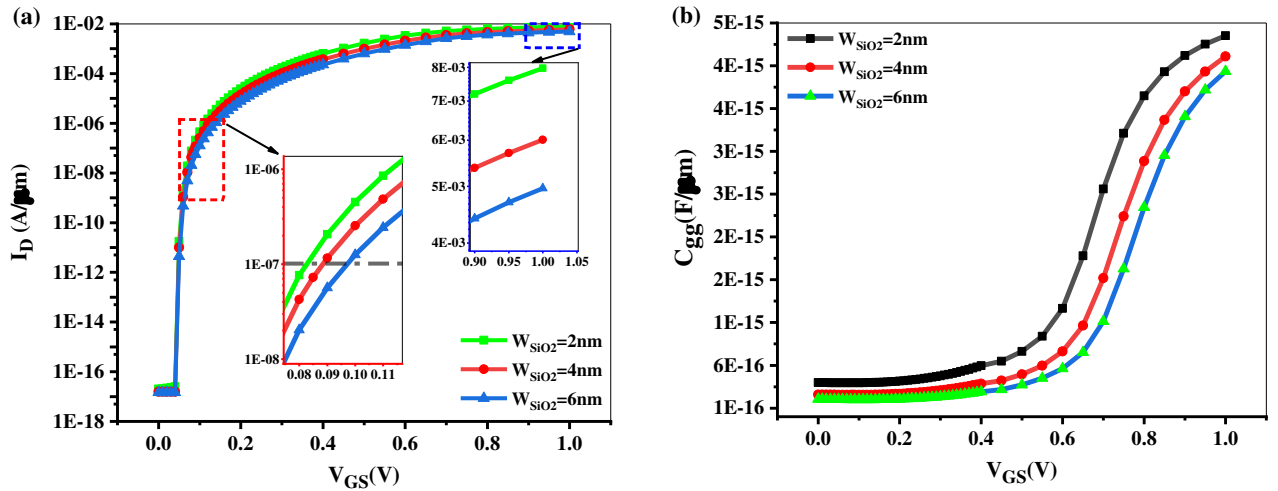


Fig.9 (a) Drain current and (b) the total gate-to-gate capacitance as a function of gate bias of $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}As$ VHJL-TFET for various W_{SiO2} . The inset of Fig. 9(a) shows the I_D - V_{GS} of simulate device in above threshold region. The bias condition is $V_{DS}=1V$.

expected, with an increase in N_D for more CG control over the channel, the body thickness should be thinner.

The simulation results show that the performance of $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET is dependent on the W_{SiO2} . In this study, to investigate the effect of W_{SiO2} on the performance of the proposed $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET in Fig. 1, W_{SiO2} is varied from 2nm to 6nm. Figure 9a shows the I_D - V_{GS} characteristic of $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET for various values of W_{SiO2} . The inset of Fig. 9a shows the performance of

the simulated devices in the above threshold region. As W_{SiO_2} increases, the slope of the energy band diagram at the tunneling junction is reduced in the source/channel interface. As a result, electron tunneling in ON-state is reduced followed by decreased I_{ON} . This is reflected in larger values by threshold voltage shift (see Fig. 9a). Based on the simulations, as W_{SiO_2} varies from 2nm to 6nm, I_{ON} is reduced by 37%.

The total gate-to-gate capacitance (C_{gg}), plays an important role in determining the intrinsic gate delay of a transistor (τ) for digital applications [22]. Figure 9b shows C_{gg} as a function of V_{GS} for $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET and for various values of W_{SiO_2} . We assume $V_{DS}=V_{DD}=1V$ for calculating C_{gg} and sweep gate voltage between 0 and 1V at a frequency of 1MHz [22]. Our simulation results show that, with an increase in W_{SiO_2} , the gate-source capacitance decreases. As a result, C_{gg} is reduced, which is more evident in the above threshold region.

Intrinsic gate delay (τ) is as follows [22, 30].

$$\tau = \frac{C_{gg} V_{DD}}{I_{ON}} \quad (6)$$

Table 1 Intrinsic gate delay comparison for various W_{SiO_2} in the $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET device.

W_{SiO_2}	I_{ON} (mA/ μ m)	C_{gg} (fF/ μ m)	Delay(τ) (pS/ μ m)
2nm	8	4.54	0.57
4nm	6	4.21	0.70
6nm	5	4.04	0.81

Where $V_{DD}=1V$ refers to supply voltage and I_{ON} refers to ON-state current. Table 1 compares the values of τ , I_{ON} and C_{gg} in bias conditions $V_{GS}=V_{DS}=1V$. To calculate τ , the device width is considered to be $1\mu m$ [22, 30]. As expected, with an increase in W_{SiO_2} , I_{ON} and C_{gg} are decreased. According to Equation 2, I_{ON} has a direct impact and C_{gg} has an

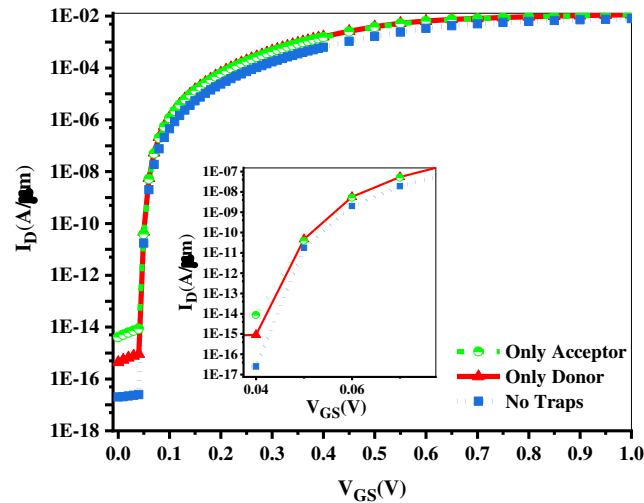


Fig. 10 The I_D - V_{GS} characteristic in the presence of the defect in the source/channel interface. defect in the source/channel interface has negligible effects on the ON-state current, however, the OFF-state current has been affected noticeably by considering defect.

inverse impact on τ . As a result, I_{ON} and C_{gg} are in competition to determine τ . The results in Table 1 show, in determination of τ , I_{ON} degradation overcome C_{gg} degradation. Consequently, as W_{SiO_2} increases, τ is increased.

It should be noted that an increase in W_{SiO_2} to values larger than 2nm might be a feasible way of bringing up the breakdown voltage of oxide between CG and PG; but the device performance is degraded. W_{SiO_2} degradation to values smaller than 2nm might lead to oxide breakdown between CG and PG. As a result, W_{SiO_2} is considered to be 2nm in our simulations.

3.3. Impact of Band-Tails on the subthreshold behavior of $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJLTFT

Our simulation results show that band tailing due to defect in the source/channel interface is thus of importance on subthreshold performance in the proposed structure. Defects in the $GaInAs/GaInSb$ interface can be of the donor or acceptor type, and their density may vary between 10^5 - 10^7 cm⁻² [34, 35]. In this section, to investigate the effect of defect in the source/channel interface on the performance of $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJLTFT, the donor type defect density is 10^6 cm⁻² and the acceptor type defect density is 10^7 cm⁻². Figure 10 shows the I_D - V_{GS} characteristic of the simulated devices. It can be seen that the interface defects increase the OFF-State current, followed by an increase in the subthreshold slope, see inset of Fig. 10. The OFF-state current and average SS for the proposed structure with only acceptor type defect are $4.17E-15$ (A/ μ m) and 4.9mV/dec respectively, and the same parameters for the proposed structure with only donor type defect are $4.45E-16$ (A/ μ m) and 4.3 mV/dec. Comparing the result of the simulated device without defect with the simulated device with only acceptor type defect and only donor type defect shows the increasing by 36% and 20% in the average SS.

Figure 11(a) shows the square root of the product of the electron-hole density $(np)^{1/2}$ taken vertically across the tunneling junction of simulated devices in the OFF-state. As shown, $(np)^{1/2}$ by taking defects into account in the source/channel interface is higher than the $(np)^{1/2}$ when the defect is absent. Figure 11b compares the recombination rate taken vertically across the tunneling junction of simulated devices in the OFF-state. As can be seen, the defects have shifted the maximum recombination rate to the source/channel interface. Moreover, the maximum recombination rate by taking defects into account is higher than the maximum recombination rate when the defect is absent. In fact, the defects increase the product of the electron-hole density in source/channel interface, followed by

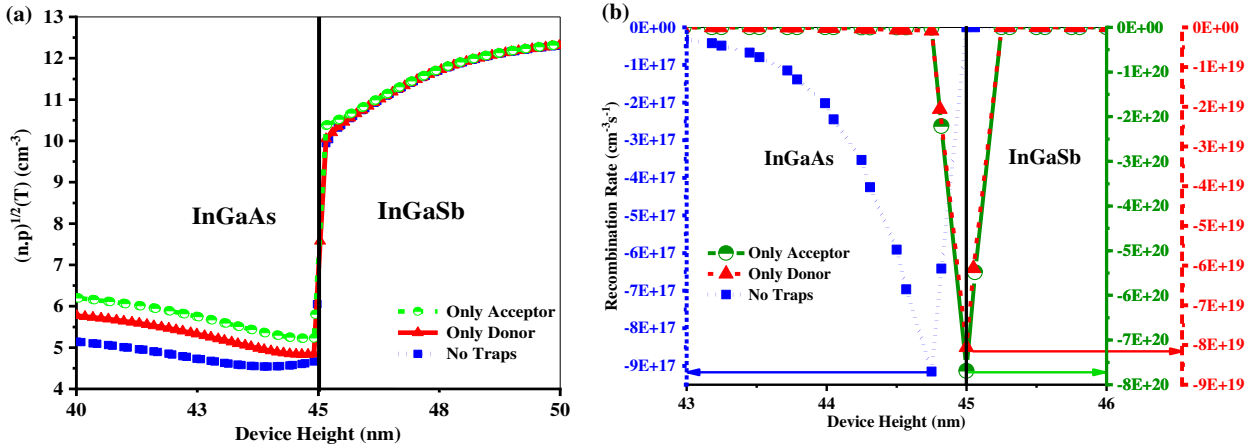


Fig.11 (a) Square product of electron-hole density and (b) recombination rate, taken vertically at the vicinity of the tunneling junction of the simulated structures in the OFF-state. The bias conditions are as follows: $V_{GS} = 0V$ and $V_{DS} = 1V$.

an increase in the recombination rate. As a result, the OFF-state current by taking defects into account is higher than the OFF-state current when the defect is absent. The higher I_{OFF} due to defect results in the deteriorating the subthreshold behavior of simulated devices.

3.4. Sensitivity analysis

The simulation results in this section have been presented without taking the defect of the source/channel interface into account. To obtain the sensitivity of the main electrical parameters of the $\text{Ga}_{0.8}\text{In}_{0.2}\text{As}/\text{Ga}_{0.85}\text{In}_{0.15}\text{Sb}$ VHJL-TFET to structural parameters, such as T_b , N_D and W_{SiO_2} , the sensitivity analysis is conducted. We considered I_{ON} , I_{OFF} , $I_{\text{ON}}/I_{\text{OFF}}$ ratio, threshold voltage (V_{th}), and average SS as the main electrical parameters of VHJL-TFET. In this study, sensitivity is considered as standard deviation divided by mean. In calculating the sensitivity of a main electrical parameter to a given structural parameter, other structural parameters are considered constant. Figure 12 shows the sensitivity of main electrical parameters of $\text{Ga}_{0.8}\text{In}_{0.2}\text{As}/\text{Ga}_{0.85}\text{In}_{0.15}\text{Sb}$ VHJL-TFET with respect to the structural parameters. To calculate the sensitivity of the main electrical parameters with respect to N_D , it is assumed that $T_b=5\text{nm}$ and $W_{\text{SiO}_2}=2\text{nm}$, and N_D is varied from 5×10^{17} to 1×10^{19} . The I_{OFF} of the simulated device has higher sensitivity than other main electrical parameters with respect to the N_D (see Fig. 12). As N_D increases, the channel resistance decreases and, then, the I_{OFF} is increased.

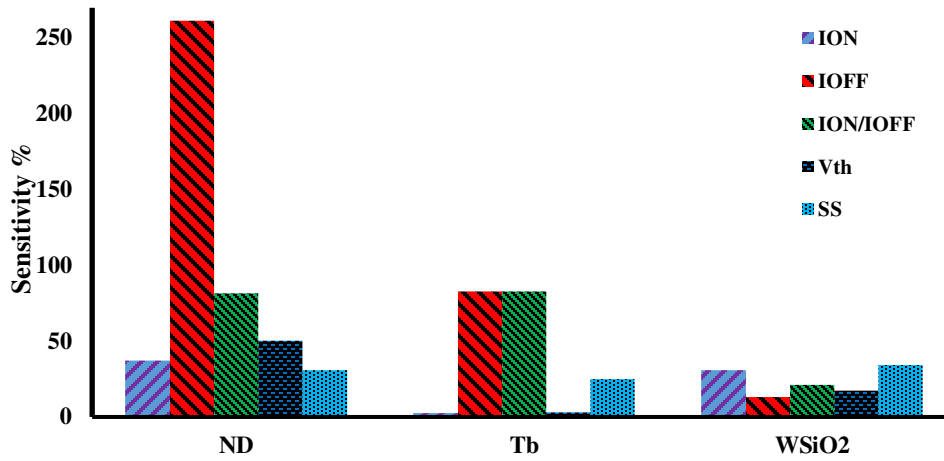


Fig.12 Sensitivity of main electrical parameters with respect to N_D , T_b , and W_{SiO_2} .

To calculate the sensitivity of the main electrical parameters with respect to T_b , $N_D=1 \times 10^{18}$ and $W_{\text{SiO}_2}=2\text{nm}$ are assumed and T_b is varied from 5nm to 10nm . Figure 12 shows that I_{OFF} has higher sensitivity to T_b than other main electrical parameters. The simulation results show, with an increase in T_b , the CG control over channel is decreased and, then, the I_{OFF} increases.

To calculate the sensitivity of the main electrical parameters with respect to W_{SiO_2} , $N_D=1 \times 10^{18}$ and $T_b=5\text{nm}$ are assumed and W_{SiO_2} varies from 2nm to 8nm . As W_{SiO_2} increases, slope of the energy band diagram in the source/channel interface is reduced and, then, I_{ON} is reduced. As seen in Fig. 9, I_{ON} has higher sensitivity to W_{SiO_2} than other main electrical parameters.

Performance of $\text{Ga}_{0.8}\text{In}_{0.2}\text{As}/\text{Ga}_{0.85}\text{In}_{0.15}\text{Sb}$ VHJL-TFET shown in Fig. 1 is compared with the performance of the recently proposed devices in Table 2. Dual material gate heterostructure junctionless TFET (DMGE-HJLTFET) proposed in [18] has a hetero structure of $\text{GaAs}_{0.1}\text{Sb}_{0.9}/\text{InAs}$. Oxide pocket hetero-gate-dielectric heterostructure. JLTFTFET (OP-HD-HS-JLTFTFET) proposed in [21] has a hetero structure of Si/GaSb . Heterostructure junctionless TFET (HJL-TFET) proposed in [22] has a hetero structure of GaAs/GaSb . The devices in Table 2 that are selected for comparison with the VHJL-TFET structure have a 20nm channel length and 5nm body thickness; the results expressed for them are extracted from [18, 21, 22]. Table 2 shows that $\text{Ga}_{0.8}\text{In}_{0.2}\text{As}/\text{Ga}_{0.85}\text{In}_{0.15}\text{Sb}$ VHJL-TFET structure proposed in this paper with the channel length of 20nm and body thickness of 5nm has higher $I_{\text{ON}}/I_{\text{OFF}}$ ratio than the structures reported in [18, 21, 22]. Moreover, average SS of $\text{Ga}_{0.8}\text{In}_{0.2}\text{As}/\text{Ga}_{0.85}\text{In}_{0.15}\text{Sb}$ VHJL-TFET in

comparison with DMGE-HJLTFET, OP-HD-HS-JLTFET, and HJLTFET is improved by 71%, 77%, and 66%, respectively. As a result, the switching rate from I_{OFF} to I_{ON} of $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET is higher than that of the structures reported in [18, 21, 22]. The results in Table 2 show the I_{ON} of $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET is improved by 204% compared to HJL-TFET and improved by at least one order of magnitude compared to structures OP-HD-HS-JLTFET and DMGE-HJLTFET. Threshold voltage of $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET compared to OP-HD-HS-JLTFET and HJL-TFET is reduced by 76% and 64%, respectively (see Table 2). As a result, $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET has turned on with a smaller gate voltage in comparison with OP-HD-HS-JLTFET and HJL-TFET devices. It's necessary to say for the faire comparison all parameters are compared in the absence of $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ interface defects.

Table 2 Switching behavior comparison between the $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET and the recently proposed devices [18, 21, 22].

Designes	I_{ON} (A/ μm)	I_{OFF} (A/ μm)	I_{ON}/I_{OFF}	SS (mV/dec)	V_{th} (V)
DMGE-HJLTFET [18]	5.46E-04	8.40E-18	6.50E+13	15.4	-----
OP-HD-HS-JLTFET [21]	4.69E-4	5.419E-17	8.66E+12	19	0.33
HJL-TFET [22]	2.63E-03	3.548E-17	7.4E+13	13	0.22
VHJL-TFET	8.00E-03	2.00E-17	4.00E+14	4.4	0.08

Due to the tunneling mechanism, the I_{ON} of TFET is less than devices in which the current mechanism is thermionic emission. This is the main restriction of the TFET device. I_{ON} of $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET proposed in this paper is compared with the devices, in which the current mechanism is thermionic emission. Nanotube junctionless FET (NJLTFET) proposed in [36] with 30nm gate length has $I_{ON}=24.9 \mu A$. Junctionless field effect diode (JL-FED) proposed in [28] with a 30nm channel length has $I_{ON}=0.1mA/\mu m$. Our simulation results show that $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET proposed here with a 30nm channel length has $I_{ON}=8mA/\mu m$. The I_{ON} $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET is higher than that of the recently proposed devices [28, 36]. Consequently, there is no low I_{ON} restriction in proposed $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET device.

4. Conclusion

In this paper, the effects of changes in indium mole fraction (X) in the drain-channel region and Y in the source region are comprehensively examined by numerical simulator to improve digital benchmarking parameters of $Ga_XIn_{1-X}As/Ga_YIn_{1-Y}Sb$ VHJL-TFET. With changes in X and Y, type I, type II and type III hetero structures are formed in the source/channel interface. For $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET (type II hetero structure), there is a small overlap between source valence band and channel conduction band in OFF-state. Additionally, electron and hole tunneling effective mass is increased. Thus, I_{OFF} is decreased significantly. Simulation results for $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET in ON-state showed that electron and hole tunneling effective mass is compensated for by reducing tunneling barrier width. Moreover, in the proposed device, III-V semiconductors are used throughout the device. As a result, I_{ON} of $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET is reasonable, which meet the requirements of international technology roadmap for semiconductors. $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET with a 20nm channel length has $I_{ON}/I_{OFF}=4E14$ and $SS=4.4mV/dec$ and could be a good candidate for digital applications. Also, in the proposed device, we has $I_{ON}=8mA/\mu m$ and maximum transconductance is 19mS/ μm . As a result, the proposed device could be reasonable for analog applications.

Changes in structural parameters on the performance of $Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}Sb$ VHJL-TFET are examined. Our simulation results show that, with an increase in doping concentration in the proposed device, the CG control over

the channel decreases; therefore, I_{OFF} is increased. Also, as W_{SiO_2} increases, the slope of the energy band diagram decreases in source/channel interface and the I_{ON} is reduced. As a result, τ is raised by increasing W_{SiO_2} . The results represented that the I_{OFF} has higher sensitivity to doping concentration and body thickness than other main electrical parameters. Furthermore, the sensitivity of I_{ON} to W_{SiO_2} is higher than that of I_{OFF} to W_{SiO_2} .

All the results reported in this study are regardless of the effects of defects in interfacial regions of $\text{Ga}_x\text{In}_{1-x}\text{As}/\text{Ga}_y\text{In}_{1-y}\text{Sb}$ layers. For more accurate results, minor improvements can be applied for considering defects in the simulation.

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Figures

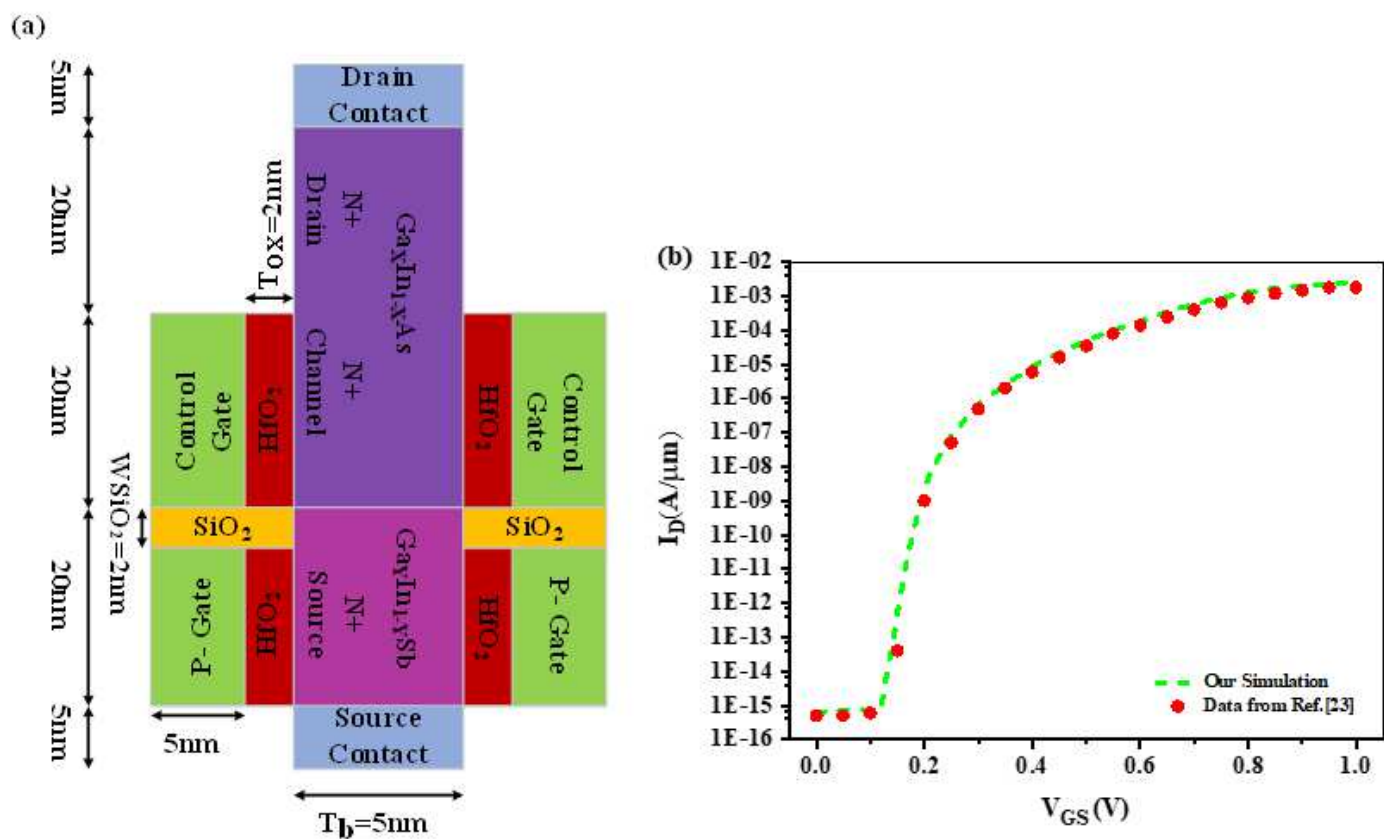


Figure 1

(a) Device structure of a GaXIn1-XAs/GaYIn1-YsSb VHJL-TFET (not to scale) and (b) Calibration with the published result, ID-VGS characteristics of 20 nm gate length HJL-TFET reported in Ref.[23].

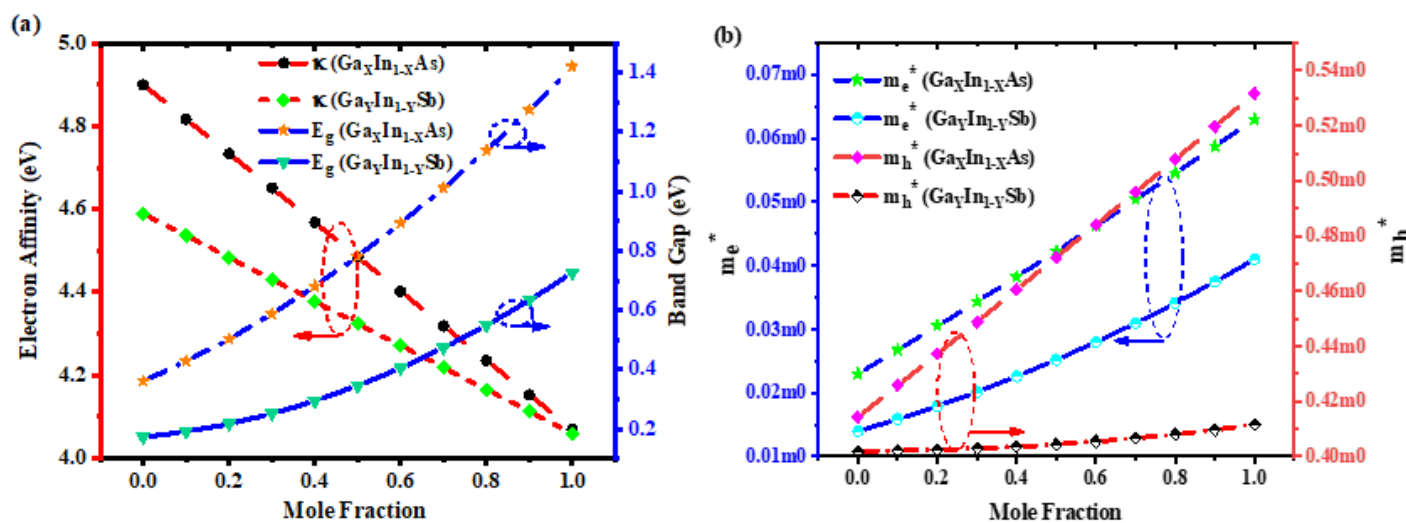


Figure 2

(a) Energy band gap and electron affinity as a function of X and Y mole fractions. (b) Electron tunneling effective mass and hole tunneling effective mass as a function of X and Y mole fractions.

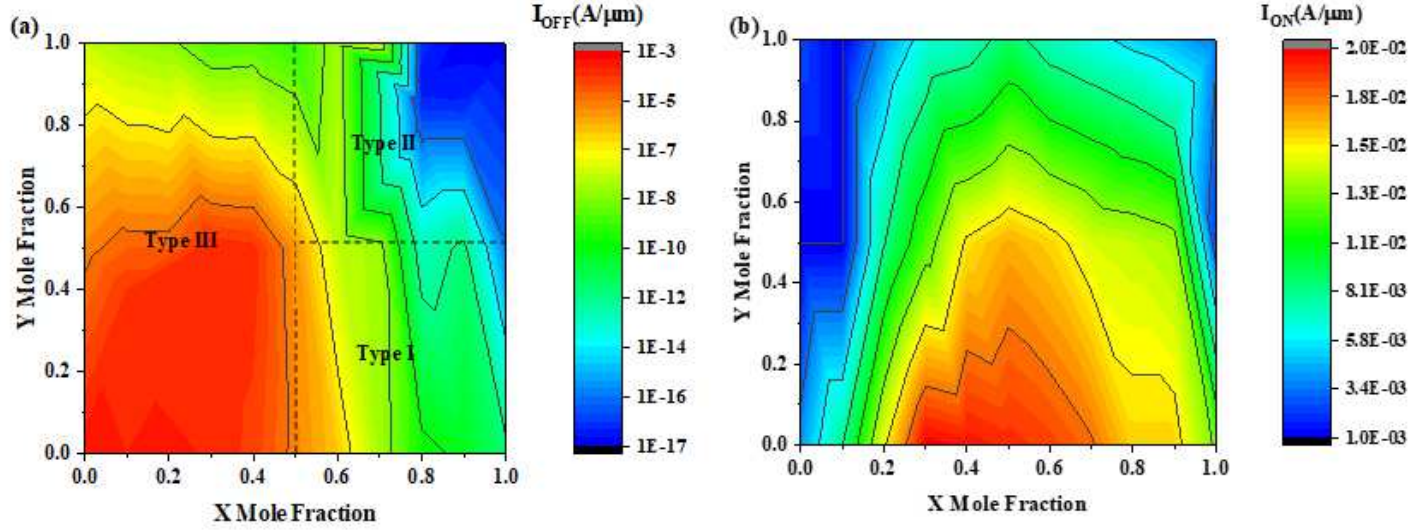


Figure 3

2D variation matrix of (a) OFF-state current (I_{OFF}) and (b) ON-state current (I_{ON}) as a function of X and Y mole fractions. I_{ON} is measured at bias conditions of $V_{GS}=1V$, $V_{DS}=1V$. I_{OFF} is measured at bias conditions of $V_{GS}=0V$, $V_{DS}=1V$.

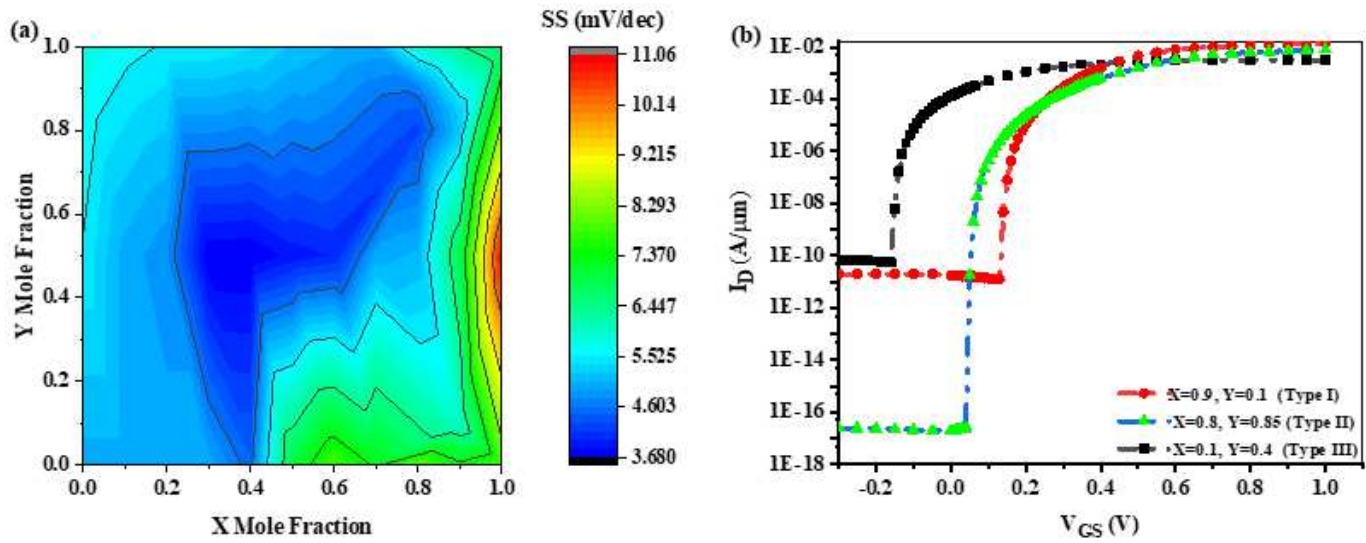


Figure 4

(a) 2D variation matrix of average subthreshold slope (SS) as a function of X and Y mole fractions. 1 V. Average SS of simulated structures has been calculated based on the method discussed in [22, 32]. (b) Input characteristics of GaXIn1-XAs/GaYIn1-YSb VHJL-TFET for typeI ($X=0.9, Y=0.1$), typeII ($X=0.8, Y=0.85$) and typeIII ($X=0.1, Y=0.4$), the bias condition is $V_{DS}=1V$.

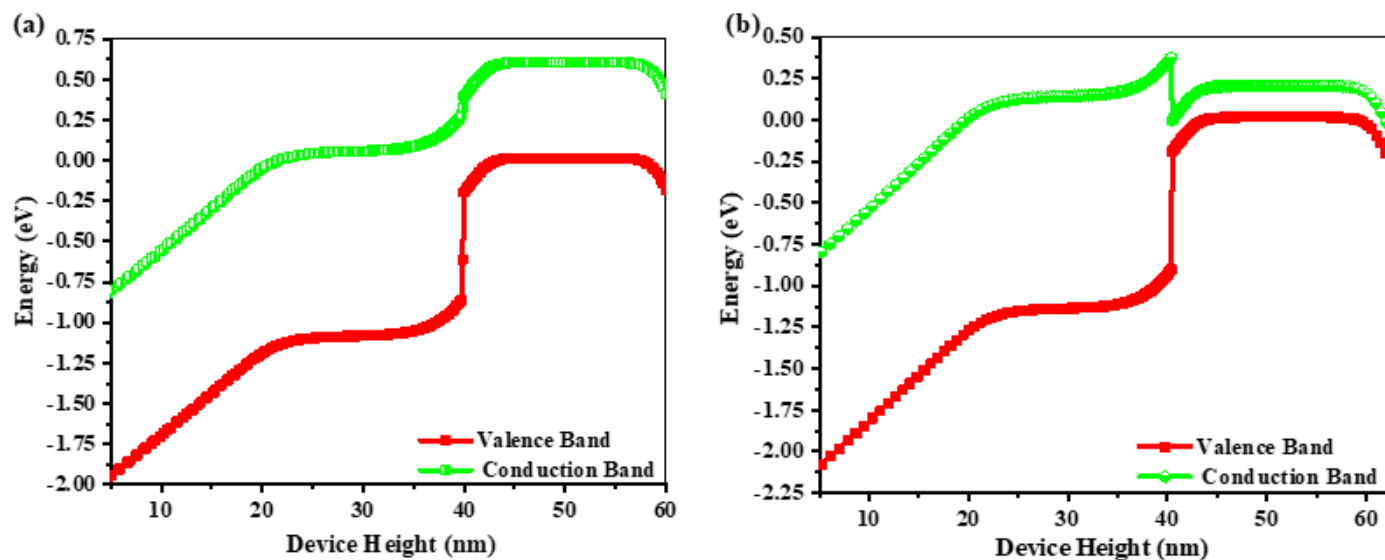


Figure 5

Energy band diagram, taken vertically across the GaXIn_{1-X}As/GaYIn_{1-Y}Sb VHJL-TFET for (a) type I ($X=0.8$, $Y=0.85$) and (b) type II ($X=0.9$, $Y=0.1$). The bias conditions are as follows $V_{GS}=0V$, $V_{DS}=1V$.

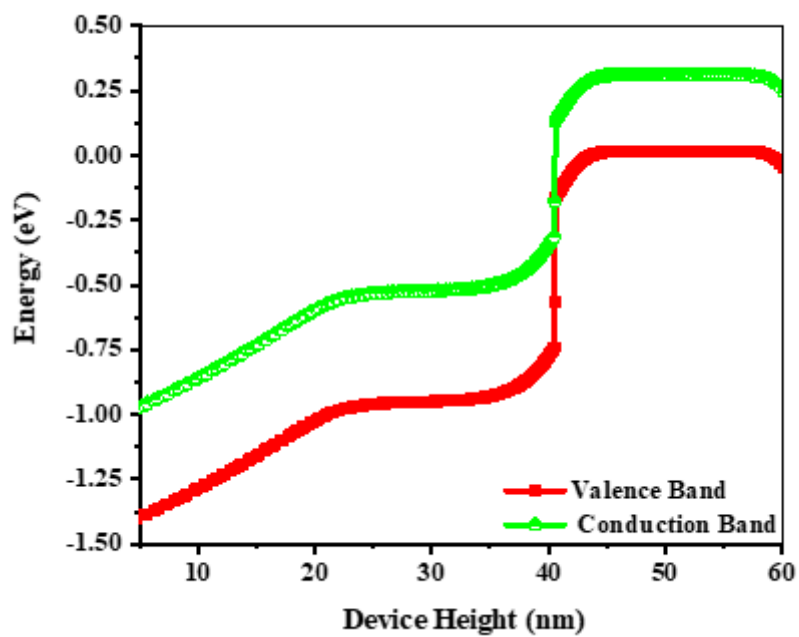


Figure 6

Energy band diagram, taken vertically across the Ga_{0.1}In_{0.9}As/Ga_{0.4}In_{0.6}Sb VHJL-TFET (i.e. type II).

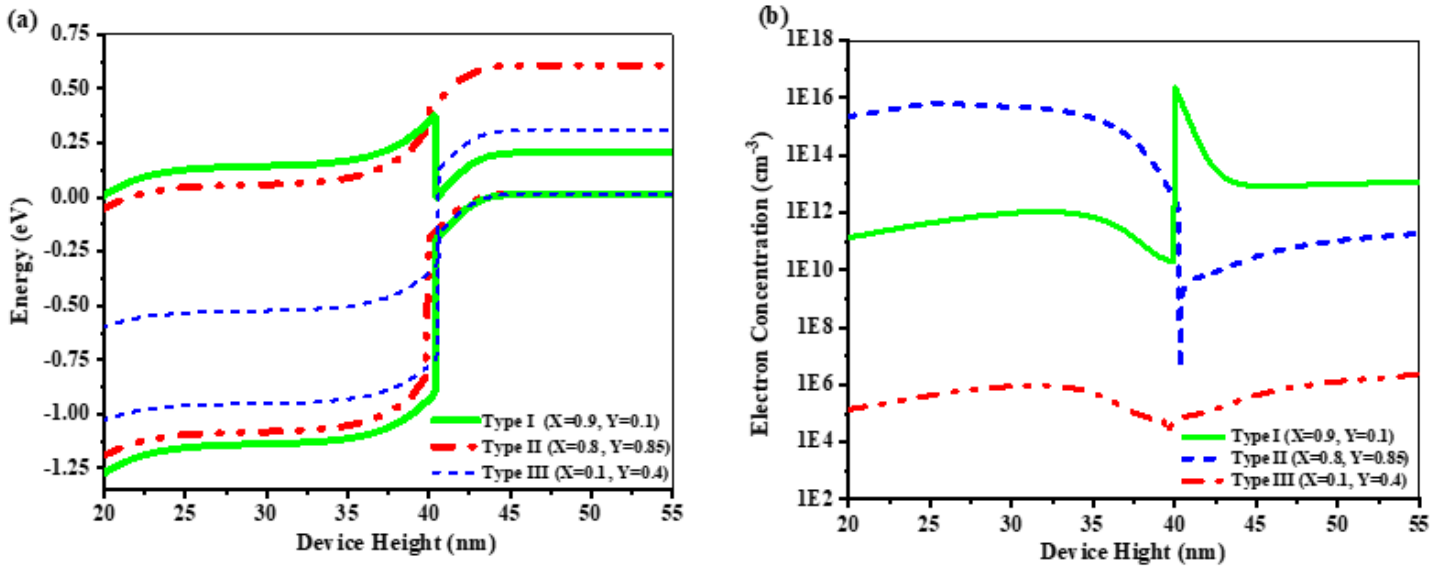


Figure 7

(a) Energy band diagram comparison and (b) electron concentration comparison between type I, type II, and type III heterostructures at the vicinity of the source/channel interface. The bias conditions are as follows $V_{GS}=0V$, $V_{DS}=1V$.

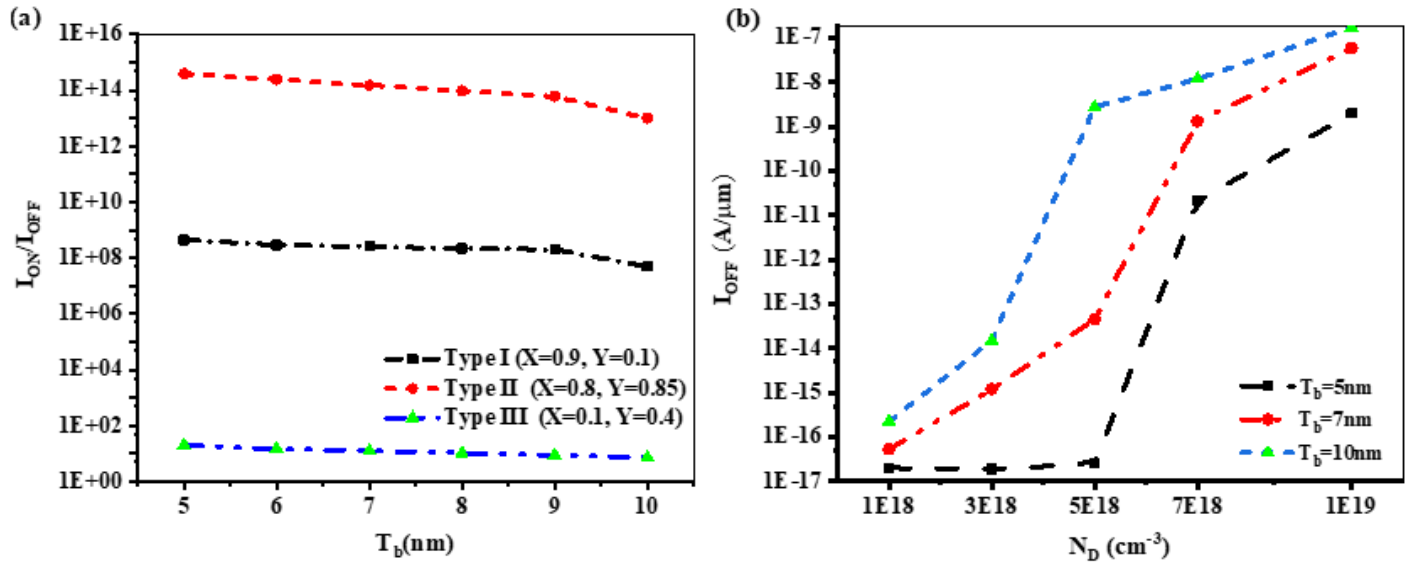


Figure 8

(a) ON/OFF current ratio as a function of body thickness (T_b) of GaXIn_{1-X}As/GaYIn_{1-Y}Sb VHJL-TFET with $N_D=1 \times 10^{18} \text{cm}^{-3}$ for various mole fractions. (b) IOFF as a function of doping concentration (N_D) of Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}As VHJL-TFET for various body thicknesses. I_{ON} is measured at bias conditions of $V_{GS}=1V$, $V_{DS}=1V$. IOFF is measured at bias conditions of $V_{GS}=0V$, $V_{DS}=1V$.

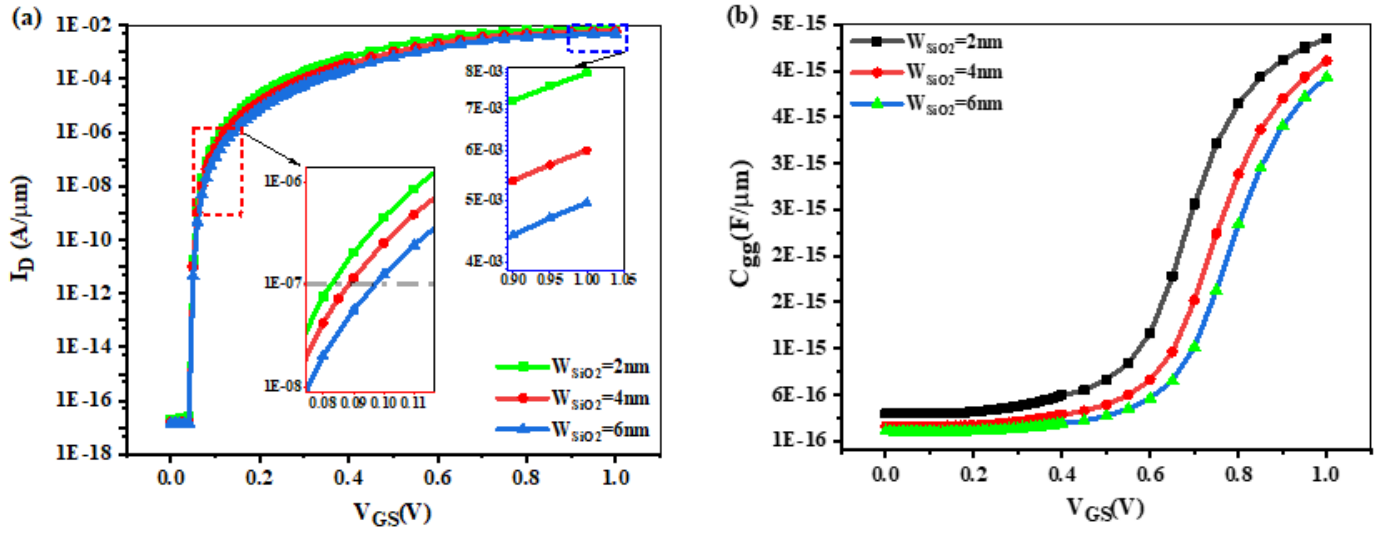


Figure 9

(a) Drain current and (b) the total gate-to-gate capacitance as a function of gate bias of Ga_{0.8}In_{0.2}As/Ga_{0.85}In_{0.15}As VHJL-TFET for various W_{SiO_2} . The inset of Fig. 9(a) shows the I_D - V_{GS} of simulate device in above threshold region. The bias condition is $V_{DS}=1\text{V}$.

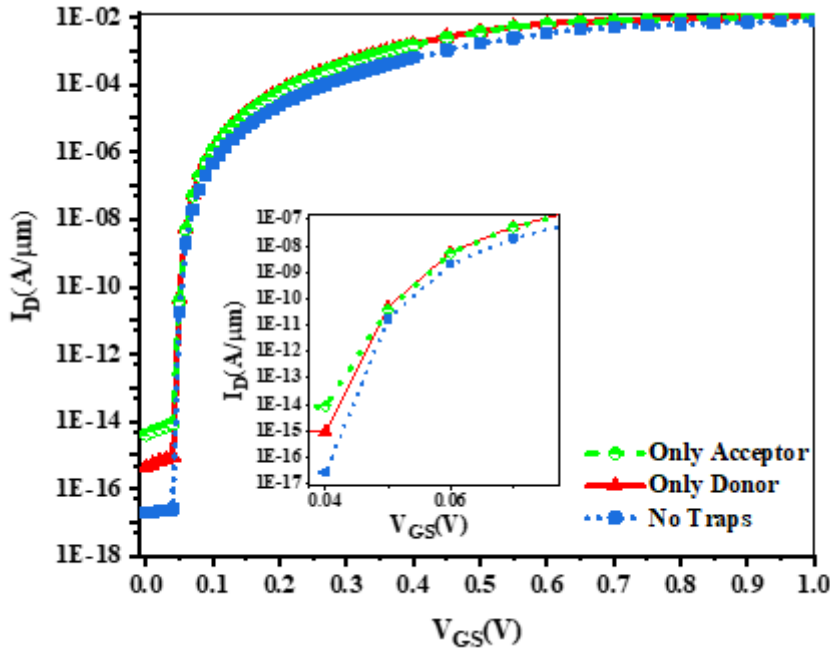


Figure 10

The I_D - V_{GS} characteristic in the presence of the defect in the source/channel interface. defect in the source/channel interface has negligible effects on the ON-state current, however, the OFF-state current has been affected noticeably by considering defect.

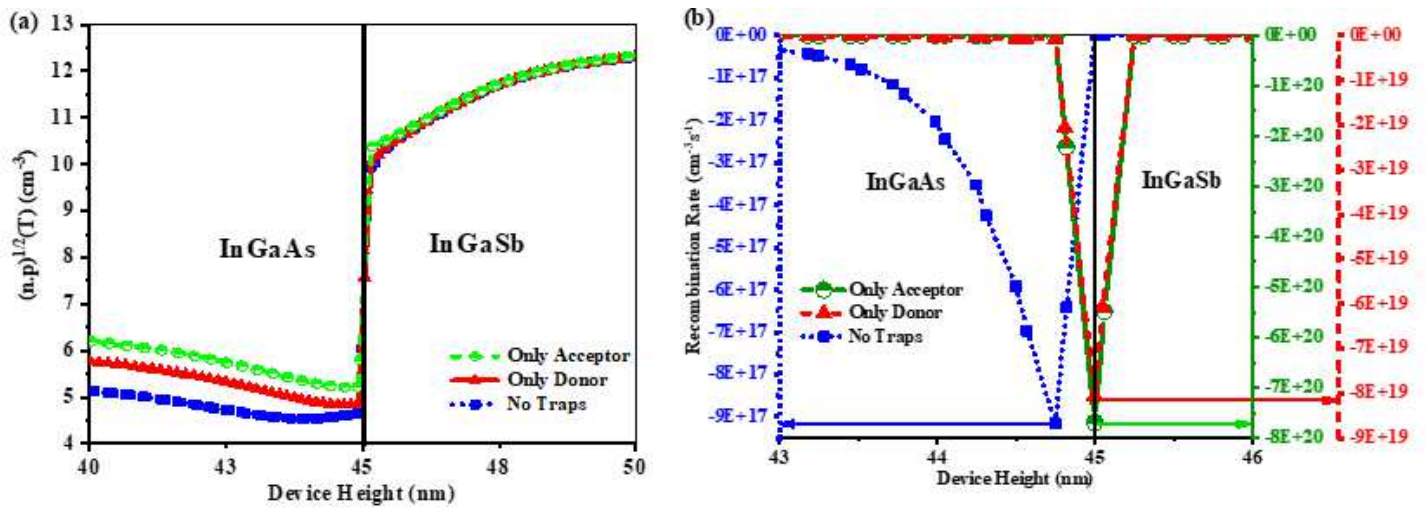


Figure 11

(a) Square product of electron-hole density and (b) recombination rate, taken vertically at the vicinity of the tunneling junction of the simulated structures in the OFF-state. The bias conditions are as follows: VGS = 0V and VDS = 1V.

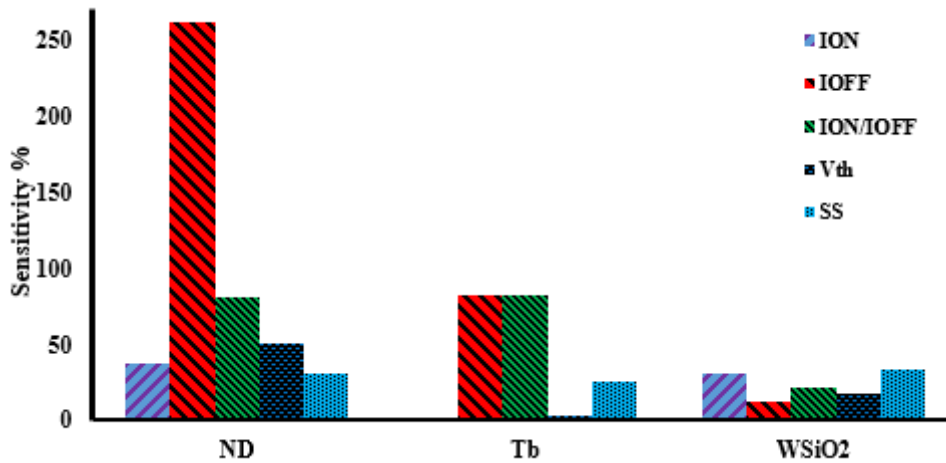


Figure 12

Sensitivity of main electrical parameters with respect to ND, Tb, and WSiO2.