A Compact Zero Bias Diode Detector with Harmonic Rejection for Radar System Application

Sadhana Kumari (sadhanak.ece@bmsce.ac.in)
BMS College of Engineering Bengaluru

Naveen Kumar Maurya
Vishnu Institute of Technology Bhimavaram

K N Madhusudhan
BMS College of Engineering Bengaluru

Research Article

Keywords: Detector, Low pass filter, Stepped impedance resonator, Schottky diode

Posted Date: February 7th, 2023

DOI: https://doi.org/10.21203/rs.3.rs-2522792/v1

License: This work is licensed under a Creative Commons Attribution 4.0 International License.
Read Full License
Abstract

In this paper it is aimed to design and develop a passive detector by employing a Schottky Barrier Diode (SBD) with zero bias. For this work a low cost commercially available Schottky barrier diode SMS7630-079LF is adopted. A compact multi stopband resonator has been incorporated to improve the sensitivity of the detector by attenuating the RF signal up to fourth harmonic at the detector output port. The entire module is based on microstrip circuit and consequently very easy and cheap to fabricate, which fulfils the low-cost necessities of radar system assembling. To validate this method, a prototype of the proposed detector is developed for 2.26 GHz, with a board size of 0.44\(\lambda_g\) x 0.36\(\lambda_g\). The measured outcomes confirm the suppression of the fundamental signal frequency by nearly 23.8 dB along with other high order harmonic suppression.

I. Introduction

Detector is one of the most important component in wireless communication receiver section and is considered as a transition between RF and DC signal.

In general, conventional detectors are composed of an input matching network, a diode and a carrier suppressor realized by a RF shorting capacitor. However, different applications altering this basic configuration according to the requirements. An emergence of high-performing planar Schottky Barrier Diode (SBD) has paved the way of designing a high-performing non-linear circuit design. With high cut-off frequency has propped up high performing non-linear circuit design. Nowadays growing demand of high-speed components made this device a potential candidate for passive circuit. It’s low potential barrier, very small forward voltage along with low junction capacitance, make it an excellent choice for power detection at high frequency. Another added advantage of SBD based detectors is low cost and simple design [1]. However, being a non-linear device diode based passive detector produces harmonics, and these harmonics consume a significant amount of power, which leads to low power sensitivity. Apart from sensitivity, noise generated due to harmonics is another issue.

A simple solution to cater the detector sensitivity is to use DC biasing for the diode [2]. Nevertheless, it consumes DC power.

A low pass RC filter using lumped component is a conventional way to suppress the fundamental component in detector circuit. However, implementing a low pass filter (LPF) using passive component is not a good idea where the power is main constraint. In addition, this kind of LPF cannot attain wide stopband to suppress several harmonics of the incoming signal.

Another way to reduce the non-linearity and increase the sensitivity is to adopt a balanced circuit configuration. A balanced circuit configuration is a useful mean to cancel the odd harmonic signal components completely provided if the devices used in the two out of phase branch in balanced configuration is electrically matched. There are various techniques available in the open literature to employ this configuration, for example balun, rat-race hybrid coupler, branch line coupler and power
divider. In [3]–[4], an ultra-wideband balun is used for balanced configuration of the detector circuit. Improved linearity can be achieved by this arrangement. However, these methods make the system more complicated, and requires a large implementation area too.

In this paper, a simple low-cost detector configuration is introduced. As a substitute of a low-pass filter, stepped impedance resonator (SIR) [5] is used to suppress the carrier and other high order harmonic.

A prototype of the proposed configuration has been realized in hybrid MMIC form with low-cost SBD (SMS7630-079LF), and implemented on 0.8 mm thick Roger substrate (RO4003) substrate having dielectric constant \( \varepsilon_r \) 3.55 and loss tangent \( \tan \delta \) 0.0027.

This paper is organized as follows. Section II illustrates the design and simulation of the proposed detector circuit. Section III describes hardware realization, comparison of simulated and measured results. Finally, concluding remarks before the reference are included in Section IV.

II. Proposed Circuit Description

Proposed detector configuration is shown in Fig. 1. It consists of three parts; a) matching network at the input side, b) non-linear device (SMS7630-079LF) spice model parameters of which is listed in Table I, and (c) a bandstop filter (BSF).

A. Design of a Multiband Bandstop Filter (BSF)

The main limitation of conventional detectors is the low-pass filter realized by the RF shorting capacitor and the load impedance, to suppress the RF signal. However, the suppression of RF signal at the output port is important.

Though BSF can be realized by conventional transmission using open stubs, it has a narrow stopband which bounds the system performance [5] and harmonic suppression. In literature, there are various reported configurations available for BSF realization using stepped impedance [6]–[8]. However, to make the configuration very simple, BSF has been realized using a single open stub with stepped impedance. SIR schematic and its S-parameters are shown in Fig. 2.

Two impedances of the SIR section (shown in Fig. 2(a)) are \( Z_1 = 115 \Omega \), \( Z_2 = 35 \Omega \) with \( 90^\circ \) electrical lengths for each transmission line at 3.39 GHz. This specific selection of impedances and line length has been made to target the stop bands at fundamental signal frequency (RF input signal @2.26 GHz) and its second harmonic. In addition to these two frequency bands 4th (9.04 GHz) and 5th (11.36 GHz) harmonic components of the input RF signal have also been suppressed, which can be clearly seen from the S-parameter plot of the SIR section depicted in Fig. 2(b).

B. Design of the Detector
After designing a SIR section as a BSF, the design of detector circuit as a single module has been started. An additional open-stub \( (90^\circ \text{ at } 2.26 \text{ GHz}) \) is used to suppress the third harmonic of RF signal \( (6.78 \text{ GHz}) \). This stub not only suppresses the third harmonic but also helps to improve the fundamental RF signal suppression level.

As the embedding impedance of the SBD differs from the RF source impedance \( (50 \Omega) \), a matching network at the input side is needed for an efficient transfer of the RF input power. In order to provide a proper matching for the RF signal \( \text{at } 2.26 \text{ GHz} \) a short-circuited stub is integrated into the input port at a certain distance from SBD is added. Next, BSF along with a designed matching network is integrated with the SBD and a non-linear analysis is performed for getting an optimal solution for the output voltage.

As the RF input signal along with its significant harmonics is rejected by employing a BSF and a quarter-wave stub \( (@2.26 \text{ GHz}) \) on the output side there is no need of employing RC based low pass filter as it is being utilized in conventional diode detectors. A pictorial view of final layout is shown in Fig. 3.

### Table 1

<table>
<thead>
<tr>
<th>Parameter</th>
<th>( I_s )</th>
<th>( R_s )</th>
<th>( N )</th>
<th>( C_{J0} )</th>
<th>( E_g )</th>
<th>( I_{BV} )</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Unit</strong></td>
<td>A</td>
<td>( \Omega )</td>
<td>-</td>
<td>pF</td>
<td>eV</td>
<td>A</td>
</tr>
<tr>
<td><strong>Value</strong></td>
<td>5E-06</td>
<td>20</td>
<td>1.05</td>
<td>0.14</td>
<td>0.69</td>
<td>1E-04</td>
</tr>
</tbody>
</table>

### III. Fabrication And Measurements

Proposed circuit of passive detector is printed on the RO4003 Roger substrate. Figure 4. shows the photograph of the printed prototype of the detector circuit and the measurement setup. For the proposed detector 16 mV DC voltage is obtained at the output of the detector for an input power of -30 dBm at 2.26 GHz, which indicates good sensitivity of the designed detector circuit.

Table II. Measured Rejection Level at Output

<table>
<thead>
<tr>
<th>Frequency (GHz)</th>
<th>2.26</th>
<th>4.52</th>
<th>6.78</th>
<th>9.04</th>
<th>11.36</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rejection at output port (dB)</td>
<td>30</td>
<td>32</td>
<td>35</td>
<td>18</td>
<td>41</td>
</tr>
</tbody>
</table>

The measured rejection level of the fundamental signal along with its different harmonics are tabulated in Table II. The plotted graph of detector sensitivity with different input RF power is shown in Fig. 5. This figure incorporates the output voltage graph for the proposed detector along with the one proposed in [9]. This figure clearly indicates that at lower input power level both the detector gives quite a similar
performance. However, for high level of input power proposed detector sensitivity is better. Furthermore, a significant reduction in the size is also achieved as compared to the detector circuit reported in [9].

Iv. Conclusion

The work carried out in this paper is dedicated to make a simple and compact zero bias detector circuit. This structure eliminates the RC based LPF. In lieu of RC based LPF microstrip multi-stopband resonator has been implemented. The overall circuit implementation area of the circuit excluding SMA connector is $0.44\lambda_g \times 0.36\lambda_g$, where $\lambda_g$ is guided wavelength at 2.26 GHz. This structure is very simple and easy to fabricate. Due to high frequency measurement limitation, the design idea has been exemplified at 2.26 GHz. However, the design idea presented in this paper can be easily implemented in high frequency range by choosing high cut off frequency SBD. The designed detector can find its application in Radar systems.

Declarations

Ethical Approval

Not applicable.

Competing interests

Not applicable.

Authors' contributions

First author “Sadhana Kumari” has designed and analyzed the proposed structure, second author “Naveen Kumar Maurya” has done the measurement and plotted all figures and the third author “Madhusudan K N” has drafted the manuscript.

Funding

Not applicable

Availability of data and materials

Not applicable

References


**Figures**

![Proposed detector configuration.](image)

**Figure 1**

Proposed detector configuration.
Figure 2

Stepped Impedance Resonator (a) schematic (b) S-parameters plot.
Figure 3

Layout of Detector Circuit with unit in mm (represented in length/width).
Figure 4

Proposed detector (a) fabricated prototype and (b) measurement set-up
Figure 5

Measured output voltage