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Monolithic three-dimensional (3D) integration of two-dimensional (2D) field effect transistors

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Abstract: Three-dimensional (3D) integration is an emerging technology that is revolutionizing the semiconductor industry. On one hand, it enables the packaging of more devices per unit volume, also referred to as “More Moore”, while on the other hand, it empowers multifunctionality, also known as “More than Moore”, both of which are key toward the development of low-cost, energy-efficient, and high-performance smart electronic systems. While silicon-based 3D integrated circuits (ICs) are already commercially available, there is limited effort on 3D integration of emerging nanomaterials such as two-dimensional (2D) materials despite their novel functionalities that may benefit many applications. Here we demonstrate monolithic 3D integration of a large volume (in excess of 600 transistors in each tier) of aggressively scaled field effect transistors (FETs) based on monolayer MoS2 at low-thermal budget (with processing temperature < 185 °C). We also
realize 3D circuits and demonstrate multifunctional capabilities including sensing, memory storage, as well as logic gates in any tier across the 3D stack. We believe that our demonstration will pave the path for more sophisticated, highly dense, and functionally divergent ICs with a larger number of tiers integrated monolithically in the third dimension.

A field-effect transistor (FET) consisting of a gate controlled switchable channel with source and drain electrodes is one of the primary component for most electronic gadgets that we use every day. FET design based on silicon (Si) have gone through incredible innovations over the past seven decades. Following Moore’s law, engineers packed chips with ever increasing number of FETs in the two-dimensional (2D) space until the beginning of the last decade [1]. The non-planar Si FinFET technology [2] represents the most advance process node, which is expected to sustain scaling for a few more years. FinFETs are expected to leave the stage soon for gate-all-around (GAA) FETs (or Ribbon FETs), which is considered to have the potential to extend Moore’s scaling until the end of this decade [3]. Going ahead, major semiconductor industries look forward to stack up devices in the third dimension to enable “More Moore” [4, 5]. The benefits of three-dimensional (3D) integration is evident from the success of the NAND flash technology, which has seen a drastic improvement in the memory storage capacity since the metamorphosis from planer 2D NAND to 24-layer 3D NAND in 2013, to 176-layer 3D NAND in 2021 [6]. The adoption of this scheme for silicon ICs has already begun and impressive technologies such as through-silicon-via (TSV), monolithic inter-tier-via (MIV), etc. already exist for 3D integration of Si ICs [7, 8].
While 3D integration has a huge potential for “More Moore”, it should also be noted that the development of this technology can potentially provide a hybrid burgeoning platform towards incorporating emerging materials that can offer newer functionalities that may not be readily available for the Si technology. This can also potentially open doors towards the integration of non-computational systems such as optical/gas/chemical sensors, memory devices, radio-frequency devices, etc., in different tiers of a 3D IC leading to better energy efficiency, lower cost, increased yield and reliability, and multifunctionality within a smaller volume. This approach is often referred to as “More than Moore” [9]. Along this route, two-dimensional (2D) semiconductors, among other contenders such as carbon nanotubes (CNT), nanowires, and III-V compound semiconductors, are considered promising for both “More Moore” and “More than Moore” technologies. In fact, it is even numerically analyzed and proposed that 2D materials have the potential to take full advantage of 3D integration [10].

From a materials perspective, the field of 2D semiconductors have seen some remarkable advancements in just one decade. For example, synthesis of 2D materials has evolved from mechanically exfoliated flakes to wafer-scale epitaxial and non-epitaxial growth [11-13]. At the same time, the performance of 2D FETs have started to meet the requirements set forth by the International Roadmap for Devices and Systems (IRDS) for advanced process nodes thanks to extensive effort on contact engineering, aggressive channel length scaling, and high-k dielectric integration [14-16]. This has prompted major semiconductor manufacturing corporations to introduce 2D FETs in their long-term technology roadmaps. In addition, realization of medium and large scale integrated circuits using 2D FETs further reinforce the potential of 2D materials for “More Moore”.
Beyond scaling, 2D materials have also shown promise with emerging computing paradigms like in-memory computing and in/near-sensor computing. Such demonstrations involve devices that co-locate “sensing”, “memory” and/or “compute”, which is key for achieving lower latency and better energy efficiency for the "More than Moore” technologies [17-24]. Besides, 2D materials enable unique straintronics, spintronics, twistrronics, and valleytronics devices as well as optical, chemical, and biological sensors, which can be harnessed for enriching the functional diversity for the "More than Moore” technologies [25-27]. Hence, even though Si electronics can be self-subsisting for coming decades, introducing 2D materials based electronics within different tiers in a 3D architecture can benefit many existing applications and create avenues for unanticipated discoveries.

Here, we achieve monolithic 3D integration of 2D FETs based on large area-grown monolayer MoS$_2$. Device statistics from more than 600 devices on two tiers is presented with high performance metrics. Even with effective oxide thickness (EOT) on tier 1 and tier 2 being 4 nm and 6 nm, respectively, the stack does not exhibit any leakage despite complex topography of associated with the 3D stacking. Low EOT values and scaled device dimensions enable low voltage operation (< 5 V) and yet at the same time the best performing devices exhibit ON-state current ($I_{ON}$) as high as ~300 $\mu$A/µm, current on/off ratio in excess of $10^7$, and subthreshold slope (SS) of ~100 mV.dec$^{-1}$. To the best of our knowledge, this is the first report showing statistics for more than ~30 devices in different tiers of a 3D IC based on scaled, high-performance 2D FETs. The thermal budget for fabricating the entire chip was ~185 $^0$C, strongly supporting the plausibility of adding a greater number of layers without compromising on the performance of lower tiers. Moreover, 3D logic circuits are realized and 2D devices are characterized for optoelectronic and
memory applications, opening doors for accommodating “sense” and “memory” layers in addition to “logic” layers. Fig. 1 summarizes the above mentioned contributions. We believe these demonstrations will pave the path for more sophisticated, highly dense, and functionally diverse 2D material-based chips with larger number of tiers integrated monolithically in the third dimension.

**Growth and characterization of monolayer MoS$_2$**

In this demonstration, monolayer MoS$_2$ was grown on an epi-ready 2” c-sapphire substrate using metal organic chemical vapor deposition (MOCVD) technique. The growth parameters are outlined in the *Methods* section and in our previous work [28]. The material quality was then assessed using material characterization techniques such as Raman spectroscopy,
photoluminescence (PL) spectroscopy, atomic force microscopy (AFM), and transmission electron microscopy (TEM). Fig. 2a,b, respectively, show the Raman spectra and corresponding spatial colormap of the two characteristic Raman active modes for monolayer MoS₂, in-plane $E_{2g}^1$ and out-of-plane $A_{1g}$, measured over an area of 40 µm × 40 µm. The average peak separation is found to be ~19 cm$^{-1}$. Similarly, Fig. 2c,d, respectively, show the PL spectra and corresponding spatial colormap of the PL peak position, measured from the same area in which Raman spectroscopy was performed. The average PL peak position is found to be ~1.82 eV. The average peak separation value from Raman spectroscopy, average PL peak position value, and their corresponding spatial colormaps confirms predominantly uniform monolayer synthesis. Fig. 2e shows the SEM of the grown MoS₂ film. Formation of multilayer islands on top of a largely monolayer film is observed.

Figure 2. Material Characterization. a) Raman spectra of the monolayer MoS₂ film used in this study taken at 676 points over a 50 µm × 50 µm area. The in-plane $E_{2g}^1$ and out-of-plane $A_{1g}$ active modes are labelled and the corresponding spatial colormaps of peak-to-peak distance is given in b). c) PL spectra of the monolayer MoS₂ measured at 676 points over a 50 µm × 50 µm area. d) Spatial colormap of A excitonic peak location for the PL spectra shown in (a). e) SEM of the grown MoS₂ film. Formation of multilayer islands on top of a largely monolayer film is observed. This is further evidenced by the atomic force microscopy (AFM), given in f). g) Atomic structure of the monolayer MoS₂ film used in this study as viewed down its c-axis. Image was taken at an accelerating voltage of 80 kV using an atomic resolution high-angle annular dark field (HAADF)-scanning transmission electron microscope (STEM). h) Selected area electron diffraction (SAED) of the MoS₂ film imaged in (g). The diffraction pattern shown indicates that the MoS₂ film possesses a uniform and single-crystalline structure.
This is further evidenced by the atomic force microscopy (AFM), given in Fig. 2d, in which 1.5 nm island formations are observed. Furthermore, scanning transmission electron microscopy (STEM) was used to investigate the structure of the transferred MoS\(_2\) film used in this study and verify its quality. A high-angle annular dark field (HAADF)-STEM image taken at an 80 kV accelerating voltage is presented in Fig. 2e, showing the atomic structure of the MoS\(_2\) film viewed down its c-axis. It can be clearly seen that the transferred film possesses a crystalline 2H-MoS\(_2\) structure with little-to-no point defects. This is supported by the selected area electron diffraction (SAED) results shown in Fig. 2f, which show a uniform single-crystalline structure.

Note that the ultimate channel thickness for most aggressively scaled FETs is expected to be in sub-1 nm range, which is difficult to achieve using bulk semiconductors. For example, mobility degradation associated with charge carrier scattering and quantum confinement effects make ultra-thin Si films of such thicknesses practically unusable [29]. In addition, manufacturing techniques for the realization of uniform and high-quality sub-1 nm Si films is non-existent highlighting the importance of monolayer 2D semiconductors for “More Moore” technology.

**Fabrication of 3D ICs based on 2D FETs**

After characterizing the MOCVD synthesized monolayer MoS\(_2\), fabrication of a two-tier monolithically integrated 3D chip was achieved on a 285 nm SiO\(_2\)/p\(^{++}\)-Si substrate. Note that this substrate functions only as a carrier substrate and in principle, any other substrates can be used. The fabrication flow is shown with schematics in *Extended Data 1*. First, the local gate electrodes for the bottom tier were defined via electron-beam (e-beam) lithography, followed by e-beam evaporation of 20 nm thick Ni. Following lift-off, ~10 nm Al\(_2\)O\(_3\), which corresponds to an effective
oxide thickness ($EOT$) of ~ 4 nm was deposited using atomic layer deposition (ALD) to serve as the gate dielectric for the bottom tier. To access the gate electrode, optical lithography was implemented and reactive ion etching (RIE) using BCl$_3$ gas was used to etch the gate oxide. Next, MoS$_2$ was transferred from the sapphire growth substrate onto the substrate with prefabricated islands of tier-1 gate-stack using a PMMA assisted wet transfer technique, followed by the process of defining the channels using e-beam lithography and RIE. Device fabrication for tier 1 was completed with the patterning of source and drain terminals using e-beam lithography followed by e-beam evaporation of 15 nm Ni/5 nm Au and lift-off. The channel lengths ($L_{Ch}$) of the fabricated FETs varied between 300 nm, 600 nm, 900 nm, and 1 µm, with a fixed channel width ($W_{Ch}$) of 1 µm. Prior to device fabrication for tier 2, a 100 nm Al$_2$O$_3$ spacer layer was deposited using ALD to separate the two tiers. Tier 2 device fabrication and dimensions are nearly identical to tier 1, with the only two variations being 1) the thickness of the gate oxide was 15 nm ($EOT$ ~ 6 nm) and, 2) the use of Ti/Pt back-gate instead of Ni. Tier 2 devices were placed in such manner that they align with tier 1 devices. Vias between the two tiers were fabricated by defining and etching rectangles near the contacts of tier 2, using optical lithography and RIE, respectively. Finally, metal evaporation is done to connect the tier 2 devices to the tier 1 devices as necessitated by the circuit design.

Note that the entire fabrication process described above is performed with a thermal budget of 185 $^0$C, and thus allows the addition of a greater number of tiers without causing any degradation to the bottom tiers. Note that the high-quality synthesis of 2D materials is still achieved with high temperatures (here 900 $^0$C), even though there exist a few demonstrations involving low temperature growth of 2D materials [30-32]. However, the van der Waals nature of 2D materials
allow wafer scale transfer from the growth substrate to any other desired substrate making 3D integration of a wide range of 2D materials relatively straightforward to achieve using our fabrication scheme described above. This is in contrast to Si, where monolithic 3D ICs restrict the process temperature for upper tiers to below ~ 450 °C, which can compromise the performance and yield of the Si FETs. Introducing high-mobility channel materials such as Ge, InGaAs, etc., in the upper tiers can compensate for degraded transistor characteristics but at the cost of increased fabrication process complexity. However, it is important to develop high-throughput wafer-scale transfer techniques for 3D integration of 2D materials. Interestingly, recent years have seen some remarkable advancements along this direction with the development of clean and automated transfer techniques [33, 34]. Such transfer techniques, when combined with wafer-scale growth and multi-tier device fabrication described here [35-38] can enable both monolithic and heterogeneous integration of 2D FETs with Si and other emerging technologies towards industrialization.

The 3D integrated stack was characterized following fabrication. Fig. 3a shows a low-magnification top-view scanning electron microscope (SEM) image consisting of arrays of MoS$_2$ based FETs stacked right on top of each other. The enlarged higher-magnification top-view SEM-BSE image given in Fig. 3b labels the accessible contact pads (source, drain and gate) and the via connection between two MoS$_2$ devices, one on tier 1 and the other on tier 2.Focused ion-beam (FIB) milling was employed to lift-out the region marked with the red-line in Fig. 3b, to observe the cross-section of the three-dimensionally integrated device stack. Fig. 3c shows the high-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of the cross-section showing the via connection between the tier 1 and tier 2 devices. 2D MoS$_2$ film can
Figure 3. 3D integration of 2D FETs. a) Low-magnification top-view scanning electron microscope (SEM) image consisting of arrays of MoS$_2$ based FETs stacked right on top of each other. The enlarged higher-magnification top-view SEM-BSE image is given in b), with the accessible contact pads (source, drain and gate) and the via connection between two MoS$_2$ devices, one on tier 1 and the other on tier 2, labelled. c) High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image of the cross-section showing the via connection between the tier 1 and tier 2 devices. 2D MoS$_2$ film can be seen in tier 1 and tier 2, as given in d) and e), respectively. Finally, a schematic detailing the materials and thicknesses of the back-gate, oxide, and contacts of devices in each tier is given in f).

be seen on both tiers, as shown in Fig. 3d,e. Extended Data 2 shows elemental analysis performed with energy dispersive spectroscopy (EDX) to confirm that the MoS$_2$ film is intact in both tiers. Finally, a schematic detailing the materials and thicknesses of the back-gate, oxide, and contacts of devices in each tier is given in Fig. 3f. As evident from Extended Data 1 and Fig. 3, the 2D-based chip is fabricated monolithically and integrated using inter-tier vias. In comparison to the currently commercialized through-silicon-via (TSV) based 3D integration technique, monolithic
3D integration possess several advantages including the use of vias with dimensions comparable to the device dimensions and the evasion of the wafer-thinning step [39, 40].

**High-performance MoS$_2$ FETs**

Electrical characterization on both tiers were performed before depositing necessary vias and connections for circuit demonstrations. **Extended Data 3** shows transfer characteristics, i.e., drain current ($I_{DS}$) plotted against the back-gate voltage ($V_{BG}$) for constant drain voltage, $V_{DS} = 1$ V, from 600 devices on each tier with all different channel lengths mentioned above. For a more organized representation, Fig. 4a,b show the transfer characteristics for 200 devices on each tier with $L_{Ch} = 300$ nm. All device parameters were extracted for a drain bias ($V_{DS}$) of 1 V, and tier 1 device characteristics were extracted before tier 2 fabrication. The threshold voltage ($V_{Th}$) of the devices was extracted using the iso-current method at 100 nA and the distribution for tier 1 and tier 2 is given. The $L_{Ch} = 300$ nm and $W_{Ch} = 1$ μm. The corresponding histograms of threshold voltage ($V_{Th}$) (extracted using the iso-current method at 100 nA) for tier 1 devices and tier 2 devices are given in c) and d) respectively. The distribution of the subthreshold slope (SS) for tier 1 and tier 2 devices for 2 orders, are given in e) and f) respectively. Finally, the distribution of the maximum ON-current ($I_{ON}$) obtained by the tier 1 and tier 2 devices at $V_{BG} = 5$ V and $V_{DS} = 1$ V, are given in g) and h), respectively.

![Figure 4. Electrical Characterization](image-url)
tier 2 devices is shown in Fig. 4c,d respectively. The average $V_{Th}$ for tier 1 devices was 0.95 V with a standard deviation of 0.75 V, and tier 2 devices demonstrated an average of 0.78 V with a standard deviation of 0.31 V. Fig. 4e,f show the distribution of the subthreshold slope ($SS$) for tier 1 and tier 2 devices, respectively, for 2 orders. Here, the average $SS$ for tier 1/tier 2 is 447/529 mV/dec with a standard deviation of 785/225 mV/dec respectively. The minimum $SS$ obtained for tier 1/tier 2 was 100/210 mV/dec, respectively. Fig. 4g,h shows the distribution of the maximum ON-current ($I_{ON}$) obtained by the tier 1 and tier 2 devices respectively. Here the average $I_{ON}$ for tier 1/tier 2 is 75.6/14.8 µA/µm with a standard deviation of 51.7/12.4 µA/µm. Larger device-to-device variation is observed in tier 1, which is attributed to the inconsistency of the wet transfer process, as tier 2 devices demonstrate significantly less variation. This is evidenced by the reduction in the standard deviation in $V_{Th}$, $I_{ON}$, and $SS$ histograms.

The above mentioned metrics and statistics stand out among other demonstrations involving 2D material-based 3D integration. In the past, there have been some remarkable demonstrations of 3D integration with 2D materials, as detailed in Extended Data 4. These achievements are indeed impressive and showcase the feasibility of incorporating 2D materials for stacking in the third dimension. However, there still exist some challenges that should be addressed for taking this technology closer to industrialization. They are, 1) some of the high performance devices in the above mentioned research efforts are based on mechanically exfoliated materials; 2) reports with devices based on large area-grown materials lack scaled device dimensions and statistical data from reasonably higher number of devices; 3) only a few of the above mentioned demonstrations showcases multifunctionality of 2D based devices such as sensing, storage, and logic circuits. Along these lines, here we have demonstrated a monolithically integrated 3D chip based on 2D
materials with low EOT values on each tier (4 nm and 6 nm), low voltage operation (3 V), statistics from more than 600 devices on each tier, and high performance metrics such as, \( I_{\text{ON}} \approx 300 \mu\text{A}/\mu\text{m} \) (at \( n_s = 2.3 \times 10^{13} \text{ cm}^{-2} \), \( L_{\text{Ch}} = 300 \text{ nm} \)) and \( SS = 100 \text{ mV.dec}^{-1} \). In addition to 3D integration, aggressive scaling is also demonstrated. *Extended Data 5* shows the transfer characteristics and a SEM image of a device with \( L_{\text{ch}} = 20 \text{ nm} \), \( W_{\text{ch}} = 400 \text{ nm} \), and contact length, \( L_{\text{C}} = 40 \text{ nm} \). We believe that this demonstration when combined with more optimization in terms of scaling with contacts, oxide, and channel length, in addition to improvements in material synthesis can usher in the path towards devices that can meet IRDS standards and thereby achieve “More Moore”. Finally, we show that 2D based FETs can be used to build logic gates as well as other non-computational systems such as photodetectors, allowing multifunctionality in a 2D-material based 3D chip, as described below.

**Multifunctional 2D FETs**

While the above described electrical characterization and statistics from a relatively large dataset strongly supports the rationale for 2D materials to be considered for 3D integration, it is also important to highlight some functionalities that can be implemented in different tiers with 2D FETs. As mentioned above, some of the functionalities that can be incorporated in a monolithically integrated 3D integrated stack can include 1) logic 2) memory and 3) sensing. Fig. 5 showcases all these three attributes executed with 2D MoS\(_2\) based FETs.

Fig. 5a,b,c highlight inverter, NAND, and NOR functionalities, respectively. Note that all circuits were operated at a supply voltage of \( V_{\text{DD}} = 1 \text{ V} \). Fig. 5a shows the circuit diagram and output characteristics, i.e., the output voltage (\( V_{\text{OUT}} \)) plotted against the input voltage (\( V_{\text{IN}} \)), for a 3D
integrated NMOS inverter. Here, the tier 1 device behaves as the depletion load transistor with the gate and source of the device shorted, while the tier 2 device works as the driving transistor. The gain of the inverter was found to be $2 \text{ V/V}$. Fig. 5b, shows the NAND implementation, in which the T1 MoS$_2$ behaves as the depletion load, and the T2 device operates as the driving transistor. In-plane logic circuits including NAND and NOR are shown in b) and c), respectively. The memory capabilities exhibited by the MoS$_2$ FETs are shown with d) transfer characteristics for ten devices that are programmed in a low conduction state (LCS), and a high conduction state (HCS), e) retention of HCS and LCS for 600 s, and f) an endurance plot (50 cycles). Finally, the photosensing capabilities of MoS$_2$ FETs are shown with g) transfer characteristics from 50 devices measured under dark and illuminated (white light, $P_{IN} = 15 \text{ Wm}^{-2}$) conditions, and the extracted h) responsivity ($R$) and i) specific detectivity ($D^*$). Thus, with the demonstration of logic, memory, and sensing, the multifunctionality of the MoS$_2$ FETs are showcased.

**Figure 5. Logic, storage, and sensing.** a) Output characteristics, i.e., the output voltage ($V_{OUT}$) plotted against the input voltage ($V_{IN}$), for a 3D integrated NMOS inverter. Inset shows the circuit diagram of the inverter, in which the T1 MoS$_2$ behaves as the depletion load, and the T2 device operates as the driving transistor. In-plane logic circuits including NAND and NOR are shown in b) and c), respectively. The memory capabilities exhibited by the MoS$_2$ FETs are shown with d) transfer characteristics for ten devices that are programmed in a low conduction state (LCS), and a high conduction state (HCS), e) retention of HCS and LCS for 600 s, and f) an endurance plot (50 cycles). Finally, the photosensing capabilities of MoS$_2$ FETs are shown with g) transfer characteristics from 50 devices measured under dark and illuminated (white light, $P_{IN} = 15 \text{ Wm}^{-2}$) conditions, and the extracted h) responsivity ($R$) and i) specific detectivity ($D^*$). Thus, with the demonstration of logic, memory, and sensing, the multifunctionality of the MoS$_2$ FETs are showcased.
successful inverse logic multiplication operation is observed. Lastly, Fig. 5c shows the NOR operation in which inverse logic addition operation is demonstrated.

The second row in Fig. 4 highlights the memory capabilities exhibited by the MoS$_2$ FETs. Fig. 5d shows the transfer characteristics for ten device that are programmed in a low conduction state (LCS), and a high conduction state (HCS). Here, a 40 nm Al$_2$O$_3$/ 3nm HfO$_2$/ 7 nm Al$_2$O$_3$ local back-gate oxide stack is implemented, in which the bottom layer of Al$_2$O$_3$ serves as the blocking layer, the HfO$_2$ functions as the charge-trapping layer, and the top Al$_2$O$_3$ is the tunneling layer. With the application of a large negative programming voltage \( V_{BG} = V_{\text{Program}} = -10 \text{ V} \) applied for a period of \( t_{\text{Program}} = 100 \text{ ms} \), holes/electrons are trapped/detrapped in the HfO$_2$.

These charges then screen the electric field across the MoS$_2$, altering the conductance of the channel, which provides access to multiple discrete conductance states. Analogously, for large positive erase voltage (for LCS, \( V_{BG} = V_{\text{Erase}} = +12 \text{ V} \) applied for a period of \( t_{\text{Program}} = 100 \text{ ms} \), electrons/holes are trapped/detrapped in the HfO$_2$, decreasing the conductance of the channel. Similar gate stack composition and operation have been demonstrated, enabling the realization of non-volatile memory with 2D materials [41, 42]. The cross-sectional TEM of nickel contacted MoS$_2$ device with the discussed gate stack is shown Extended Data 6. The applicability of 2D MoS$_2$ FETs for in-memory computing applications is a testament to the highly conformal deposition of the programmable gate stack and successful electrical demonstration. In addition, the programmed/erased state is retentive as shown in Fig. 5e, where \( I_{DS} \) at each state is measured by applying a read voltage \( V_R = V_{BG} = 0 \text{ V} \) and \( V_{DS} = 1 \text{ V} \) to the device for 600 s. Minimal degradation for each conductance state is observed. An endurance of the device is also provided.
with 50 consecutive program and erase cycles, in Fig. 5f. Minimal degradation in the memory ratio during the cycling process is observed, highlighting the good endurance of the MoS$_2$ FETs.

Finally, the third row in Fig. 4 highlights the sensing capabilities exhibited by the MoS$_2$ FETs. The photoresponse of the MoS$_2$ FETs is shown in Fig. 5g in which the transfer characteristics from 50 devices are measured under dark and illuminated ($P_{IN} = 15$ Wm$^{-2}$, $\lambda = \sim500$ nm) conditions. Here a negative shift in the threshold voltage resulting from the photogating effect is observed, in which defects and/or absorbates trap photogenerated carriers and screen the electric field across the MoS$_2$ transistor [43, 44]. To illustrate the efficacy of the photo-response in the MoS$_2$ FETs, responsivity and specific detectivity is extracted, as shown in Fig. 5h,i, respectively. The average responsivity and detectivity was obtained to be 27.9 AW$^{-1}$ and 6.2 $\times$10$^7$ Jones, respectively. Thus, with the demonstration of logic, sensing, and memory, the multifunctionality of the MoS$_2$ FETs are showcased. The diverse functionality of 2D materials makes them strong contenders for “More Moore” and “More than Moore” technologies.

**Conclusion**

In conclusion, we have demonstrated monolithic 3D integration with MoS$_2$ across two tiers, which can be extended to any desired number of layers. MoS$_2$ based FETs have been sequentially fabricated, with vias connecting the two tiers. Along with logic capabilities, the devices demonstrate sensing and memory capabilities, successfully demonstrating the multifunctionality of our devices in the pursuit of realizing a “More Moore” and “More than Moore” 3D chip. In addition, we demonstrate 600 devices in each tier and provide statistical data on the device
performance. Our results are the first step towards the realization of densely packed 3D IC based on 2D materials.
Extended Data Figure 1. Fabrication flow schematic of the 2D based 3D integrated chip.
Extended Data Figure 2. The elemental analysis performed with energy dispersive spectroscopy (EDX) for a) tier 1 and b) tier 2 show that MoS$_2$ is intact on both tiers. The stack shown in a) for tier 1 shows multilayer MoS$_2$. We believe that the cross-section was done through a multi-layer island of MoS$_2$ since the material is predominantly monolayer as shown in the SEM (Fig. 2e) and AFM (Fig. 2f) images.
Extended Data 3

Extended Data Figure 3. Transfer characteristics of 600 devices each, from a) tier 1 and b) tier 2, respectively.
**Extended Data 4.**

To the best of our knowledge, the first attempt in utilizing 2D semiconductors as a sensing layer in a 3D-integrated chip was done by Yang et. al. in 2016, where they fabricated a $5 \times 5$ phototransistor array based on CVD grown MoS$_2$ on top of poly-Si nanowire based FETs [45]. This demonstration clearly shows the benefits associated with sequentially fabricating tiers of devices including flexibility towards choosing different materials/devices functionalities in each tier, in addition to reducing the active device/circuit area footprint. In the same year, Sachid et. al. demonstrated monolithic 3D CMOS including inverter, NOR, NAND, amplifiers, and mixers using exfoliated MoS$_2$ and WSe$_2$ [46]. While exfoliation is generally considered an impractical technique from the perspective of industrializing the technology, the demonstration of low-power circuits with relatively high-performance n-type and ambipolar FETs is certainly impressive. In 2018, Wang et. al., fabricated 3D monolithic stacked 1T1R cells using CVD-grown monolayer MoS$_2$ and h-BN RRAM [47]. Even though these cells were not stacked right on top of each other due to topography considerations, they successfully demonstrated that their fabrication steps can be repeated to achieve any number of desired levels owing to their low thermal budget < 150 °C. While the above demonstrations showed integration of sensing and logic, 3D CMOS circuits, and integration of logic and memory, 2D materials, in principle, can also be stacked to explore their capability as an alternative nanosheet channel material in currently explored GAAFET and MBCFET nano-sheet device structures. This was first explored by R. Zhou and J. Appenzeller where they showed a 2-channel FET based on exfoliated MoS$_2$ flakes with source-to-drain current, $I_{DS} = 55 \mu A/\mu m$ at $V_{OV}$ (over-drive voltage) = $V_{DS}$ (drain-to-source voltage) = 1 V, which was a two-fold increase in comparison to their single channel device [48]. Huang et. al. also fabricated a 2-channel FET with gate-all-around structure using exfoliated MoS$_2$ and h-BN (gate-oxide) [49]. Recently, Xia et. al. demonstrated 2-channel FETs using CVD-grown n-type MoS$_2$ and stacked
complementary FETs using CVD-grown p-type MoTe$_2$ and n-type MoS$_2$ [50]. They showed NAND and NOR circuits based on n-type MoS$_2$ in addition to an inverter based on p-type MoTe$_2$ and n-type MoS$_2$. While this demonstration is certainly a step ahead in stacking 2D materials, owing to the use of large area-grown n-type and p-type materials, their device dimensions were relatively large ($L_{CH} > 10 \, \mu m$) in all cases. In another demonstration, Liu et. al. fabricated and characterized 22 CVD-grown WSe$_2$-based p-FETs on top of CVD-grown MoS$_2$ based n-FETs with 5 $\mu m$ long channels [51].
Extended Data 5

Extended Data Figure 4. a) Transfer characteristics and b) SEM image of a device with $L_{\text{Ch}} = 20$ nm, $W = 400$ nm, and contact length, $L_{C} = 40$ nm.
Extended Data Figure 5. Cross-sectional TEM of a nickel contacted MoS$_2$ device with a gate stack consisting of 40 nm Al$_2$O$_3$/3 nm HfO$_2$/7 nm Al$_2$O$_3$ to implement a charge-trapping memory for MoS$_2$ based FETs.
Methods

Large-area monolayer MoS$_2$ film growth: To synthesize the large area MoS$_2$, MOCVD was carried out on epi-ready 2” c-sapphire substrate using. A cold-wall horizontal reactor with inductively-heated graphite susceptor was implemented, in which Molybdenum hexacarbonyl (Mo(CO)$_6$) and hydrogen sulfide (H$_2$S) were flowed into the chamber. To obtain uniform growth the stainless-steel bubbler containing Mo(CO)$_6$ was kept at 10°C at 650 Torr and was delivered to the growth chamber at $1.1 \times 10^{-3}$ sccm, while H$_2$S is flowed at 400 sccm. The growth chamber was maintained at 900°C under 50 Torr H$_2$ ambient environment. The growth of monolayer MoS$_2$ was achieved in 18 min. More details can be found in our earlier work [52-54].

MoS$_2$ film transfer to local back-gate islands: To fabricate the 2D FETs, MOCVD grown monolayer films were transferred from the sapphire growth substrate to the Ti/Pt island substrate using PMMA (polymethyl-methacrylate) assisted wet transfer process. Initially, the grown film was spin coated with PMMA and then baked at 200 °C for 120 s. All sides of the spin-coated film were scratched using a razor blade and immersed inside a DI water bath at room temperature. Water molecules intercalate between the substrate/film due to capillary action, separating the film from the substrate. The target substrate is used to fish out the film from the water bath and then baked at 50 °C and 70 °C for 10 min to improve the adhesion between the film and the substrate. The PMMA layer is subsequently removed by placing the sample in an acetone bath for 10 min, followed by an IPA bath for 10 min to clean the sample.

Fabrication of local back-gate islands for memory and sensing: To define the back-gate island regions, a commercially purchased substrate (thermally-grown 285 nm SiO2 on p++-Si) was spin
coated at 4000 RPM for 45 s with a bilayer photoresist consisting of Lift-Off-Resist (LOR 5A) and Series Photoresist (SPR 3012); following application, these resists were baked at 185 °C for 120s and 95 °C for 60 s, respectively. The bilayer photoresist was then patterned using a Heidelberg Maskless Aligner (MLA 150) to define the islands and developed by immersing the substrate in MF CD26 microposit for 75 s, followed by a 60 s de-ionized (DI) water rinse. The back-gate electrodes of 20/50 nm Ti/Pt were then deposited using electron-beam (e-beam) evaporation in a Temescal FC-2000 Bell Jar Deposition System. Liftoff of the remaining photoresist and excess metal was achieved using acetone and Photo Resist Stripper (PRS 3000); the substrate was then cleaned using 2-propanol (IPA) and DI water. An atomic layer deposition (ALD) process was then implemented to grow the back-gate dielectric stack consisting of 40 nm Al₂O₃ (ε₀x ≈ 10), 3 nm HfO₂ (ε₀x ≈ 25), and 7 nm Al₂O₃ across the entire substrate, including the island regions. Access to the individual Pt back-gate electrodes was achieved via a reactive ion etch (RIE) process conducted in a Plasma-Therm Versalock 700. First, etch patterns were defined using the same bilayer photoresist (LOR 5A and SPR 3012) used previously. The bilayer photoresist was again exposed using an MLA 150 and developed using MF CD26 microposit with a DI water rinse. The dielectric stack was then dry etched using a BCl₃ RIE chemistry at 5 °C for 80 seconds; this process was split into four 20 s etch steps separated by 60 s stabilization steps to minimize heating in the substrate. Finally, the photoresist was removed using the same process described earlier for liftoff.

**Scaled Device Fabrication:** Scaled devices of L_{Ch} = 20 nm and L_{c} = 40 nm were fabricated after the isolation etch of MoS₂. The sample is initially dipped in Surpass 4K for 60 s, rinsed in DI water, and then baked at 100 °C for 60 s to improve the wettability of ZEP 1:1 photoresist. ZEP 1:1 was
spun at 5000 RPM for 45 s and baked at 180 °C for 3 min. E-beam lithography is carried out at a beam energy of 100 keV, and is developed in n-amyl acetate chilled at -10 °C for 3 min and IPA at room-temperature for 60 s. Next, e-beam evaporation is done to deposit the channel contacts, followed by lift-off in acetone and IPA. Next, contacts are to be deposited that connect the channel contacts to pads that are accessible by the probestation. Initially the sample is spin coated with MMA EL6, followed by A3 PMMA. E-beam lithography is again used to pattern the pads, followed by development using MIBK:IPA for 60 s and IPA for 45 s. Lastly, e-beam evaporation was done to deposit 40 nm Ni/30 nm Au, followed by lift off.

*Raman and photoluminescence (PL) spectroscopy:* Raman and PL spectroscopy of the pre- and post-irradiation MoS$_2$ film were performed on a Horiba LabRAM HR Evolution confocal Raman microscope with a 532 nm laser. The power was 34 mW filtered at 5% to 1.7 mW. The objective magnification was 100× with a numerical aperture of 0.9, and the grating had a spacing of 1800 gr/mm for Raman and 300 gr/mm for PL.

*Scanning electron microscopy (SEM):* Scanning electron microscopy (SEM) of the 2D MoS2 transistors used in this study was conducted using a Zeiss Gemini 500 field emission scanning electron microscopy (FESEM) system at an accelerating voltage of 5 kV.

*Atomic Force Microscopy (AFM):* AFM was used to study the surface morphology, domain size, coverage, and thickness of the deposited layers. Scanasyst air probe AFM tips with a nominal tip radius of ~2 nm and spring constant of 0.4 N/m were employed for the measurements, and images
were collected using peak-force tapping mode with a peak force of 500 pN and scan speed of 2 Hz.

**Electrical Characterization:** Electrical characterization of the fabricated devices was performed using a Lake Shore CRX-VF probe station under atmospheric conditions with a Keysight B1500A parameter analyzer. A continuous wave white light source was used for all experiments involving light illumination unless otherwise stated.

**Data Availability:** The datasets generated during and/or analyzed during the current study are available from the corresponding author on reasonable request.

**Code Availability:** The codes used for plotting the data are available from the corresponding authors on reasonable request.
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Author Contributions
S.D., R.P. and D.J. conceived the idea and designed the experiments. D.J., and R.P. fabricated the 3D chip. S.D., D.J., and R.P. performed the experiments, analyzed the data, discussed the results, and agreed on their implications. N.T. grew and characterized MOCVD MoS$_2$ under the supervision of J.M.R. Y.Y. performed the FIB for the 3D chip. Y.Y. and Y.H. performed TEM for the 3D chip. All authors contributed to the preparation of the manuscript.

Competing Interest

The authors declare no competing interests.
References


