A Noise-free Bias, 0.2TΩ Input Impedance CMOS Ultra-Low Noise Front-end Neural Amplifier in 65nm Process

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A Noise-free Bias, 0.2TΩ Input Impedance CMOS Ultra-
Low Noise Front-end Neural Amplifier in 65nm Process

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Abstract

This work proposes a CMOS two-stage ultra-low noise front-end neural amplifier (FENA) that is realized in the UMC 65nm Process. The proposed FENA consists of an operational transconductance amplifier along with incorporated low pass filter (LPF) technique. Due to this technique, FENA circuit provided best performances such as ultra-low input referred noise, ultra-high input impedance and high gain. An algorithm and mathematical noise model are employed to optimize the dimensions of LPF technique and transistor fingers which yield noise-free biasing current and ultra-low input referred noise of 18fV/√Hz at 10 KHz. The ultra-low input referred noise of FENA is achieved by reducing the gate distributed resistance method which is ignored in conventional FEA design. The FENA achieves an ultra-high input impedance of 0.2 TΩ, while a splendid post-layout gain of 80 dB has succeeded. FENA has layout area of 0.0023 mm² which consumes lower power consumption of 1 mW under supply voltage of 1.2V. The FENA is found to be less prone to PVT variations as 1mHz of high-pass corner frequency is achieved for robust design. The best performance parameters of FENA could be beneficial for the purpose of deep exploration neural activities in wireless neural monitoring systems.

Keywords: Front-end neural amplifier, Low-pass filter (LPF), Complementary metal oxide semiconductor (CMOS), Bio-medical, Neural system

1. INTRODUCTION
Nowadays thrive, research in biomedical applications insists on new designs and techniques with improved performance for neural monitoring wireless systems. An implantable neural interface system records the neural activity by multichannel electrodes and monitors a large number of neurons of the human being [1], [2]. However, this neural interface system should be in a small die area, with less noise with ultra-low power consumption, which ensures no damage to the tissue. In several biomedical applications such as Electromyogram (EMG), Electrocardiogram (ECG), and Electroencephalography (EEG) biopotentials are very low in both amplitudes as well as frequency.

![Fig. 1. Implicit view of the Human brain.](image)

Fig. 1 shows an implicit view of the human brain where the observable electrical activity of neurons is very small in amplitude and operates in the sub Hz frequencies. It can be further classified as Action potential value (A.P.) and Local field potential value (LFP). Typically, A.P.'s have a maximum peak-to-peak amplitude of 500 µV down to 5µV in the frequency range of 300Hz to 7.0 kHz, whereas LFP's amplitude is around 5 mV down to 1 mV over the frequency 25 MHz to 100 Hz [3],[4],[5]. To perceive such signals, an efficient and robust high-performance front-end amplifier (FEA) with low noise, high input impedance, and low power consumption with less form factor is required [6].

In [7], a bio amplifier is employed, which uses off-chip capacitors in the order of nF, in which the high pass corner frequency (HPF) (i.e. the minimum frequency at which FEA is able to amplify sub-Hz biomedical potentials) is limited to 30 Hz only. Typically, implantable devices dissipate power in the form of heat flux, which is around to be 80 mW/cm² and which damages the sensitive muscle tissues; hence less power dissipation became an essential metric in biomedical applications [8]. An active electrode integrated
circuit consumes a large power dissipation of 360 µW with an input impedance of 100 MΩ, while it is not suitable for implantable [9]. A complementary input amplifier (C.A.) dissipates the considerable power dissipation of 12 µW and operates in the band of 0.05 Hz to 10.5 kHz [10]. FEA using an instrumentation amplifier provides different variable gains of (14, 20, 26, and 40 dB), according to requirement; however, the large Form Factor (F.F.) of 1.2 mm² is the bottleneck to implantable devices [11]. In [12], the Current feedback instrumentation amplifier uses switched capacitor integrator to suppress flicker noise, resulting in a high noise density of 64 nV/√Hz. In bio-potential amplifier with a current mirror operational transconductance amplifier (OTA) achieved a fine form factor of 0.22 mm², which yielded less gain of 39.8 dB with a bandwidth of 30 Hz, bearing 21 nV/√Hz of input-referred noise [13],[14]. Moreover, the auto zeroing (AZ) technique is commonly used in FEA to reduce the leakage current and flicker noise to zero, which employs a two-state sample and hold technique [15]. However, the equivalent input referred noise was achieved to be 79 µV rms. While in [16], input referred noise was reduced to 4.98 µV rms in low power LNA, with high pass corner frequency limited to 10 mHz, with less input impedance of 16 MΩ at 1 kHz. Capacitive feedback techniques are used to increase input impedance up to 1.6 GΩ only, with a power consumption of 2.8 µW [17]. A fixed value of a capacitor is used in the current compensation feedback (CCF) to reduce the leakage current; thus input current of FEA reduces, which boosts the input impedance to 60 GΩ, with a less gain of 14 dB in the expense of 7.6 µW [18]. Bootstrapped FEA improves gain to 75 dB, with improvement in input impedance to 42 GΩ by reducing leakage current, but high pass corner frequency restricted to 300 MHz. Its inherent input referred noise is achieved 18.2 nV/√Hz at 1 MHz where residing in the chip area of 0.042 mm² at the expense of 3.1 µW [19]. In addition, [20] suggested the measurement results of MOSFETs which showed an induced gate noise that deviates from most of the models. Hence it is necessary to reduce distributed gate resistance which helps to attain an ultra-low noise.

Therefore in this work, the proposed FENA with Low Pass Filter (LPF) biasing technique and optimized TULN-OTA helped to achieve an ultra-low noise design here that led to input referred noise of 18 fV/√Hz, with a splendid gain of 80 dB. To give more prominence to biomedical signals (as frequency lies in the order mHz), it sustains with a high pass corner of 1 mHz. In order to prevent tissues from heat flux issues, the proposed FENA dissipates a less power of 1 µW. The work is organized as follows: Section 2 includes conventional FEA design and their trade-offs, while section 3 includes a proposed FENA design using gm over
id algorithm. And finally, section 4 describes the results and discussion, followed by a conclusion in section 5.

2. Conventional FEA Design
In this section, the design trade-off of conventional Front End Amplifier (FEA) will be discussed.

2.1 Conventional FEA design Trade-offs
A Conventional FEA consists of two operational transconductance amplifiers (named OTA1 and OTA2) with neutralization current feedback (NCF) and voltage bootstrapping (VB) techniques which are shown in Fig. 2(a). To be elaborative, each OTA has a two-stage low noise amplifier (TLNA) as shown in Fig. 2(b). The cumulative gain of two OTA’s (OTA1 and OTA2) is 75 dB which in turn increased the input impedance to 42 GΩ (observed at 1kHz). The NCF and VB techniques are implemented with the elements of three capacitors named as  \( C_{Neu,f} \),  \( C_N \) and  \( C_B \) and three Pseudo resistors named \( PR_1 \) to \( PR_3 \). To achieve large input resistance with an acceptable layout area, a Pseudo resistor was designed by the back-to-back connection of the two Metal Oxide Semiconductor Field Effects (MOSFET’s) [19].
Fig. 2. Conventional FEA with its (a) Block schematic representation and (b) Full schematic view of TLNA.

In general, an FEA leakage current ($I_{\text{leak}}$) depends upon gate oxide capacitance and area ($W \times L$) of the differential input stage in the TLNA. The leakage current $I_{\text{leak}}$ of FEA is given by (1) [19].

$$I_{\text{leak}} = (W \times L) \times \left( \frac{V_{\text{oxide}}}{t_{\text{oxide}}} \right)^2 \times e^{Y} \left[ 1 - \left( \frac{V_{\text{oxide}}}{t_{\text{oxide}}} \right)^{1.5} \right]$$  \hspace{1cm} (1)

Where $W$ and $L$ are the width and length of the differential amplifier input stage MOSFET's, $X = \frac{q^3}{16\pi^2h\phi_{ox}^{1.5}}$, $Y = -4\pi\sqrt{2m_{ox}\phi_{ox}^{1.5}}$, $h$ is Planck's constant, $q$ is the electron charge, $t_{\text{oxide}}$ is the oxide thickness, and $V_{\text{oxide}}$ is the gate oxide breakdown voltage, $m_{ox}$ is the effective mass of tunneling particle, $\phi_{ox}$ is the height of tunneling barrier. Here, the neutralization of leakage current ($I_{\text{leak}}$) minimizes the input-referred noise of the FEA. This compensation happens due to the applied neutralization capacitor $C_{\text{Neu,f}}$ in the current feedback path by $I_{\text{Neu,f}}$. The input current of FEA can be expressed as in equation (2) [19].

$$I_{\text{in}} = I_{P_{R}} + I_{\text{leak}} - I_{\text{Neu,f}}$$  \hspace{1cm} (2)

From equation (2), it is realized that input current ($I_{\text{in}}$) was optimized, such that input referred noise was reduced to 18.2 nV/√Hz only at 1 KHz. In addition, it is also observed with our research potential that each PMOS/NMOS with large form factor (F.F.) was employed in the conventional FEA (both OTA’s). Due to this, the $R_G$ of corresponding MOSFET’s increases which results in high thermal noise by the amount of $4kTR_G$, and the observation picture is shown in Fig. 3 [21]. The equivalent distributed gate resistance ($R_G$) can be expressed as in equation (3).
Precisely, the current biasing circuit of a differential amplifier in TLNA schematic, current \((I_{pm4})\) replicating MOSFET \(PM_4\) \((\text{aspect ratio as } 1 \times \frac{20\mu m}{0.5\mu m})\) made twice the aspect ratio of the reference MOSFET \(PM_{REF}\) \((\text{aspect ratio as } 1 \times \frac{10\mu m}{0.5\mu m})\) to meet the required current. This reference bias current \((I_{bias})\) multiplication by two times increases the flicker noise by the same amount in \(I_{pm4}\). So, this work derived the current noise spectrum of the \(PM_4\), \(I_{n,PM4}\), is enumerated by applying the superposition theorem to the individual noise spectrums of \(\bar{v}_{n,PM_{ref}}^2\) and \(\bar{v}_{n,PM4}^2\) as given in equations (4) and (5).

\[
I_{n,PM4}^2 = \left[ \frac{\bar{v}_{n,PM_{ref}}^2}{(1|g_{PM_{ref}}^2)} \right] g_{PM4}^2 + \left[ \bar{v}_{n,PM4}^2 \right] g_{PM4}^2
\]

(4)

\[
I_{n,PM4}^2 = (\bar{v}_{n,PM_{ref}}^2 g_{PM_{ref}}^2 + \bar{v}_{n,PM4}^2) g_{PM4}^2
\]

(5)

As \((W/L)_{PM4} = 2(W/L)_{PM_{ref}}\), then \(\bar{v}_{n,PM_{ref}}^2 = 2\bar{v}_{n,PM4}^2\), then equation (5) can be modified as in (6) and (7) resemble high current noise spectrum \(I_{n,PM4}^2\).

\[
I_{n,PM4}^2 = (2\bar{v}_{n,PM_{ref}}^2 g_{PM_{ref}}^2 + \bar{v}_{n,PM4}^2) g_{PM4}^2
\]

(6)

\[
I_{n,PM4}^2 = (2g_{PM_{ref}}^2 + 1)\bar{v}_{n,PM4}^2
\]

(7)

Where \(\bar{v}_{n,PM_{ref}}^2, \bar{v}_{n,PM4}^2\) represent the output noise voltage spectrum of \(PM_{REF}\) and \(PM_4\), respectively. \(I_{n,PM4}^2\) is the input current noise spectrum of \(PM_4\). \(g_{PM_{ref}}, g_{PM4}\) represents transconductance of \(PM_{REF}\) and \(PM_4\) respectively. The above derivation of the noise current spectrum is formulated by considering current replicating MOSFET’s \((PM_{REF}, PM_4)\) and its noise equivalent sources, which are given in Fig. 4(a) and (b), respectively.
Fig. 4. Partial view of conventional FEA-bias current distribution network with (a) current replicating MOSFET’s $PM_{REF}$ and $PM_4$ and (b) Noise equivalent sources of $PM_{REF}$ and $PM_4$.

It is clear from Fig. 4, this increased noise component in the $I_{bias}$ propagates to the amplifier, which corrupts the signal and degrades the performance of FEA. Moreover, it is also perceived that the conventional FEA, VB technique not only reduces signal current but also improved high pass corner frequency and the input impedance of FEA (42 GΩ at 1KHz). Sorting of node voltages $V_{out}$, $V_{in}$ and $V_B$ using the elements OTA2, $C_B$, $PR_2$ and $PR_1$ in the VB. When $V_B$ approaches $V_{in}$, the current through large $PR_1$ minimized subjected to the parasitic capacitance ($C_p$) across $PR_1$. The high pass corner frequency is a function of $C_B$ and $PR_2$. Therefore, the minimum high pass corner frequency of conventional FEA obtained is 300 mHz. Hence to attain the infinitesimal noise, input noise current spectrum, $I_{n,PM1}^2$, overall distribution resistance ($R_G$), and parasitic capacitance ($C_p$) of FEA have to be minimized. Therefore, a noise elimination technique is proposed here, which incurs the conventional design parameter trade-offs, which will be discussed in the next section.
3. Proposed FENA Design and Optimization

Fig. 5(b) is shown the proposed schematic of FENA with incorporated techniques. The proposed FENA consists of only a two-stage ultra-low noise operational transconductance amplifier (TULN-OTA) operated with the proposed low pass filter current biasing circuit. A TULN-OTA has a differential mode topology named $PM_1$, $PM_2$, $NM_1$ and $NM_2$ followed by a common source amplifier named $PM_5$ and $NM_5$. Here the current biasing circuit consists of various dimensions named $PM_{REF1}, PM_{REF2}, R_{LPF}, C_{LPF}, NM_3, NM_4, PM_3$ and $PM_4$. Here the resistance $R_{LPF}$ (constituting $PM_{LPF1}, PM_{LPF2}$) and $C_{LPF}$ form low pass filter design. The equivalent resistance $R_{eq}$ is the summation of resistance offered by $PM_{REF} \left( \frac{1}{g_{PMref}} \right)$, and composite MOSFET $PM_{LPF}$ is considered as $R_{LPF}$. A comprehensive noise performance analysis is done to achieve an ultra-noise metric of 18 fV/√Hz at 10 kHz with the proposed noise-free biasing current and optimum design of TULN-OTA. TULN-OTA is designed in such a way that it yields the best high pass corner frequency (1 mHz) and noise by considering the operating input stage MOSFET’s named as $(PM_1, PM_2, NM_1, and NM_2)$ in deep subthreshold region and MOSFET’s optimized using an appropriate number of fingers too using gm over id algorithm in section 3.2.

3.1 Noise Optimization

The purity of biasing current plays a vital role in the noise metric. The bias current multiplication requirement increases the flicker noise, and this can be avoided by the
proposed low-pass filter technique designed by \( R_{\text{LPF}} \) and \( C_{\text{LPF}} \). From equation (7), it can be seen that the conventional bootstrapped FEA provides noise in the biasing current (\( I_{n,\text{PM4}}^2 \)). For the proposed FENA, the optimum current noise spectrum (\( I_{n,\text{PM4}}^2 \)) of MOSFET \( \text{PM}_4 \) is expressed as (8) to (11).

\[
I_{n,\text{PM4}}^2 = \left[ \frac{1}{1 + R_{\text{eq}}C_{\text{eq}}S} \right]^2 \left( v_{n,\text{PMref}}^2 + v_{n,R(\text{lpf})}^2 + v_{n,\text{PM4}}^2 \right) g_{\text{PM4}}^2
\]

(8)

\[
I_{n,\text{PM4}}^2 = \left[ \frac{1}{1 + \left( \frac{1}{g_{\text{PMref}}} + R_{\text{lpf}} \right) C_{\text{lpf}}S} \right]^2 \left( v_{n,\text{PMref}}^2 + v_{n,R(\text{lpf})}^2 + v_{n,\text{PM4}}^2 \right) g_{\text{PM4}}^2
\]

(9)

\[
I_{n,\text{PM4}}^2 = \left[ \frac{g_{\text{PMref}}^2}{g_{\text{PMref}}^2 + (1 + g_{\text{PMref}}R_{\text{lpf}}) C_{\text{lpf}}^2 S} \right]^2 \left( v_{n,\text{PMref}}^2 + v_{n,R(\text{lpf})}^2 + v_{n,\text{PM4}}^2 \right) g_{\text{PM4}}^2
\]

(10)

\[
I_{n,\text{PM4}}^2 = \left[ \frac{g_{\text{PMref}}^2}{g_{\text{PMref}}^2 + (1 + g_{\text{PMref}}R_{\text{lpf}}) C_{\text{lpf}}^2 S} \right]^2 \left( v_{n,\text{PMref}}^2 + v_{n,R(\text{lpf})}^2 + v_{n,\text{PM4}}^2 \right) g_{\text{PM4}}^2
\]

(11)

Where, \( v_{n,\text{PMref}}^2 \), voltage noise spectrum of reference MOSFET. \( g_{\text{PMref}}, g_{\text{PM4}} \) represents transconductance of \( \text{PM}_{\text{REF}} \) and \( \text{PM}_4 \) respectively. \( R_{\text{lpf}} \) and \( C_{\text{lpf}} \) are resistance and capacitance offered by low pass filter, and \( w \) is the frequency in radians per second. Here, voltage noise spectrums of both \( \text{PM}_{\text{REF}} \) and \( \text{PM}_{\text{lpf}1,2} \) \( v_{n,R(\text{lpf})}^2 \) reduces by the factor of \( g_{\text{PMref}}^2 + (1 + g_{\text{PMref}}R_{\text{lpf}})^2 C_{\text{lpf}}^2 w^2 \), thus resulting reduction in a noise current factor, \( I_{n,\text{PM4}}^2 \). Here for the frequency range of 1mHz to 10kHz, prior to the low pass filter noise bias current, \( I_{n,\text{bias}}^2 \) is in the order of \( 10^{-4} \) and after low pass filter noise-free bias current, \( I_{n,\text{PM4}}^2 \) obtained is in the order of \( 10^{-18} \) to \( 10^{-24} \), which is shown in Fig. 6.
Fig. 6. Comparison plot of noise spectrum of biasing current ($\bar{I}_{n,bias}^2$) and biasing current ($\bar{I}_{n,PM4}^2$) vs. frequency.

The use of a low pass filter in the biasing circuit reduces the noise contribution of each MOSFET (PM$_{REF1,2}$, PM$_{lpf1,2}$, PM$_{3,4,5}$, and NM$_{3,4,5}$) in the biasing circuit. The spot noise analysis at 1 kHz gives $1.18610^{-8}$ $V_{rms}$ for the proposed FEA. Here, the noise of biasing MOSFET’s (PM$_{REF1,2}$, PM$_{lpf1,2}$, PM$_{3,4,5}$, and NM$_{3,4,5}$) decreased to the order of $10^{-18}$, which is almost zero percent, and only input stage MOSFET's (PM$_{1,2}$ and NM$_{1,2}$) contributing noise as shown through pie-chart in Fig. 7.

![Pie Chart for Noise Contribution](image)

Fig. 7 Noise Contribution pie-chart.

Moreover, the input-referred noise can be optimized by incorporating techniques into conventional FEA design. In general, the equivalent noise circuit of MOSFET has thermal noise ($\bar{v}_{n,RG}^2$ and $\bar{i}_{n,ch}^2$) and flicker noise ($\bar{v}_{n,f}^2$), which are uncorrelated to one another. Here, voltage noise spectrum ($\bar{v}_{n,RG}^2$) is induced by gate distributed resistance ($R_G$), current noise spectrum ($\bar{i}_{n,ch}^2$) induced across the channel, and voltage noise spectrum ($\bar{v}_{n,f}^2$) is induced due to improper bonds at the Si-SiO$_2$ interface of the MOSFET. Even though flicker noise is dominant in sub-Hz frequencies, thermal noise is not ignoble in the comprehensive noise metric for the same frequency range [22]. The side view of the MOSFET structure and its complete noise equivalent is shown in Fig. 8 (a) and 8 (b), respectively.
Fig. 8. (a) Sideview representation of MOSFET and (b) the overall noise equivalent of a MOSFET.

The total noise spectrum ($v_{n,\text{Total}}^2$) of the MOSFET can be expressed in (12)

$$v_{n,\text{Total}}^2 = v_{n,\text{RG}}^2 + v_{n,f}^2 + t_{n,\text{ch}}^2 r_o^2$$  \hspace{1cm} (12)$$

Where $r_o$ represents the channel resistance of the MOSFET. It is observed that increasing the transconductance of input stage MOSFET’s could suppress both flicker noise and thermal noise. Here operating input stage of MOSFET’s $PM_1, PM_2, NM_1, \text{and } NM_2$ in the deep subthreshold region can increase the transconductance ($g_m$) of corresponding MOSFET’s. In the deep subthreshold, the MOSFET current $I_{DS}$ is exponential dependant on the gate to source voltage $V_{GS}$; thus, transconductance upon $I_{DS} (g_m/I_{DS})$ is higher in the deep subthreshold region in comparison to strong inversion. While in strong inversion, $g_m/I_{DS}$ is dependent on $I_{DS}^{-0.5}$, but it is a fixed value of $q/(mkT)$ in deep sub-threshold region, where $q$ is a charge of electron $1.6*10^{-19}$ C, $k$ is Boltzmann constant, $T$ is the absolute temperature and $m = (g_{mb} + g_m)/g_m$ (here, $g_{mb}$ is transconductance parameter of body effect) [4]. Therefore, the gain of FEA upon D.C. power in deep subthreshold becomes very high as compared to strong inversion. Moreover, operating input stage MOSFET’s in deep subthreshold also decreases the high pass corner frequency, which is achieved around to be 1mHz. Hence, increasing the gain of FENA can increase the input impedance ($Z_{in}$) with the
deferred output signal of 498.82 μS in the post-layout. Furthermore, the thermal noise can be decreased by considering fingers to each of the MOSFET in FENA. The fingers fold the MOSFET, which decreases both source and drain area, thus decreasing both gate distributed resistance \((R_G)\), and parasitic capacitance \((C_p)\) of corresponding MOSFET’s. Here for the sake of simplicity, MOSFET\((PM_4)\) is only considered to explain the concept of fingers. Here, assuming one finger for the \(PM_4\), which is shown in Fig. 9(a) where its distributed gate resistance value would be \((R_G)\), and its voltage noise spectrum due to \(R_G\) is \(v_{n,RG4}^2\) and it can be expressed in (13) [2].

\[
v_{n,RG4}^2 = 4KT \frac{R_G}{3}
\]

Then, the total output voltage \(v_{on,Total}^2\) spectrum noise for the same MOSFET can be expressed below in equations (14), (15), and (16), respectively.

\[
v_{on,Total}^2 = v_{n,RG4}^2 + v_{n,fn}^2 + v_{n,PM4}^2 r_o^2
\]

\[
v_{on,Total}^2 = 4KT \frac{R_G}{3} \left( \frac{1}{C_{ox}} \frac{1}{WL} \right) + 4KT \gamma g_m r_o^2
\]

\[
v_{on,Total}^2 = 4KT \frac{R_G}{3} \left( \frac{1}{C_{ox}} \frac{1}{WL} \right) + 4KT \gamma g_m r_o^2
\]

Where \(\gamma\) is a constant and it is a technology dependant parameter which is generally considered as a value of 3. Now by taking four fingers for the \(PM_4\) (as shown in Fig. 9(b)), the distributed gate resistance value is minimized to \(\frac{R_G}{16}\) i.e., \((\frac{R_G}{\text{no of fingers}^2})\). Hence, the noise component introduced by distributed gate resistance can reduce drastically. Now with four fingers MOSFET \(PM_4\), voltage noise spectrum due to\(R_G\) is \(v_{n,RGF4}^2\), which can be expressed as equations (17) and (18), respectively.

\[
v_{n,RGF4}^2 = 4KT \frac{R_G}{3} \frac{1}{4^2}
\]

\[
v_{n,RGF4}^2 = 4KT \frac{R_G}{48}
\]

Now with four fingers, the total voltage noise spectrum \(v_{on,Total}^2\) of the same MOSFET is expressed as below in (19).

\[
v_{on,Total}^2 = 4KT \frac{R_G}{48} \left( \frac{1}{C_{ox}} \frac{1}{WL} \right) + 4KT \gamma g_m r_o^2
\]
Fig. 9 $PM_4$ transistor with its (a) Single finger representation and (b) Optimization using four fingers representation.

Here the finger width of every transistor, appropriate number of fingers are considered without effecting other metrics using $gm$ over $id$ algorithm. By doing so, gate parasitic capacitance ($C_p$) of the overall proposed FENA is minimum (in the order of fF), eventually giving minimum leakage current (in the order of fA) for the common mode voltage range 0.4 V to 0.8 V in the post-layout, thus resulting improvement in noise metric as shown in the plot of Fig. 10.

Fig. 10 Post layout result of parasitic capacitance and Leakage current versus common mode voltage.

3.2 $G_m/I_d$ Algorithm to Improve Noise-Metric

Miniaturization leads to include short channel effects and the performance metric deviates from the superficial theoretical results. A flawless $G_m/I_d$ algorithm needs to be adopted for submicron technologies [23]. The algorithm endorsed to attain ultra-low noise, which is very much useful in monitoring electrical activities of neuron. Here the comparison of $G_m/I_d$ with regularized drain current ($I_d$ over aspect ratio) improved the noise metric. In the proposed
current biasing circuit $R_{\text{LPF}}$ is optimized by fixing $C_{\text{LPF}}$ (nominal value of 51fF). Using $g_m$ over $I_d$ iterations algorithm it is observed that $R_{\text{LPF}}$ proportionally depend on PM$_{\text{REF2}}$ size but inversely depends on its own size, and transconductance of PM$_{\text{REF2}}$. Thus noise current factor, $\frac{I_n}{I_{\text{PM4}}}$ well controlled by $R_{\text{LPF}}$ and $C_{\text{LPF}}$. This algorithm also useful for deciding dimensions to operate PM$_{1,2}$ in deep subthreshold, and also administrates while considering appropriate number of fingers for each MOSFET. The flowchart of procedure to improve noise metric is shown in the Fig.11.

Fig. 11 $G_m/I_d$ algorithm to improve noise metric

Here Table.1 lists the dimensions of each device used in FENA.

**Table. 1 Dimensions of proposed FENA**

<table>
<thead>
<tr>
<th>Device</th>
<th>Size (M*W/L)</th>
<th>Number of Fingers</th>
</tr>
</thead>
<tbody>
<tr>
<td>PM$_{\text{REF 1,2}}$</td>
<td>4*7.5 µm / 2µm</td>
<td>2</td>
</tr>
<tr>
<td>PM$_{1,2}$</td>
<td>4*3.75 µm / 1 µm</td>
<td>2</td>
</tr>
<tr>
<td>PM$_3$</td>
<td>8*7.5 µm / 2µm</td>
<td>2</td>
</tr>
<tr>
<td>PM$_{4,5}$</td>
<td>8*7.5 µm / 2 µm</td>
<td>4</td>
</tr>
<tr>
<td>PM$_{\text{LPF 1,2}}$</td>
<td>1*160 nm / 3 µm</td>
<td>1 (considered due to minimum width)</td>
</tr>
<tr>
<td>NM$_{1,2}$</td>
<td>4*750 nm / 2 µm</td>
<td>2</td>
</tr>
<tr>
<td>NM$_{3,4}$</td>
<td>4*250 nm / 1 µm</td>
<td>2</td>
</tr>
</tbody>
</table>
### 3.3 Process Voltage Temperature (PVT) Variations

Here, the analysis of PVT variations using Monte-Carlo simulations is evaluated and discussed. To that match the input differential amplifier, inter digitized centroid layout technique is applied to the input stage MOSFET’s (PM_{1} with PM_{2} and NM_{1} with NM_{2}) [21]. Both PM_{1} and PM_{2} have a multiplier value of 4, i.e., PM_{1} has four elements PM_{11}, PM_{12}, PM_{13}, and PM_{14}. Similarly PM_{2} has four elements from PM_{21}, PM_{22}, PM_{23} and PM_{24}. In the inter-digitized centroid layout, PM_{1} elements, PM_{11}, and PM_{12}, are placed in the center with edges as PM_{2} elements, while PM_{21}, and PM_{22} as in row1. In row2, PM_{2} elements PM_{23} and PM_{24} are placed in the center with edges as PM_{1} elements while PM_{13}, and PM_{14} as in row2 which are in Fig. 12, and the same is applied to NM_{1} and NM_{2}.

![Fig. 12. Inter-digitized centroid layout to PM_{1} with PM_{2}.](image)

By Monte-Carlo analysis, Process Voltage Temperature (PVT) variations are observed for the gain (at three different temperatures 27°C, −40°C, and 125°C), bandwidth (27°C) with 1000 samples (N). The mean (µ) of gains is 79.19 dB, 81.62 dB, and 74.21 dB with standard deviation(σ) of 1.93, 4.38, and 0.7, respectively, which are shown in Fig. 13(a) to 13(c), respectively. The mean (µ) of unity gain-bandwidth is 3.71 MΩ with standard deviation (σ) of 0.2 MΩ for the temperature of 27°C as shown in Fig. 12(d). For the input-referred noise, Fast Fast(FF-Best case), Typical Typical (TT-Normal), Slow Slow (SS-Worst case) corners analysis at −40°C, 27°C, and 125°C with a varying supply voltage of 1.08 V, 1.2 V and 1.32 V are executed. It is observed that the same type of corners is coinciding with one another (i.e., all F.F. corners are coinciding), the input-referred noise (v/√Hz) values are $5.63 \times 10^{-14}$, $1.87 \times 10^{-14}$, $9.48 \times 10^{-15}$ at 1KHz for the F.F., T.T. and S.S. corners respectively, which are shown in Fig. 14.
Fig. 13. PVT Variations with (a) Gain at $27^0C$, (b) Gain at $-40^0C$, (c) Gain at $125^0C$, and (d) Unity gain bandwidth at $27^0C$

Fig. 14. PVT variations at extreme corners for input referred noise

4. Results and Discussion

In this section, the performance evaluation of the FENA will be discussed. The FENA design and its full layout are made using 65 nm CMOS technology in cadence virtuoso design tool. The layout of the proposed FENA is implemented with inter digitized centroid technique, which occupies a chip area of 0.0023 $mm^2$ as shown in Fig. 15.
The performance of FENA commences with a voltage gain, which is obtained at about 60 dB in the simulation scenario. In the biasing circuit, MOSFET $P_{M_{REF}}$ is placed in the center, and remaining biasing MOSFET's are placed around the same in the layout, ensuring even distribution of bias current, operating transistors with high $g_m/I_d$, resulting in a splendid gain of 80 dB but moderate unity gain bandwidth of 4 MHz in the post layout result which can be seen in Fig. 16. By adopting low pass filter, reducing $R_G$, proposed FENA design achieves an ultra-low noise of 18 $fV/\sqrt{Hz}$, input referred noise at 10 kHz, which is shown in Fig. 17.
Moreover, as the implicit resistance is reduced by inter digitized centroid in the layout, the proposed FENA provides post layout input impedance value \( (Z_{in}) \) of 200 GΩ over a simulated value of 1.47 TΩ, in the sub-Hz frequencies, which is shown in Fig. 18. Arranging biasing MOSFET’s properly, later inter digitization of input stage together increased the matching among MOSFET's to improve the linearity. Fig. 19 shows total harmonic distortion (THD) vs. frequency characteristics, with ten harmonics of a sine wave for an input of 1mVpp at 1 kHz, and THD is achieved as -68 dB.
Operating in subthreshold, high \( \text{gm/}I_D \) provided optimum power supply rejection ratio (PSRR) of the proposed FENA is approximately 95 dB and 80 dB for simulated and Post layout results, respectively, as depicted below in Fig. 20.

In addition, the noise efficient factor for the FENA is expressed as (20).

\[
\text{NEF} = \frac{v_{\text{in,rms}}}{\sqrt{\frac{2 I_{\text{bias}}}{4kT \pi V_T B.W}}}
\]

(20)

Where, \( v_{\text{in,rms}} \) is the input-referred noise in RMS (root mean square), \( I_{\text{bias}} \) total biasing current, \( K \) is Boltzmann constant, \( T \) is Temperature, \( V_T \) is thermal voltage, and \( B.W. \) is the bandwidth of the FENA. As this FENA can provide less input-referred noise, NEF values
improved to 0.09 and 0.27 for the AP (300 Hz to 7.5 KHz), LFP (25 mHz to 100 Hz), respectively. The comparison of proposed FENA with other referred ones is shown in Table 2 (Post-layout results). Even though this FENA competes with others in most of the metrics, however moderate unity gain bandwidth of 4 MHz and the deferred output signal of 498.82 µS is observed in the post-layout.

Table 2: Performance comparison of proposed FENA’s with other works

<table>
<thead>
<tr>
<th>Parameter / FENA’s</th>
<th>[18]</th>
<th>[10]</th>
<th>[16]a</th>
<th>[19]</th>
<th>[24]a</th>
<th>[12]</th>
<th>This work</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology</td>
<td>0.18</td>
<td>0.13</td>
<td>0.18</td>
<td>0.35μm</td>
<td>0.18μm</td>
<td>0.13μm</td>
<td>65 nm CMOS</td>
</tr>
<tr>
<td>Biasing Technique</td>
<td>CCF</td>
<td>CA</td>
<td>FL</td>
<td>NCF</td>
<td>Tunable Bandwidth</td>
<td>Chopper Stabilization</td>
<td>PDF</td>
</tr>
<tr>
<td>Chip area (mm²)</td>
<td>0.025</td>
<td>0.072</td>
<td>-</td>
<td>0.042</td>
<td>0.048</td>
<td>-</td>
<td>0.0023</td>
</tr>
<tr>
<td>Supply voltage (V)</td>
<td>1.8</td>
<td>1</td>
<td>0.6</td>
<td>3.3 a</td>
<td>1</td>
<td>1 a</td>
<td>1</td>
</tr>
<tr>
<td>Power (µW)</td>
<td>7.6</td>
<td>12.1</td>
<td>0.72</td>
<td>3.1 a</td>
<td>3.6</td>
<td>2.3 a</td>
<td>1</td>
</tr>
<tr>
<td>Input Referred Noise (v/√Hz)</td>
<td>5.6 μ</td>
<td>2 μ</td>
<td>1 μ</td>
<td>18.2 n a</td>
<td>2.1 μ</td>
<td>64n a</td>
<td>35 f (at 1 kHz)</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>14</td>
<td>40</td>
<td>40</td>
<td>75 a</td>
<td>45-55</td>
<td>55 b</td>
<td>80</td>
</tr>
<tr>
<td>Bandwidth (Hz)</td>
<td>23 K</td>
<td>10.5 K</td>
<td>10 K</td>
<td>22.8 M a</td>
<td>8.2 K</td>
<td>1.1 K b</td>
<td>4 M (Gain=0)</td>
</tr>
<tr>
<td>Input Impedance (Ω)</td>
<td>60G a</td>
<td>4 M</td>
<td>16 M</td>
<td>42 G b</td>
<td>-</td>
<td>-</td>
<td>200 G</td>
</tr>
<tr>
<td>CMRR (dB)</td>
<td>61</td>
<td>-</td>
<td>77</td>
<td>-</td>
<td>98.28</td>
<td>115 to 125&lt;sup&gt;b&lt;/sup&gt;</td>
<td>77</td>
</tr>
<tr>
<td>PSRR (dB)</td>
<td>57</td>
<td>-</td>
<td>60</td>
<td>-</td>
<td>92.48</td>
<td>-</td>
<td>80</td>
</tr>
<tr>
<td>THD (dB)</td>
<td>&lt;1</td>
<td>-</td>
<td>75</td>
<td>-</td>
<td>-46.32</td>
<td>-</td>
<td>-68</td>
</tr>
<tr>
<td>Noise Efficiency Factor : AP</td>
<td>4.7</td>
<td>-</td>
<td>2.13</td>
<td>-</td>
<td>1.7</td>
<td>3.8&lt;sup&gt;a&lt;/sup&gt;</td>
<td>0.09</td>
</tr>
<tr>
<td>Noise Efficiency Factor : LFP</td>
<td>9.6</td>
<td>-</td>
<td>2.13</td>
<td>-</td>
<td>1.7</td>
<td>3.8&lt;sup&gt;a&lt;/sup&gt;</td>
<td>0.27</td>
</tr>
<tr>
<td>High pass corner Frequency (Hz)</td>
<td>0.01</td>
<td>-</td>
<td>10 m</td>
<td>300 m&lt;sup&gt;a&lt;/sup&gt;</td>
<td>0.8</td>
<td>0.1&lt;sup&gt;a&lt;/sup&gt;</td>
<td>1 m</td>
</tr>
</tbody>
</table>

<sup>a</sup>Simulated results, <sup>b</sup>Measurement results.

### 5. Conclusion

In this paper, proposed FENA with a LPF has been proposed which occupies less area of 0.0023 mm<sup>2</sup>, which increases the feasibility to implantable and wearable neuro-sensing devices. The gm over Id algorithm endorsed to attain Noise-free biasing current, and TULN-OTA yields ultra-low noise of 18 fV/√Hz input referred noise at 10 kHz, which is very much useful in monitoring electrical activities of neuron. This can achieve input impedance of 200 GΩ at 1mHz while consuming 1 μW of power. The inter digitized centroid layout not only decreases leakage current but also ensures FENA, matching of input stage differential amplifier. FENA able to provide a splendid post-layout gain of 80 dB which is very useful for bio-medical low potentials with moderate unity gain bandwidth of 4 MHz and deferred output signal of 498.82 μS.

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**Declarations:** Conflict of interest

The authors declare that they have no conflict of interest.

**Data availability:** The datasets generated and/or analysed during the current study are available from the corresponding author on reasonable request

**References:**


