

A SiGe-Source Doping-Less Double-Gate Tunnel FET: Design and Analysis Based on Charge Plasma Technique with Enhanced Performance

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Abstract

In this article, a distinctive charge plasma (CP) technique is employed to design two doping-less dual gate tunnel field effect transistors (DL-DG-TFETs) with $\text{Si}_{0.5}\text{Ge}_{0.5}$ and Si as source material. The CP methodology resolves the issues of random doping fluctuation and doping activation. The analog and RF performance has been investigated for both the proposed devices i.e. $\text{Si}_{0.5}\text{Ge}_{0.5}$ source DL-DG-TFET and Si-source DL-DG-TFET in terms of drive current, transconductance, cut-off frequency. In addition, the linearity and distortion analysis has been carried out for both the proposed devices with respect to higher order transconductance (g_{m2} and g_{m3}), VIP2, IMD3, and HD2. The $\text{Si}_{0.5}\text{Ge}_{0.5}$ source DL-DG-TFET has better performance characteristics and reliability in compare to Si-source DL-DG-TFET owing to low energy bandgap material and higher mobility. The switching ratio obtained for $\text{Si}_{0.5}\text{Ge}_{0.5}$ source DL-DG-TFET is order of 5×10^{14} that makes it a suitable contender for low power applications.

I. Introduction

In the coming decade, Moore's law will be relevant only by scaling down the power consumption along with process size. Miniaturizing the size of MOSFETs give rise to various issues related to leakage power, fabrication, subthreshold swing (SS), gate induced drain lowering (GIDL), and several other second order effects [1], [2].

These complications enforce to search for the novel devices, whose working philosophy is other than thermionic emission. In this aspect, Tunnel FET has come up as a strong candidate to outplay the conventional MOSFETs. TFETs exhibits low leakage current, SS below 60 mV/decade, and minimized SCEs due to its in-built tunneling barrier. The advantage of TFETs over MOSFETs is its better performance below 1 V.

TFETs employ band to band tunneling; the OFF-state current obtained is low due to large tunneling width for smaller biasing which prohibits the tunneling of charge carriers. The constraint of TFETs till date is low ON current and high ambipolar current [3].

The ambipolar effect can be minimized by employing lightly doped drain region and gate-drain underlap [4]. The tunneling path increases at channel-drain junction by decreasing the doping concentration of drain that suppresses the ambipolar current. To increase the drain current, various methods have been reported such as high-k dielectric engineering [5], L-shaped gate [6], triple material double gate [7], heterojunction [8], hetero dielectric [9], junctionless [10]. The inclusion of ferroelectric material as gate insulator also increases the tunneling rate that further increase the drive current and suppresses the subthreshold swing [11][12].

The double gate methodology provides better electrostatics restriction over the channel that enhances the device characteristics by increasing the inversion charge carriers. Incorporation of low band gap materials such as $\text{Si}_v\text{Ge}_{1-v}$, Ge, or InAs at source side minimizes the tunneling path thereby increasing the

ON-state current [13]. Another issue is of uniform doping that originates during fabrication process; due to scaling down the doping becomes very difficult and costly for the formation of p-n junction. The junction less transistors (JLTs) were introduced by Tyndall's group that does not has any metallurgical junction and has uniform high doping throughout the source, channel and drain regions [14]. The JLTs suffered from random dopant fluctuations (RDF) [15] that severely deteriorates the characteristics of the device.

In order to address the RDF effects, charge plasma methodology has been suggested by Rajasekharan et al [16] to enhance the device performance. Charge plasma techniques is a high temperature process that employs electrodes with suitable work functions to induce doped drain and source regions on an undoped substrate i.e. doping-less (DL) [17].

In this work, charge plasma technique along with low band gap material at source is employed to improve the performance of double gate tunnel FET (DL-DG-TFET). The $\text{Si}_{0.5}\text{Ge}_{0.5}$ and Si based source doping-less DG-TFETs are compared in accordance with analog, RF, linearity and distortion performance metrics. Furthermore, the linearity and distortion analysis of the two devices i.e. $\text{Si}_{0.5}\text{Ge}_{0.5}$ source DL-DG-TFET and Si source DL-DG-TFET has been carried out. The aim is to obtain the improved performance of the device in terms of ON-current, subthreshold swing, linearity, and distortion.

ii. Device Dimensions And Models

The 2-D structures of the intended devices, DL-DG-TFET with $\text{Si}_{0.5}\text{Ge}_{0.5}$ and Si source has been presented in figure 1(a) and (b) respectively. The undoped source, drain, and channel regions of the proposed device are formed on an intrinsically doped Si film with $n_i=10^{15} \text{ cm}^{-3}$. The thickness of undoped Si body is 5 nm. Charge plasma methodology has been employed in order to induce doping in the source and drain regions of the proposed devices. Charge plasma technique is applicable only when the Debye length is greater than channel thickness.

The drain region material of both the proposed devices are same to obtain the low OFF-state current, however, the source material in one of the device is a low band gap material i.e. $\text{Si}_{0.5}\text{Ge}_{0.5}$, to achieve high drive current.

The two gates are connected with the device namely control gate and fixed gate. Control gate is present above the channel region to control the flow of majority charge carriers. However, the fixed gate is located above the source region to create the p-type doping in source. Control and fixed gate are isolated by spacer (SiO_2) of length 2 nm. The work function of fixed gate and source electrode is selected to be 5.93 eV (Platinum) to induce p-type doping (accumulation of positive charges) in source region. Furthermore, the work function of drain electrode is 3.9 eV (Hafnium) to induce n-type doping in drain region. The work function of control gate is 4.2 eV (Aluminium). The insulator (SiO_2) thickness for both the device is 2 nm. For optimum performance, the mole fraction of SiGe is taken as 0.5 [17]. The channel length for both the proposed devices is 22 nm; drain and source regions is of 20 nm each.

Numerical calculations has been carried out by using 2D device simulator, Silvaco TCAD, for both the proposed devices. The models used during the numerical simulation are Shockley-Read Hall recombination model, Lombardi mobility model, quantum model, non-local BTBT model, and phonon-assisted tunneling model. Non local model inspects the spatial variation of energy bands. Quantum model was employed as the thickness of channel is 5 nm.

iii. Results And Discussion

In this work, the performance analysis has been carried out for the proposed devices DL-DG-TFET with Si and Si_{0.5}Ge_{0.5} source. The numerical calculation models utilized for the analysis are calibrated against the previously published result [18]. In order to fine-tune the Kane's tunneling model, its tunneling masses are tuned from their standard values to a adjusted value, i.e. $m_{e.tunnel} = 0.272m_0$ and $m_{h.tunnel} = 0.54m_0$, where m_0 is the electron rest mass. Figure 2 shows the model validation, all the dimensions and doping parameters are kept identical to that of [18].

The energy band diagram variation along the channel in OFF and ON-state for both the proposed devices is shown in Fig. 3(a) and 3(b), respectively. In OFF-state the gate voltage ($V_{GS} = 0$ V) is zero, and drain voltage ($V_{DS} = 1$ V) is 1 V. However, in the ON-state the $V_{GS} = 1$ V, and $V_{DS} = 1$ V. The incorporation of low band gap material (Si_{0.5}Ge_{0.5}) at source side reduces the tunneling path, as it can be observed from Fig. 3(b). Consequently, the reduction in tunneling path minimizes the tunneling resistance and enhances the tunneling of charge carriers. The band gap of Si_{0.5}Ge_{0.5} is 0.94 eV, which is smaller than Si, minimizes the tunneling path that additionally increases the tunneling rate of charge carriers. The WKB tunneling probability approximation of Si_{0.5}Ge_{0.5} source DL-DG-TFET is given below:

$$T(E) = \exp\left(-\frac{4\lambda\sqrt{2m^*E_g^{1.5}}}{3qh(E_g + \Delta\phi)}\right) \quad (1)$$

$$\lambda = \sqrt{\frac{\epsilon_{Si}t_{Si}t_{ox}}{\epsilon_{ox}}} \quad (2)$$

where λ is screening length, E_g is energy bandgap, $\Delta\phi$ is potential difference between source valence band and channel conduction band, and m^* is effective mass. It can be observed from (1) that tunneling probability increases with low energy bandgap and low effective mass. Therefore, the tunneling probability is high for Si_{0.5}Ge_{0.5} source DL-DG-TFET that can be reflected from Fig. 4 with increased BTBT rate, as the Si_{0.5}Ge_{0.5} has lower energy band gap in contrast to Si.

Figure 5 visualizes the variation of surface potential along the channel for both the proposed devices. In addition, the enhanced tunneling rate of Si_{0.5}Ge_{0.5} source DL-DG-TFET reflects higher surface potential.

The electron concentration for the proposed devices DL-DG-TFET with Si and Si_{0.5}Ge_{0.5} source has been

shown in Fig. 6. It can be observed from Fig. 6 that the electron concentration for Si_{0.5}Ge_{0.5}-source based device is higher in contrast to Si-source. This fashion remains same until the graph reaches the drain region; further the electron concentration becomes equal for both the intended structures as the drain material is identical.

Figure 7 represents the transfer characteristics for both the proposed devices. The ON-current of Si_{0.5}Ge_{0.5}-source based device is higher in contrast to Si-source. However, OFF-current of both the devices remains same; this leads to enhance the switching ratio (I_{ON}/I_{OFF}) for Si_{0.5}Ge_{0.5}-source based device. The drive current depends on the tunnel resistance and channel resistance. However, the tunneling width of Si_{0.5}Ge_{0.5}-source is smaller in contrast to Si-source based device, which is reflected in Fig. 3(b). Tunneling width totally depends on the tunneling resistance that is caused by proper gate to source voltage. Thus, the smaller tunneling width leads to higher drive current for Si_{0.5}Ge_{0.5}-source in compare to Si-source. The drive current and switching ratio obtained for Si_{0.5}Ge_{0.5} source based device are 71.4 $\mu\text{A}/\mu\text{m}$ and order of 5×10^{14} , respectively.

The transconductance (g_m) variation for both the proposed devices is shown in Fig. 8. Transconductance is the significant device parameter, it evaluates the current driving potentiality of the device and is calculated as $\partial I_D / \partial V_{GS}$ keeping V_{DS} constant. It is evident from the Fig. 7 that since I_D has higher value for Si_{0.5}Ge_{0.5}-source based device, therefore, g_m will certainly be high due to direct dependence of g_m with respect to drain current.

Figure 9(a) and 9(b) presents the graph of total gate capacitance and cut-off frequency, respectively, against V_{GS} for both the proposed structures. Total gate capacitance (C_{GG}) is calculated by the summation of gate-to-source capacitance (C_{GS}) and gate-to-drain capacitance (C_{GD}). From figure 6, it is evident that the electron concentration for Si_{0.5}Ge_{0.5}-source based device is higher; this leads to increase in total gate capacitance of the device because of increase in gate-to-source capacitance. Therefore, C_{GG} for Si_{0.5}Ge_{0.5}-source based device has higher value in compare to Si-source. Cut-off frequency reflects the maximal frequency that can be escalated by a discrete device and can be expressed as:

$$f_T = \frac{g_m}{2\pi C_{GG}} \quad (3)$$

The direct dependence of cut-off frequency with transconductance confirms that higher value of g_m will certainly have higher value of f_T . Hence, it has been observed from Fig. 9(b) that cut-off frequency of Si_{0.5}Ge_{0.5}-source based device is higher as its drain current and transconductance has higher value in contrast to Si-source based device.

The gain-bandwidth product (GBP) is an important metric for RF analysis and is expressed as:

$$GBP = \frac{g_m}{2\pi \times 10^9 * C_{GD}} \quad (4)$$

GBP has direct dependence on ratio of transconductance and parasitic capacitance. Figure 10 shows GBP variation with respect to V_{GS} for both the proposed structures. The GBP graph increases with V_{GS} due to increase in transconductance and reduction in parasitic capacitance. Higher value of transconductance for $Si_{0.5}Ge_{0.5}$ -source in compare to Si-source, results in higher value of its GBP, as can be observed from Fig. 10. Transconductance frequency product (TFP) is another important figure of merit (FOM) for RF performance, which is expressed as:

$$TFP = \left(\frac{g_m}{I_D} \right) \times f_T \quad (5)$$

Figure 11 presents the TFP variation with respect to V_{GS} for both the proposed structures. TFP shows the compromise between power and bandwidth [19]. It has been observed from Fig. 11 that TFP of $Si_{0.5}Ge_{0.5}$ -source is higher in contrast to Si-source based device due to higher value of g_m and f_T .

The linearity parameters has been evaluated in order to analyse the device for distortion free output. In order to improve linearity, the transconductance of the device should be invariant with regard to V_{GS} [20]. Unfortunately, the transconductance of TFET varies with gate voltage that depicts the non-linear characteristics of TFET. The higher order transconductance (g_{m2} and g_{m3}) are shown in Fig. 12 for both the proposed devices that depicts non-linear characteristics of device. The main reason of non-linearity is the involvement of higher order transconductance with the fundamental frequency. In contrast to g_{m2} , g_{m3} is more related in evaluating the non-linearity of the device. The balanced techniques can be employed to minimize the even harmonics, however g_{m3} is not controllable. In order to attain the least distortion, the magnitude of both high order transconductance (g_{m2} and g_{m3}) should be low. The g_{m2} and g_{m3} increases for $Si_{0.5}Ge_{0.5}$ -source based device in compare to Si-source that can be viewed from Fig. 12, therefore the linearity of the device is enhanced for latter case.

Other FOMs such as VIP2 and IMD3 have been plotted with respect to V_{GS} in Fig. 13 (a) and 13 (b) respectively. VIP2 is an extrapolated input voltage for which fundamental and second harmonic voltage are equal. IMD3 is the third order intermodulation distortion that depicts the extrapolated current at which the fundamental and third order intermodulation harmonic currents are equal. In order to attain high linearity and low distortion, higher values of VIP2 and lower values of IMD3 are required. Fig. 13 (a) presents the higher values of VIP2 for $Si_{0.5}Ge_{0.5}$ -source that depicts the improved linearity in contrast to Si-source. The lower values of IMD3, as shown in Fig. 13(b), for $Si_{0.5}Ge_{0.5}$ -source confirms to have low internal noise in contrast to Si-source based device.

The second-order harmonic distortion (HD2) is a critical parameter of distortion. In order to minimize the Loading [MathJax]/jax/output/CommonHTML/fonts/TeX/fontdata.js as possible. Figure 14 presents the graph of

HD2 against V_{GS} for both the proposed structures, it can be depicted from the graph that for $Si_{0.5}Ge_{0.5}$ source, the value of HD2 is lower in compare to Si-source. Hence, it can be summarised that $Si_{0.5}Ge_{0.5}$ source based TFET has better linearity, reliability and reduced distortion then Si-source based TFET.

IV. Conclusion

In this article, CP based technique has been introduced to design the doping-less dual gate structure with Si and $Si_{0.5}Ge_{0.5}$ source. The analog, RF, linearity and distortion analysis has been carried out for both the proposed structures. The $Si_{0.5}Ge_{0.5}$ source based DL-DG-TFET has better characteristics in compare to Si-source based DL-DG-TFET due to assimilation of a low bandgap material in the source region. The drive current and switching ratio obtained for $Si_{0.5}Ge_{0.5}$ source DL-DG-TFET are $71.4 \mu A/\mu m$ and order of 5×10^{14} , respectively. The improved linearity and distortion metrics for $Si_{0.5}Ge_{0.5}$ source DL-DG-TFET in compare to Si-source DL-DG-TFET makes it a worthy contender for low power applications.

Declarations

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Availability of data and material: The research data of this manuscript will not be available.

Compliance with ethical standards: This article does not contain any studies involving animals or human participants performed by any of the authors.

Consent to participate: Not Applicable

Consent for Publication: Yes

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$\text{Si}_x\text{Ge}_{1-x}$

$\text{Ge}_x\text{Si}_{1-x}$

$\text{Si}_x\text{Ge}_{1-x}$

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Figures

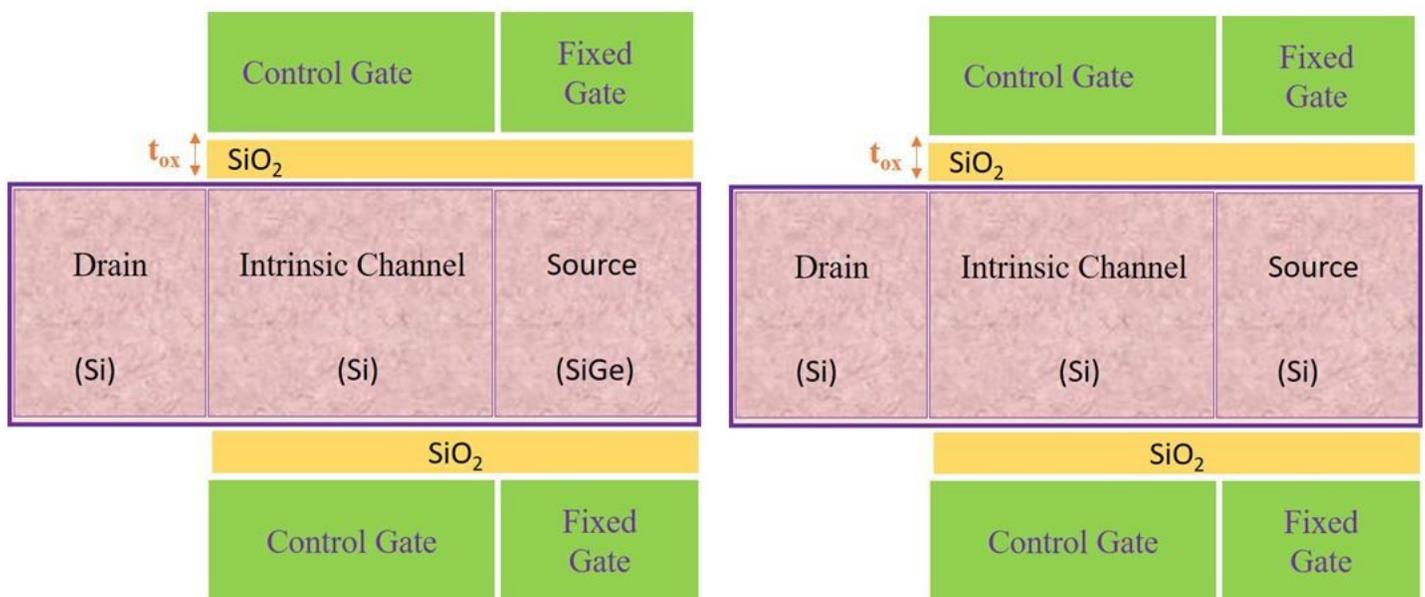


Figure 1

2-D structures of DL-DG-TFET with (a) Si_{0.5}Ge_{0.5} source, and (b) Si source.

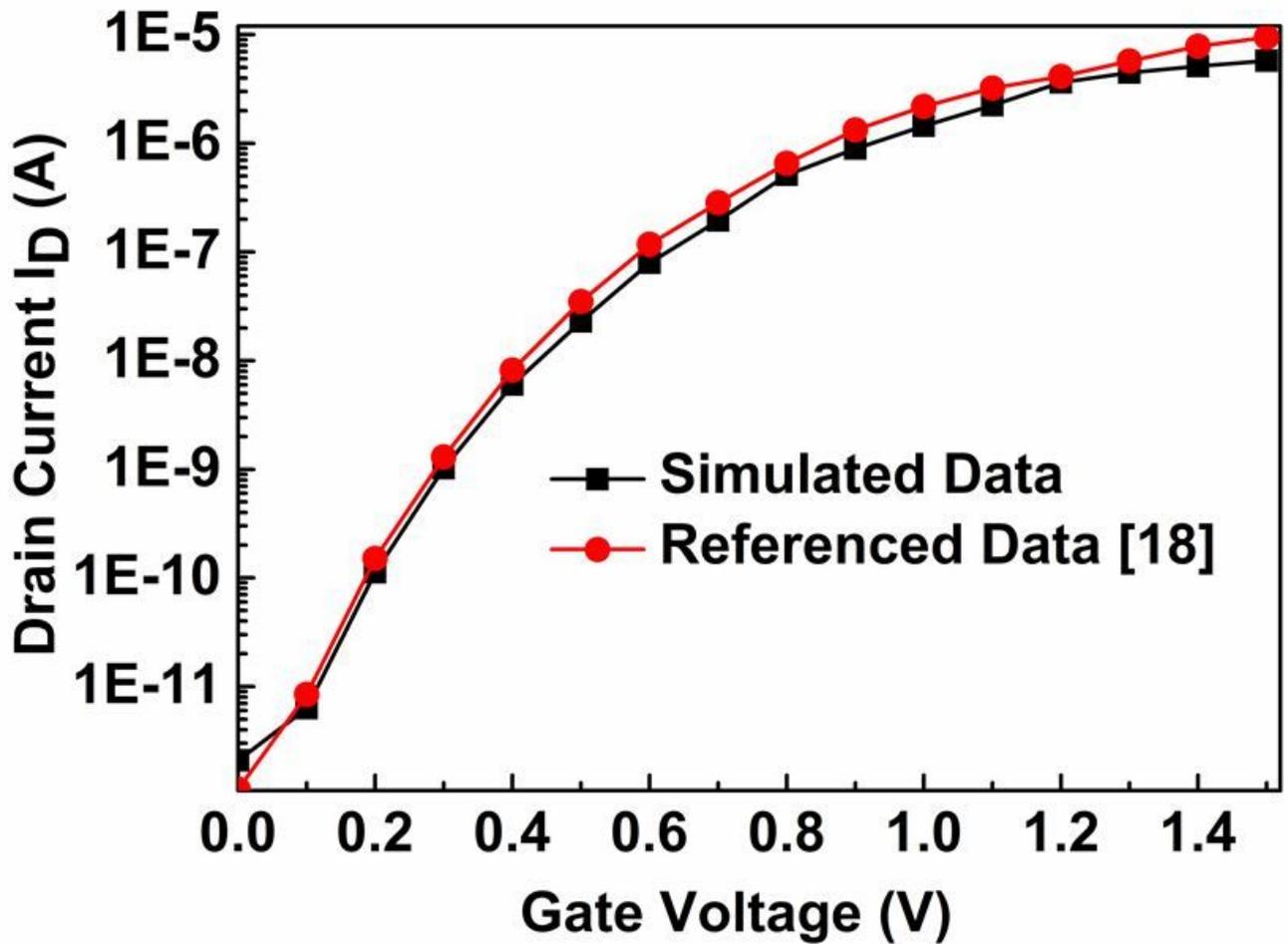
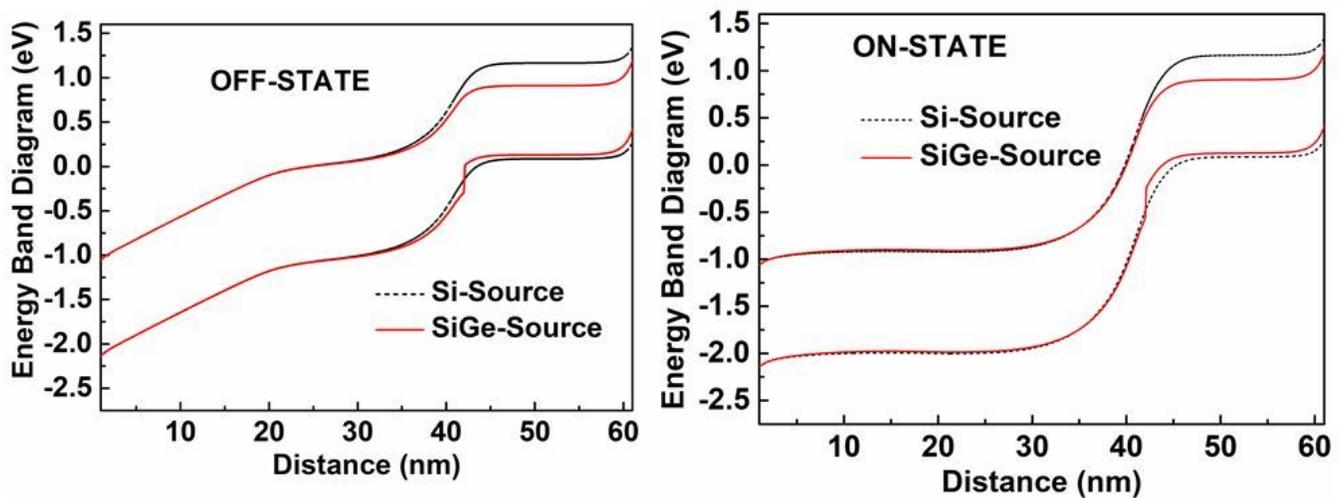


Figure 2

Validation curve with the published experimental work [18].



Energy band diagram of DL-DG-TFET with Si_{0.5}Ge_{0.5} source and Si source in (a) OFF-state, and (b) ON-state.

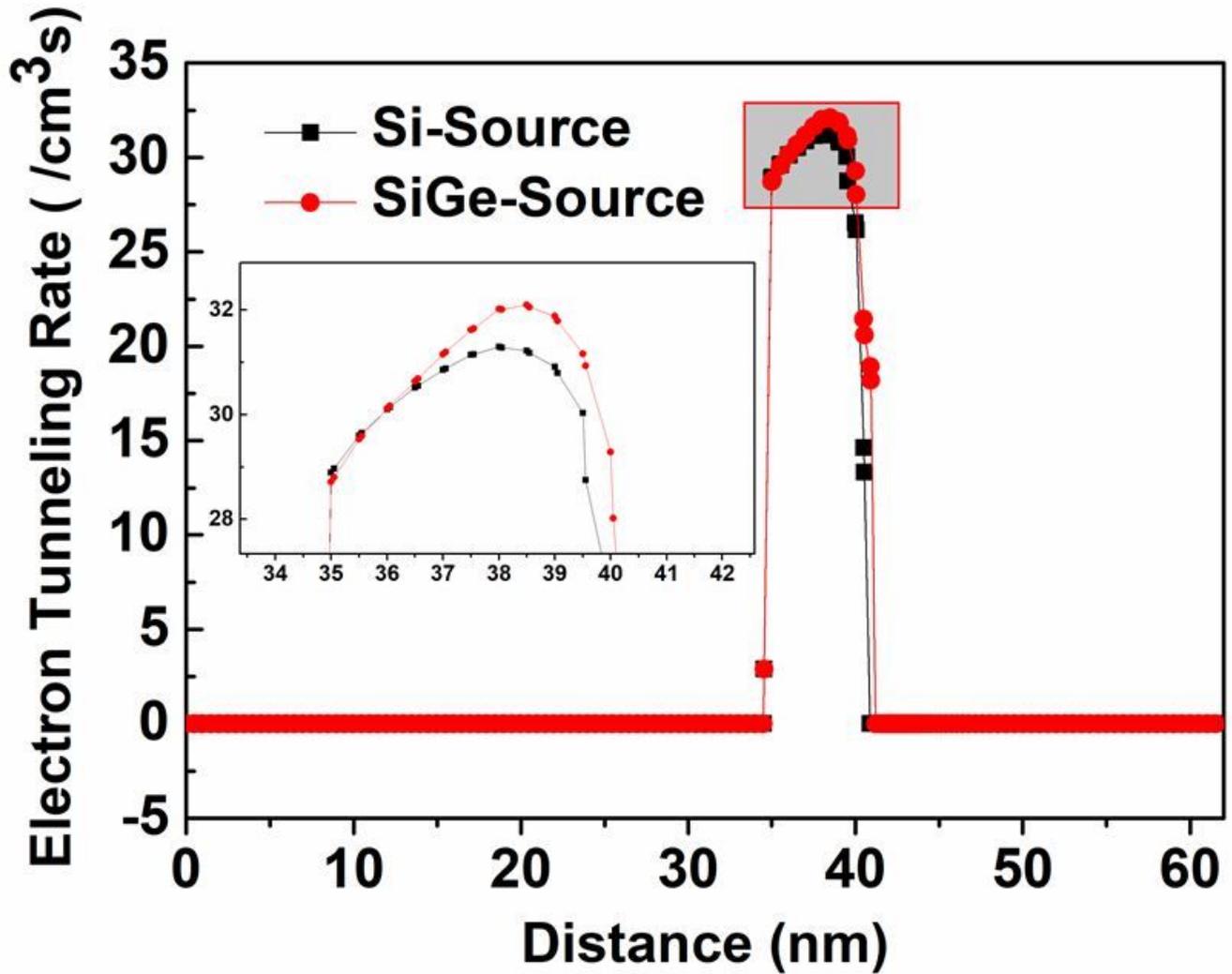


Figure 4

BTBT rate of DL-DG-TFET with Si_{0.5}Ge_{0.5} source and Si source at VGS = 1 V and VDS = 1 V.

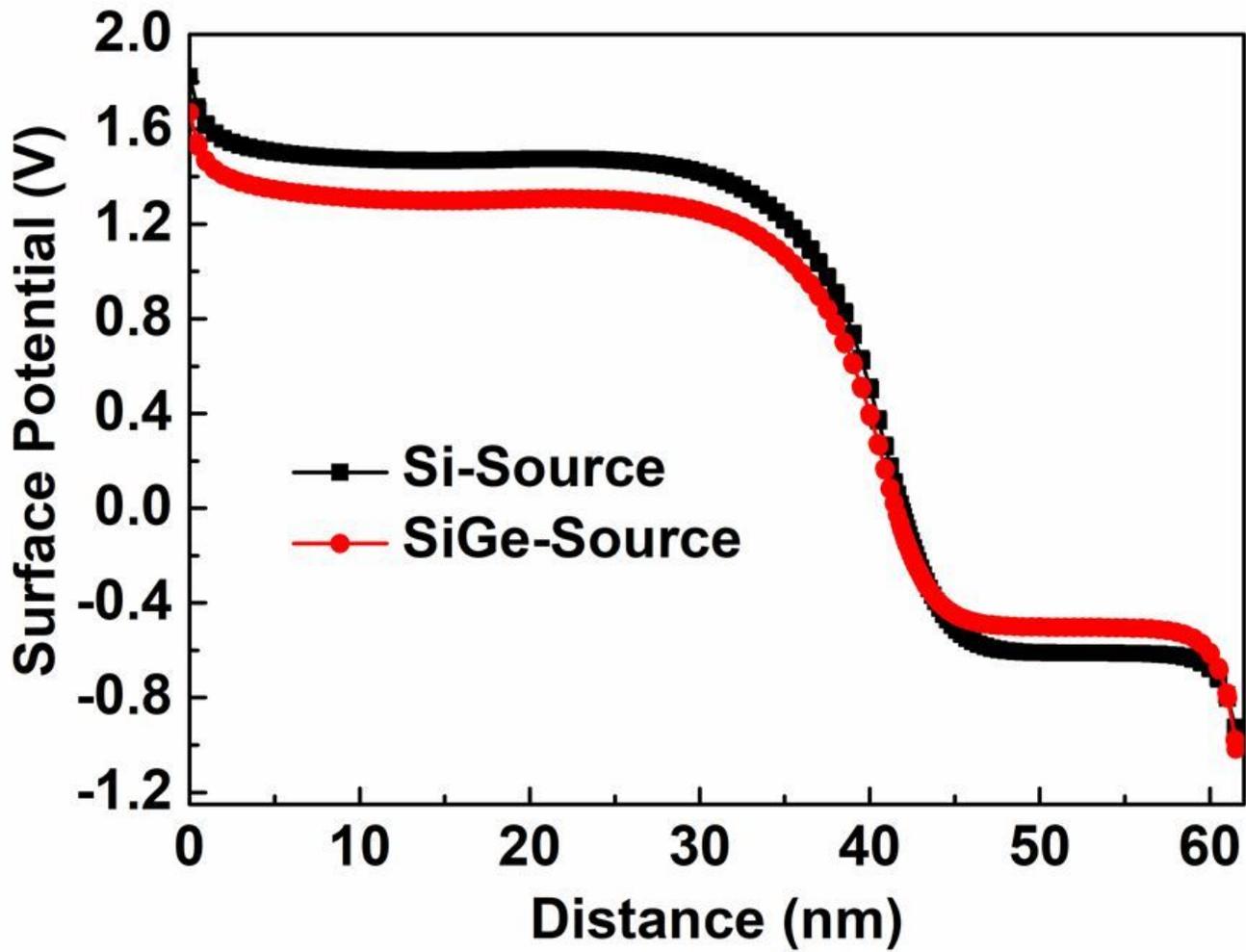


Figure 5

Surface potential variation of DL-DG-TFET with Si_{0.5}Ge_{0.5} source and Si source at VGS = 1 V and VDS = 1 V.

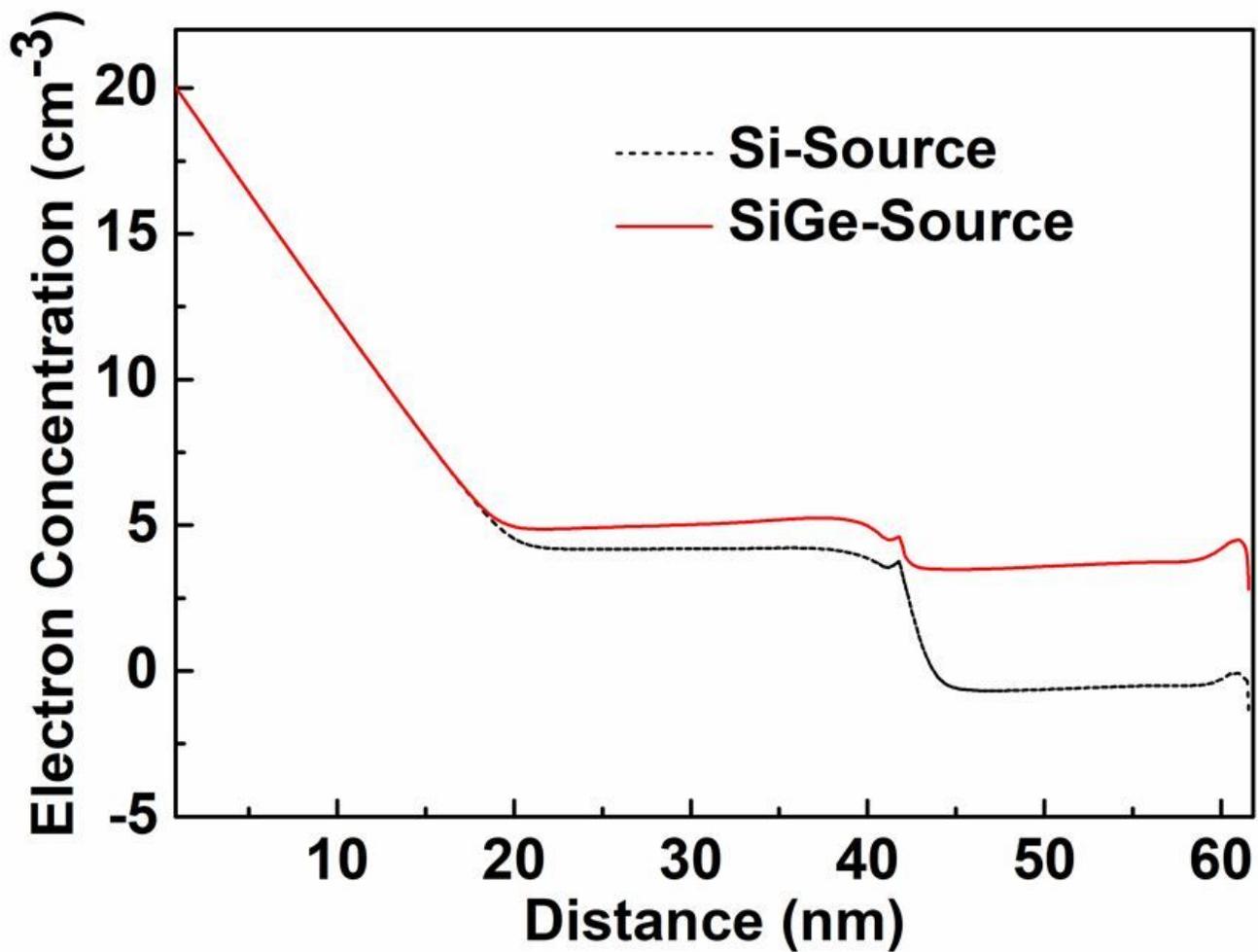


Figure 6

Electron concentration variation of DL-DG-TFET with Si_{0.5}Ge_{0.5} source and Si source at V_{GS} = 0 V and V_{DS} = 1

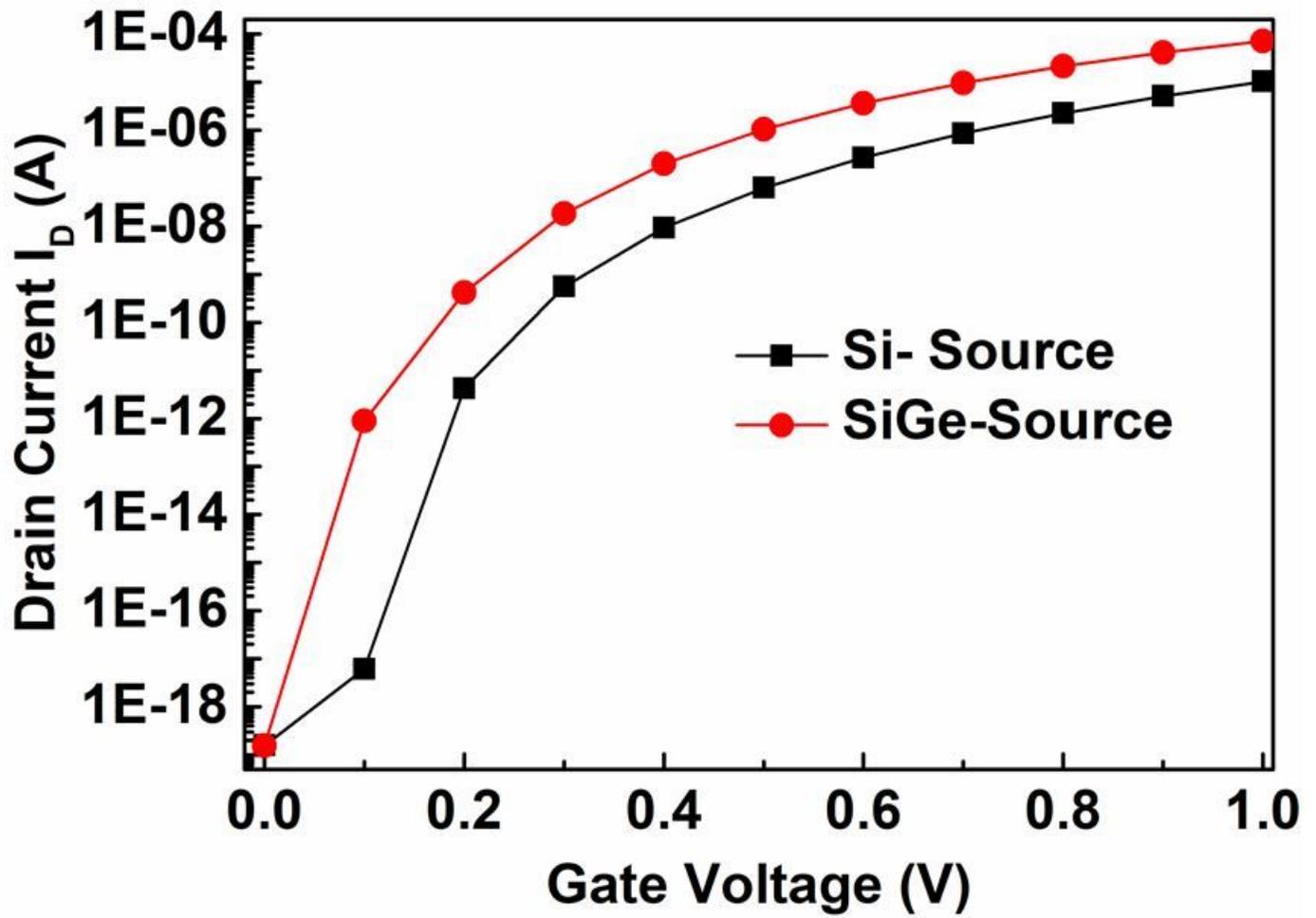


Figure 7

I_D - V_{GS} variation of DL-DG-TFET with Si_{0.5}Ge_{0.5} source and Si source at $V_{DS} = 1$ V.

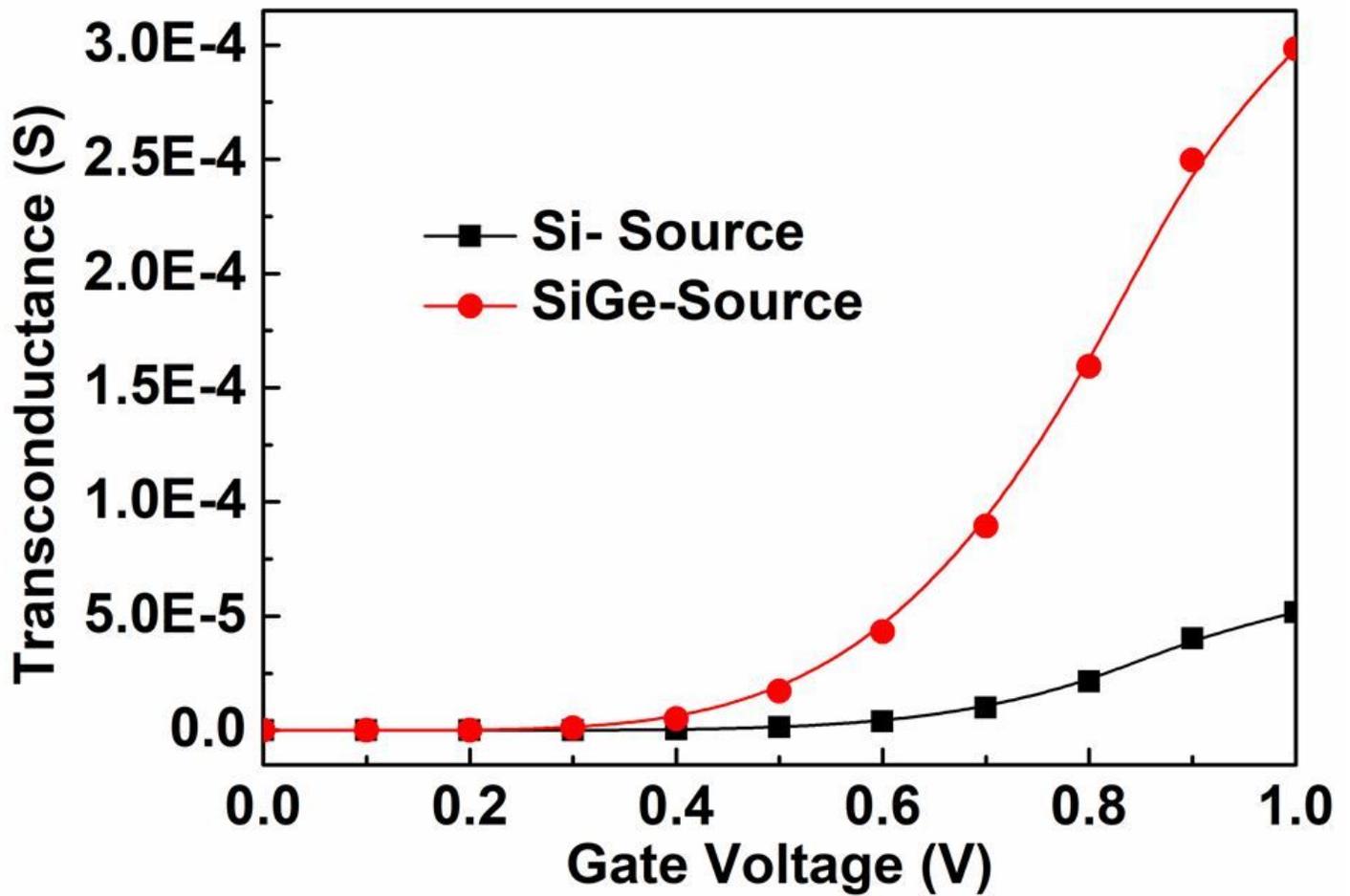


Figure 8

Transconductance variation of DL-DG-TFET with Si_{0.5}Ge_{0.5} source and Si source at V_{DS} = 1 V.

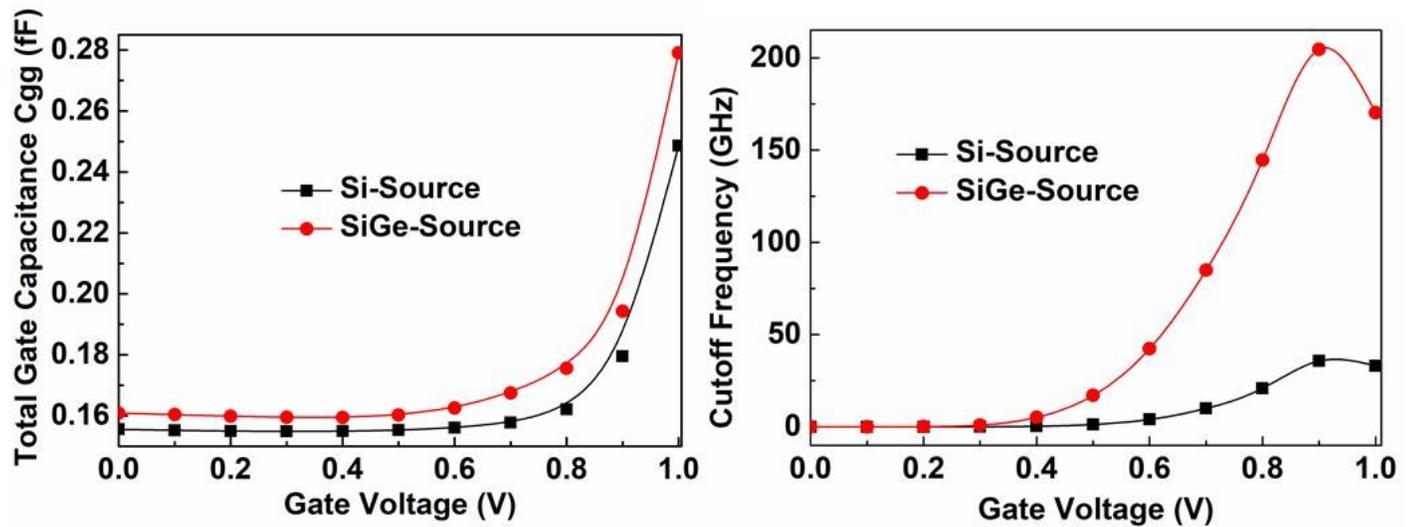


Figure 9

Comparison of DL-DG-TFET with Si_{0.5}Ge_{0.5} source and Si source in terms of (a) Total gate capacitance, and (b) Cut-off frequency.

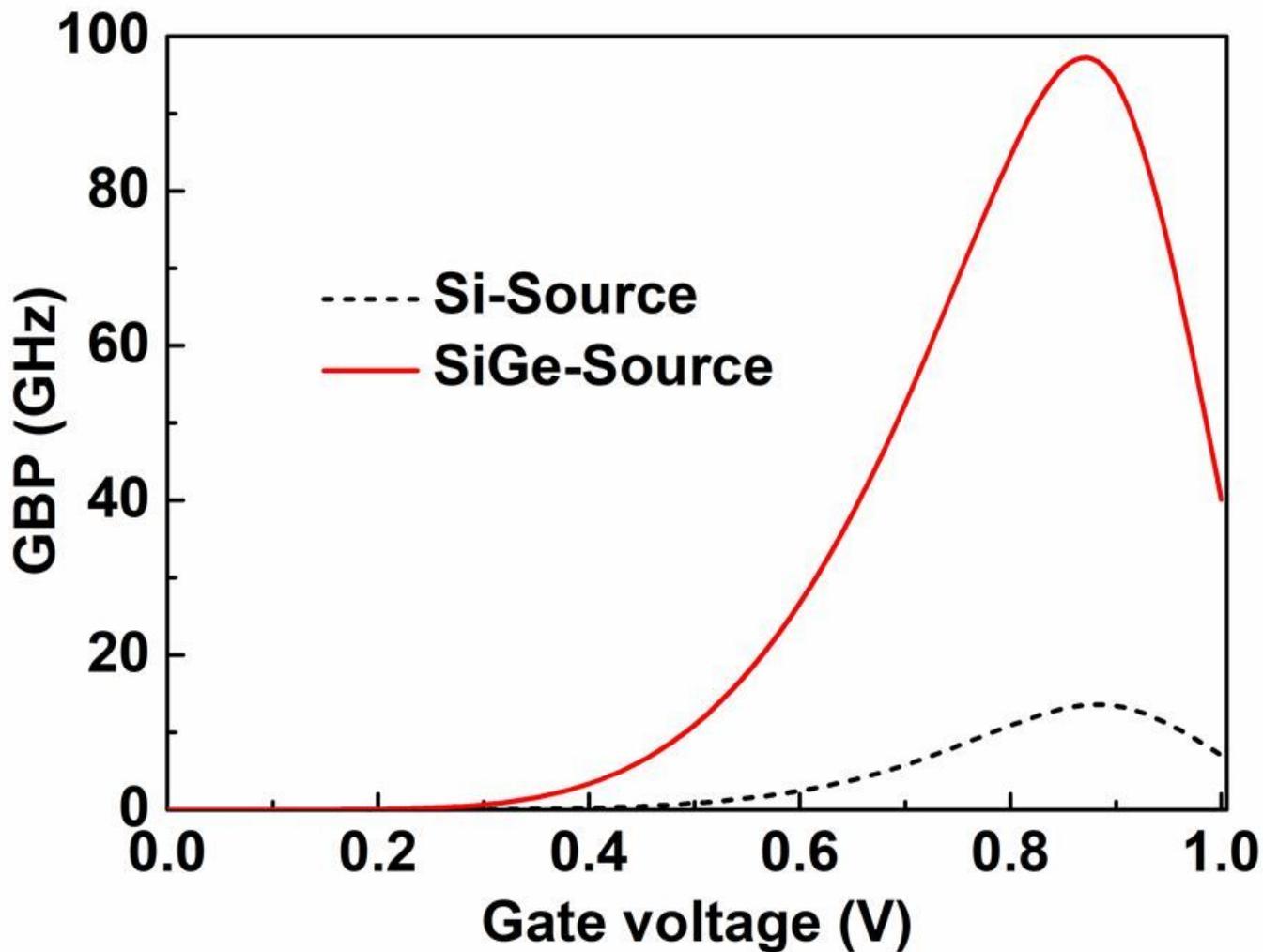


Figure 10

GBP variation of DL-DG-TFET with Si_{0.5}Ge_{0.5} source and Si source.

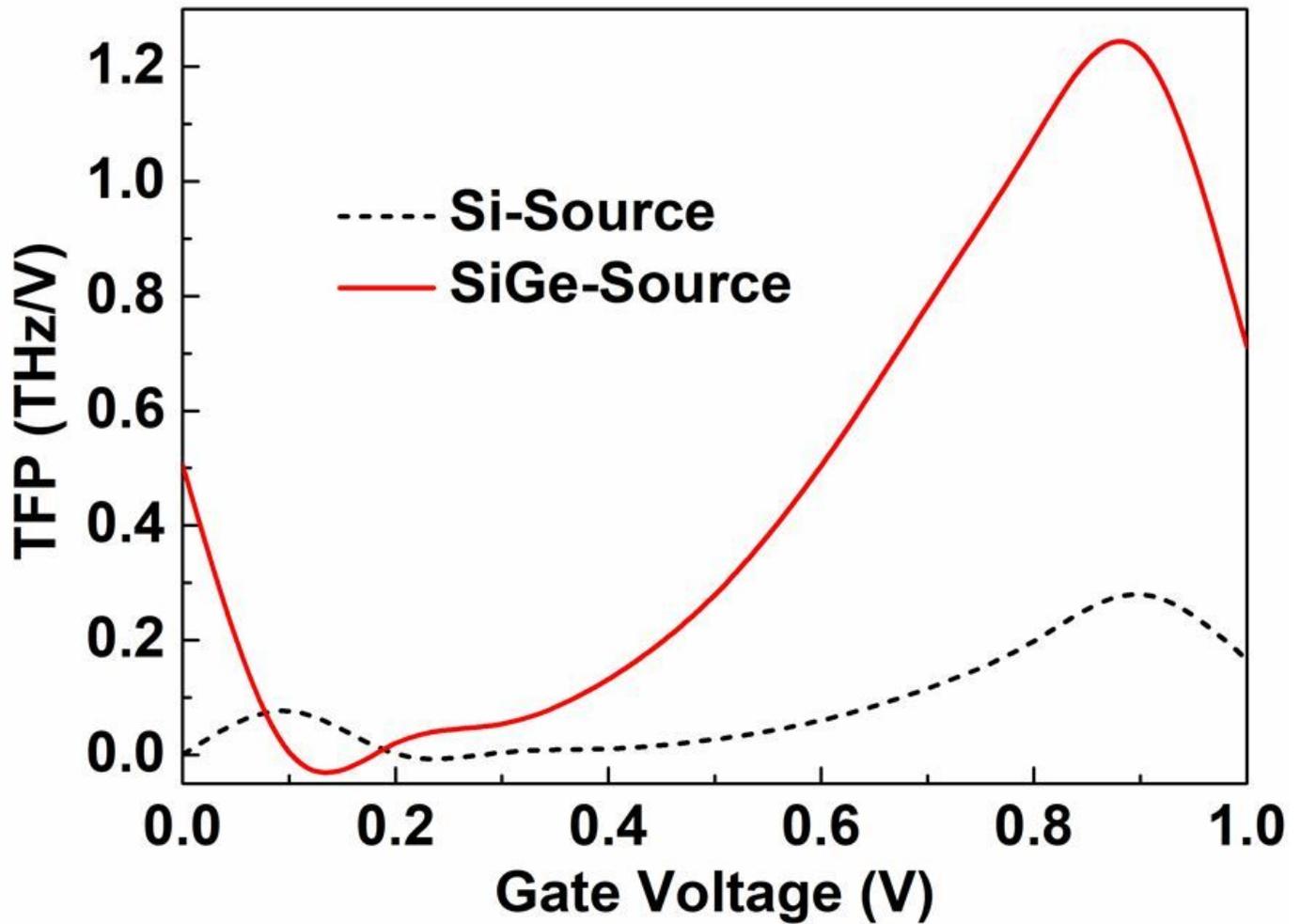


Figure 11

TFP variation of DL-DG-TFET with Si_{0.5}Ge_{0.5} source and Si source.

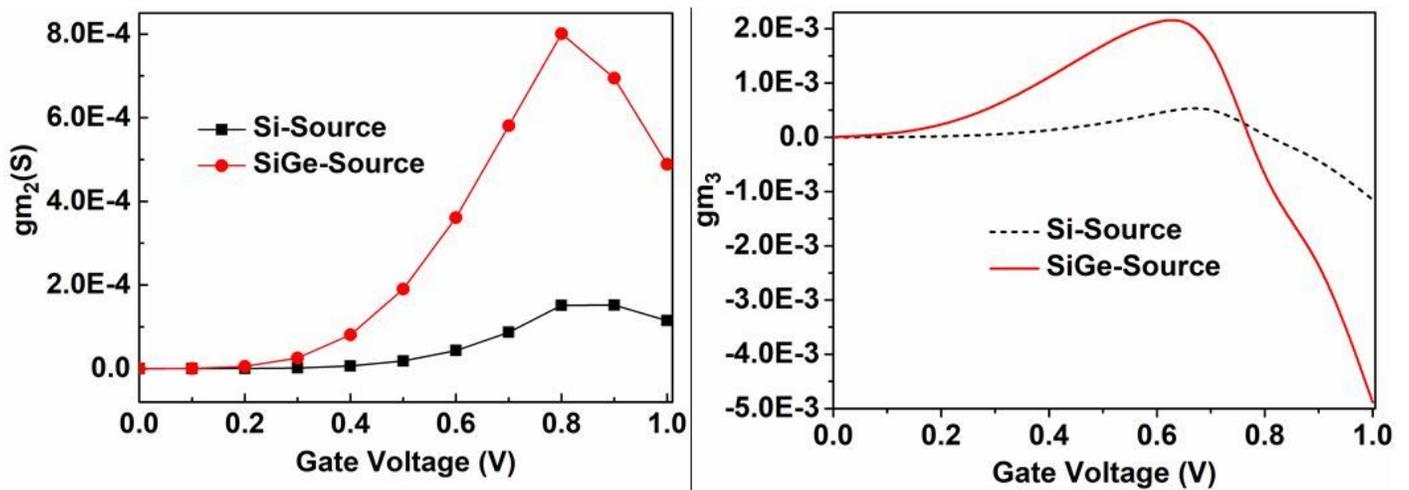


Figure 12

Comparison of DL-DG-TFET with Si_{0.5}Ge_{0.5} source and Si source in terms of (a) gm₂, and (b) gm₃.

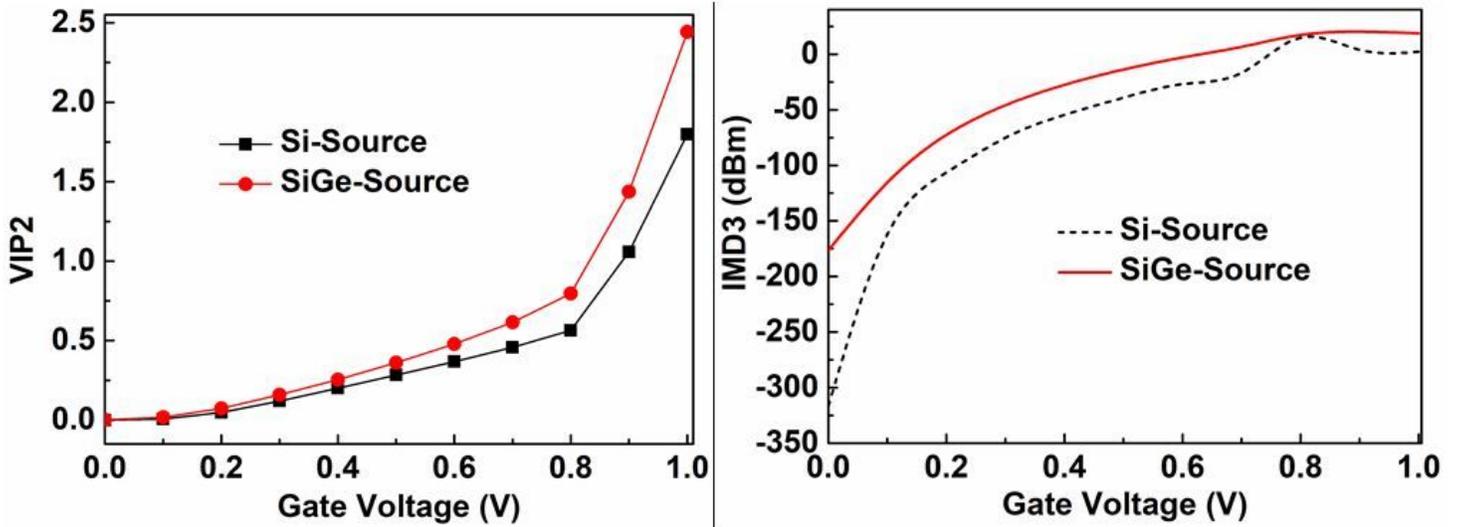
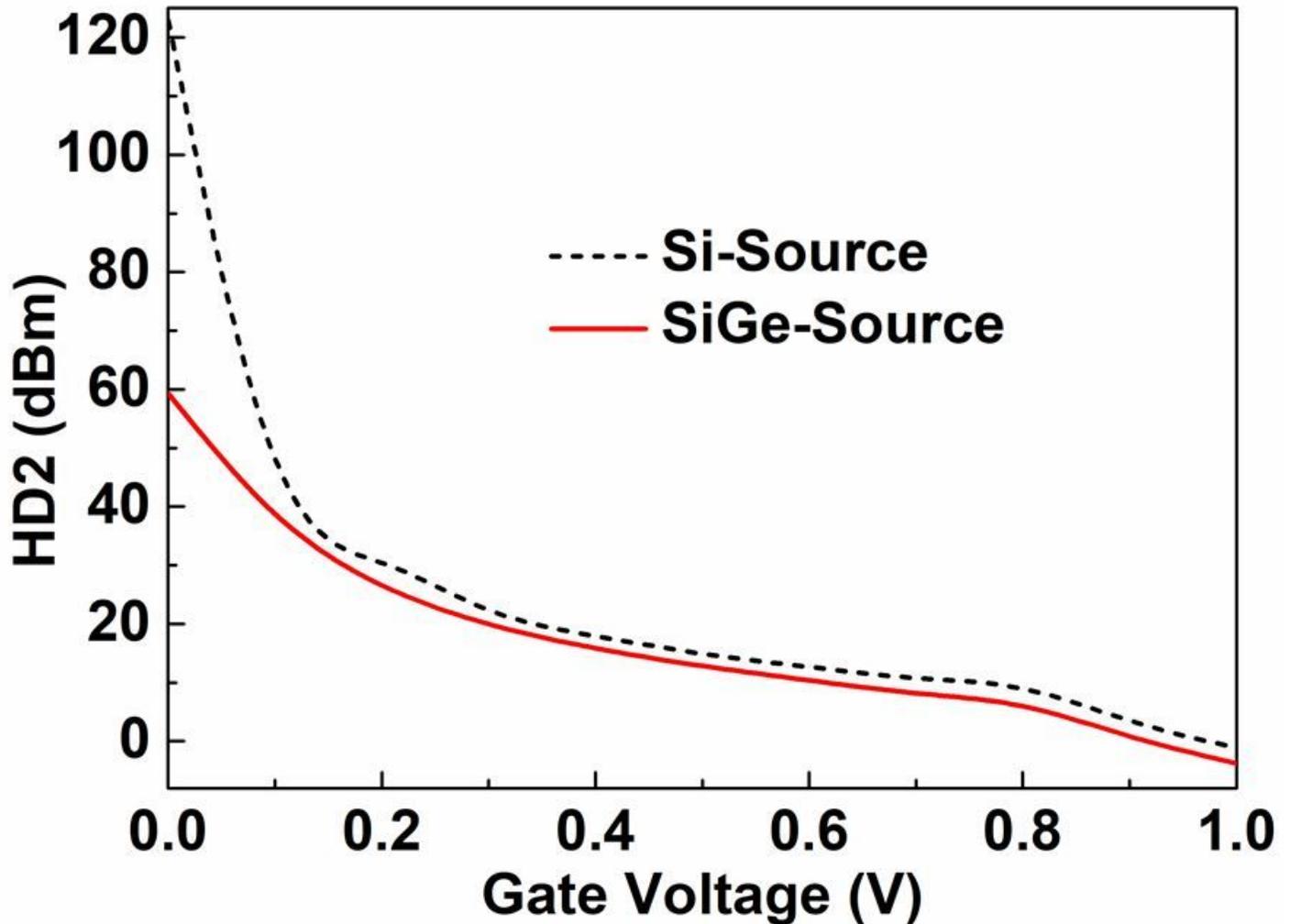


Figure 13

Comparison of DL-DG-TFET with Si_{0.5}Ge_{0.5} source and Si source in terms of (a) VIP₂, and (b) IMD₃.



HD2 variation of DL-DG-TFET with Si_{0.5}Ge_{0.5} source and Si source