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Triple Metal Surrounding Gate Junctionless Tunnel FET based 6T SRAM design for Low Leakage Memory System

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Abstract—The promising capability of Triple Material Surrounding Gate Junctionless Tunnel FET (TMSG – JL – TFET) based 6T SRAM structure is demonstrated by employing Germanium (Ge) and High-K gate dielectric material. The high – K insulation guarantees the proposed device to be used in low leakage memory systems. The corresponding analytical model is developed to extract various device parameters such as surface potential, electric field and threshold voltage. The results yield minimization of hot carrier effects at the drain end, when compared to conventional Silicon (Si) based tunnel FETs (TFETs). Further, the ambipolar characteristics of the proposed device is explored and 6T Ge – TMS – SG – JL – TFET based SRAM design is proposed. The results are compared with CMOS based SRAM and the analytical model presented is validated using 3D-TCAD ATLAS simulation, which ensures the accuracy and exactness of the developed model.

Keywords: Germanium; Junctionless; SRAM; Delay Analysis; Standby leakage power.

1. Introduction

The intense development of channel engineering and manufacturing technology to obtain better efficiency has successfully driven continued device scaling. As the dimensions of the semiconductor devices are continually shrinking, control gate loses its sway over the channel, leading to diverse Short Channel Effects (SCEs). In order to further enhance the device efficiency in terms of reduced SCEs [1], engineers in the field of nanotechnology have been researching and looking for new device architectures. In this concern, Junctionless FETs (JLFETs) [2 - 4] have been the most influential device in rendering decreased SCEs, high ON – OFF current ratio and almost ideal subthreshold slope ($SS \sim 60$ mV/dec).

In addition to JLFETs, the subthreshold swing of the Tunnel FET (TFET) is less than 60mV/dec, which is the substantial limit of the MOSFET [5]. On top of it, Junctionless Tunnel FETs [6, 7] and the concept of gate material [8 - 11] engineering is another tangible solution to reduce the SCEs. In this process of improving the reliability of device, Germanium (Ge) based TFETs [12 - 15] with enhanced oxide interface can serve as a supreme solution for minimizing the control gate leakage current.

Silicon (Si) based Tunnel FETs with silicon dioxide, turned out to perform with poor electrostatics and deserved a huge gate to source voltage for tunneling FET's to operate. Above this, because of the outpouring of electrons through the poor insulation layer, the leakage current will reach a high value, exceeding 1 A/cm² at 1V [16]. The analytical model for junctionless DMDG FET [9] is proposed, but the aggregate advantages of Ge, High-K gate dielectric [17 - 19] (Titanium Oxide - TiO₂), and triple material gate work function engineering has not been explored in short channel (12nm) junctionless surrounding gate tunnel FETs [20 - 22]. Also, from the application perspective the design of SRAM memory cell has been explored in the literature using various conventional FETs. Here, to extend the proposed Ge-TMSG-JLTFET for low power applications, design of 6T SRAM has been explored [23 - 25]. Therefore, the foremost objective of developing a 2-D mathematical model for Triple Material Surrounding Gate (TMSG) Junctionless TFET (JLTFET) with Germanium (Ge) and High-K gate dielectric materials is of great interest.

In view of all the above-mentioned details, an analytical model for junctionless surrounding gate TFETs with Ge, high-K gate dielectric and gate metal engineering has been demonstrated. In order to observe the short channel effects, the surface potential and electric field are critical components and can be estimated by solving the 2-D Poisson's equation by parabolic approximation. The design of 6T SRAM using Ge-TMSG-JLTFET has been explored to analyze the subthreshold leakage power / memory cell for utilizing in low power applications. The extracted results from the mathematical approach are checked with the results of JLTFETs based on traditional Silicon technology. Furthermore, the findings of the analytical model, with TCAD results, are also verified.

2. Mathematical Modeling

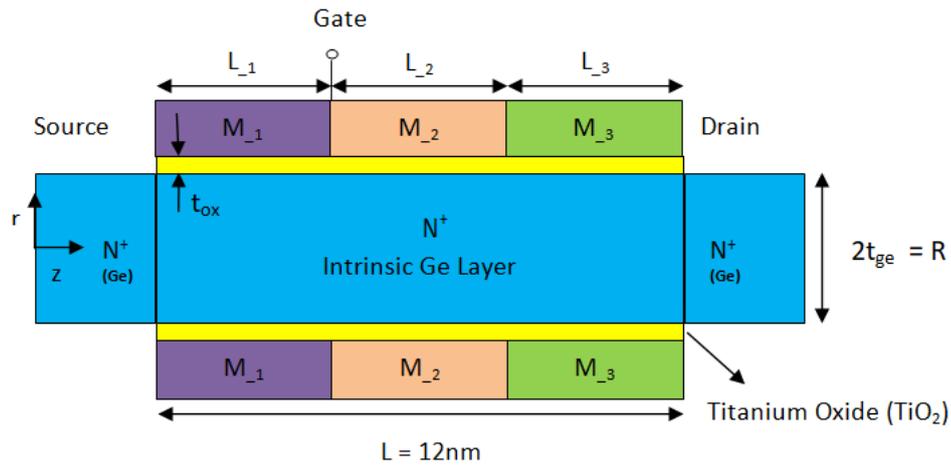
The schematic, 3D and mesh profile view of the proposed device (Ge-TM-SG-JL-TFET) is presented in Fig.1. The gate electrode is made of three M_{-1} , M_{-2} and M_{-3} materials with their gate lengths to be L_{-1} , L_{-2} and L_{-3} . The total gate length ($L = 12\text{nm}$) is expressed as $L = L_{-1} + L_{-2} + L_{-3}$.

Tunneling gate metals M_{-1} , M_{-2} and M_{-3} have work functions of $\phi_{M_{-1}} = 4.8$ eV (Au), $\phi_{M_{-2}} = 4.6$ eV (Mo), $\phi_{M_{-3}} = 4.4$ eV (Ti). The three different materials for the gate metal are chosen in such a way that $\phi_{M_{-1}} > \phi_{M_{-2}} > \phi_{M_{-3}}$. There is a 12nm germanium channel in the proposed model, which is strongly doped with n – type material of 10^{19}cm^{-3} . The regions of source and drain are uniformly doped on the germanium channel.

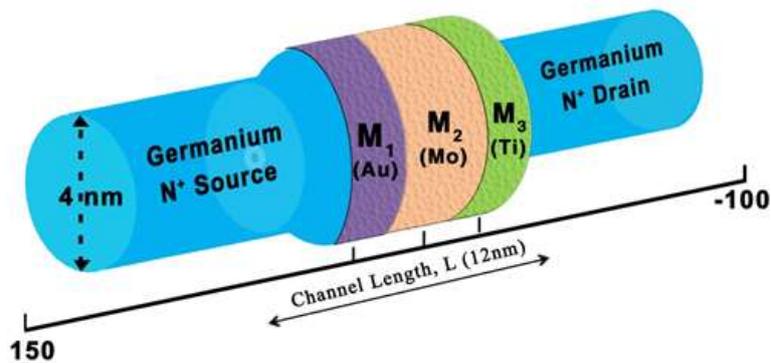
The potential distribution in the channel is expressed using 2-D Poisson's equation,

$$\frac{1}{r} \frac{\partial}{\partial r} \left(r \frac{\partial \phi_i(r, z)}{\partial r} \right) + \frac{\partial^2 \phi_i(r, z)}{\partial z^2} = -\frac{qN_d}{\epsilon_{Ge}}; i = 1, 2, 3; \quad (1)$$

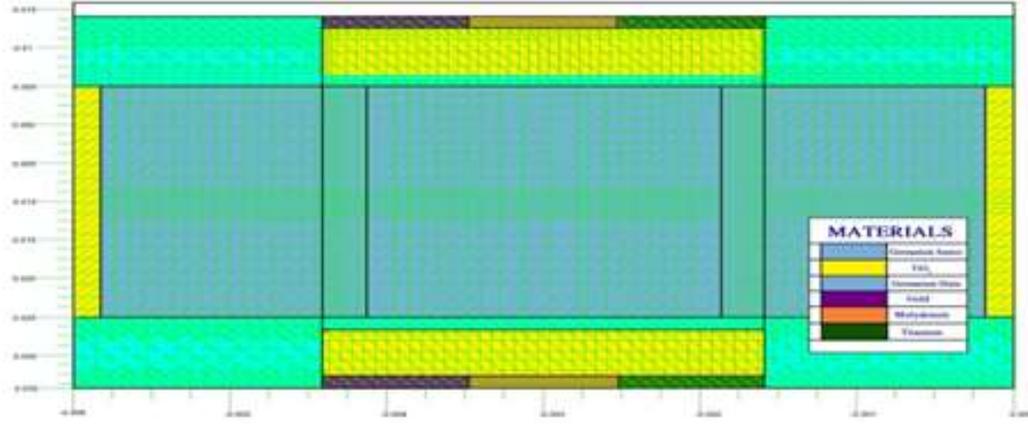
where $\phi(r, z)$ - 2-D profile of the potential, q - charge of an electron, N_d - uniform channel - doping concentration and ϵ_{Ge} - germanium permittivity.



(a)



(b)



(c)

Fig.1.(a) 12nm Ge based Triple Material - Surrounding Gate - Junctionless - Tunnel FET (Ge-TM-SG-JL-TFET)– Cross sectional view (b) 3D ATLAS TCAD representation of the proposed device (c) Simulated mesh profile of Germanium based TM-SG-JL-TFET by Silvaco ATLAS.

A straightforward parabolic function is utilized to align the potential in the vertical direction, which is shown as below [26 - 27],

$$\phi(r, z) = Y_1(z) + Y_2(z)r + Y_3(z)r^2 \quad (2)$$

where $Y_1(z)$, $Y_2(z)$ and $Y_3(z)$ are approximate functions of z only.

The Poisson's equation is solved independently using the boundary conditions listed below;

(a) The surface potential as a function of z is denoted as;

$$\phi(r = 0, z) = Y_1(z) = \phi_s(z) \quad (3)$$

(b) At the center of the germanium pillar, the electric field is zero.

$$\left. \frac{\partial \phi(r, z)}{\partial z} \right|_{r=0} = 0 \quad (4)$$

(c) At the interface of the gate and gate dielectric layer, the electric field is continuous.

$$\left. \frac{\partial \phi(r, z)}{\partial z} \right|_{r=2*t_{ge}} = \frac{\epsilon_{ox}}{\epsilon_{Ge}(2*t_{ge})} \left[\frac{\psi_G - \phi_s(z)}{\ln \left(1 + \frac{t_{ox}}{(2*t_{ge})} \right)} \right] \quad (5)$$

(d) The source and drain end potentials are;

$$\phi(r = 0, z = 0) = V_{_bip} \quad (6)$$

$$\phi(r = (2 * t_{ge}), z = L = L_{-1} + L_{-2} + L_{-3}) = V_{-bip} + V_{ds} \quad (7)$$

$$\text{where } \psi_G = V_{G-t-s} - \phi_{M_{-i}} + \chi_{ea} + \frac{E_{GB}}{2}; i = 1, 2, 3 \quad (8)$$

V_{G-t-s} -Gate to source bias,

E_{GB} -Energy band gap of germanium,

χ_{ea} -Electron affinity of germanium,

$\phi_{M_{-i}}$ -Gate metal work functions and V_{bip} - built-in potential.

For the three gate metal regions, the flat-band voltages are:

$$V_{FLB_1} = \phi_{M_{-1}} - \phi_{Ge}; V_{FLB_2} = \phi_{M_{-2}} - \phi_{Ge}; V_{FLB_3} = \phi_{M_{-3}} - \phi_{Ge} \quad (9)$$

where $\phi_{M_{-1}}$, $\phi_{M_{-2}}$ and $\phi_{M_{-3}}$ are the work functions of individual gate materials and ϕ_{Ge} is the germanium work function.

2.1 Surface Potential

In this structure, as the control gate metal has three regions, the potential underneath each region are as follows;

$$\phi_{-1}(r, z) = Y_{11}(z) + Y_{12}(z)r + Y_{13}(z)r^2, \text{ for } 0 \leq z \leq L_{-1} \quad (10)$$

$$\phi_{-2}(r, z) = Y_{21}(z) + Y_{22}(z)r + Y_{23}(z)r^2, \text{ for } L_{-1} \leq z \leq L_{-1} + L_{-2} \quad (11)$$

$$\phi_{-3}(r, z) = Y_{31}(z) + Y_{32}(z)r + Y_{33}(z)r^2, \text{ for } L_{-1} + L_{-2} \leq z \leq L_{-1} + L_{-2} + L_{-3} \quad (12)$$

where, $Y_1(z)$, $Y_2(z)$ and $Y_3(z)$ are found using the boundary conditions (3 -5).

On substitution of these above functions in (2), we obtain;

$$\phi(r, z) = \phi_s(z) + \frac{\epsilon_{ox}}{4\epsilon_{Ge} * t_{ge}^2} \left[\frac{\psi_G - \phi_s(z)}{\ln \left(1 + \frac{t_{ox}}{(2 * t_{ge})} \right)} \right] \quad (13)$$

Substituting (13) in the 2-D Poisson's equation, the potential underneath each control gate-metal region is expressed as;

$$\phi_{s_{-1}}(z) = C_1 e^{\mathcal{G}z} + D_1 e^{-\mathcal{G}z} - \frac{\phi_{g1}}{\mathcal{G}^2}; \text{ for } 0 \leq z \leq L_{-1} \quad (14)$$

$$\phi_{s_{-2}}(z) = C_2 e^{\mathcal{G}(z-L_{-1})} + D_2 e^{-\mathcal{G}(z-L_{-1})} - \frac{\phi_{g2}}{\mathcal{G}^2}; \text{ for } L_{-1} \leq z \leq L_{-1} + L_{-2} \quad (15)$$

$$\phi_{s_{-3}}(z) = C_3 e^{\mathcal{G}(z-(L_{-1}+L_{-2}))} + D_3 e^{-\mathcal{G}(z-(L_{-1}+L_{-2}))} - \frac{\phi_{g3}}{\mathcal{G}^2}; \text{ for } L_{-1} + L_{-2} \leq z \leq L_{-1} + L_{-2} + L_{-3} \quad (16)$$

where, C_i and D_i used in (16) are as follows;

$$C_i = \frac{\left[V_{-bip}(1 - e^{-\mathcal{G}L_{-i}}) + \frac{\phi_{g_i}}{\mathcal{G}^2}(1 - e^{-\mathcal{G}L_{-i}}) + V_{ds} \right]}{(e^{\mathcal{G}L_{-i}} - e^{-\mathcal{G}L_{-i}})}; i = 1, 2, 3$$

$$D_i = \frac{\left[V_{-bip}(e^{\mathcal{G}L_{-i}} - 1) + \frac{\phi_{g_i}}{\mathcal{G}^2}(e^{\mathcal{G}L_{-i}} - 1) - V_{ds} \right]}{(e^{\mathcal{G}L_{-i}} - e^{-\mathcal{G}L_{-i}})}; i = 1, 2, 3 \quad (17)$$

2.2 Lateral & Vertical Electric Field

The electric - field at the drain end intruding into the channel is one of the most remarkable reasons for devices to degrade at shorter channel lengths of 12nm. This is supposed to have an adverse effect on the performance of the device. Hence, estimation of electric - field components becomes essential and is found by a simple differentiation of surface potential. Components of the electric - field $LE_i(z)$, lateral electric - field and $VE_r(z)$, vertical electric - field are represented as:

$$LE_i(z) = \left[\frac{\mathcal{G}}{\text{Sinh}(\mathcal{G}L_{-i})} \right] \times \left[\begin{array}{l} V_{-bip} [\text{Cosh}(\mathcal{G}z) - \text{Cosh}(\mathcal{G}(z - L_{-i}))] \\ + \frac{\phi_{g_i}}{\mathcal{G}^2} [\text{Cosh}(\mathcal{G}z) - \text{Cosh}(\mathcal{G}(z - L_{-i}))] \\ + V_{ds} [\text{Cosh}(\mathcal{G}z)] \end{array} \right]; i = 1, 2, 3 \quad (18)$$

$$VE_r = \frac{\epsilon_{ox}}{\epsilon_{Ge}(2^* t_{ge})} \left[\frac{\psi_G - \phi_s(z)}{\ln \left(1 + \frac{t_{ox}}{(2^* t_{ge})} \right)} \right] \quad (19)$$

2.3 Threshold Voltage

As the electric field approaches zero, it indicates that there is a minimal electrostatic potential. Also, when this minimum potential beneath the gate metal region M_{-1} approaches zero, the value of threshold - voltage may be set equivalent to the value of control - gate bias. The mathematical equations are expressed below;

$$\left. \frac{d\phi_{S-1}(z)}{dz} \right|_{z=z_{\min}} = 0 \quad (20)$$

$$\phi_S(z_{\min}) = 2\sqrt{C_1 D_1} - \frac{\phi_g}{g^2} \quad (21)$$

where,

$$\phi_g = - \left[\frac{qN_d}{\epsilon_{Ge}} + g^2 \psi_G \right],$$

$$g^2 = \frac{\epsilon_{ox}}{(2 * t_{ge}^2) * \epsilon_{Ge} \ln \left(1 + \frac{t_{ox}}{(2 * t_{ge})} \right)} \quad \text{and} \quad (22)$$

$$z_{\min} = \frac{1}{2g} \ln \left(\frac{D_1}{C_1} \right)$$

Incorporating this potential minimum underneath control gate - metal region M_{-1} , as two times the bulk - potential and equating $V_{G-t-S} = V_{\text{threshold}}$, the final expression for threshold - voltage is represented as,

$$V_{\text{threshold}} = 2\phi_{\text{Bulk}} - 2\sqrt{C_1 D_1} - \frac{qN_d}{\epsilon_{Ge} g^2} + \phi_{M_{-1}} - \chi_{ea} - \frac{E_{GB}}{2} \quad (23)$$

3. Results and Discussions

The complete mathematical model presented is verified against 3-D TCAD device simulator. Shockley-Read-Hall (SRH) recombination model combined with Auger recombination model is incorporated to model carrier concentration. In addition to this, to analyze the transport mechanism of the carriers in device simulation, model of Drift Diffusion (DD) has also been included. The total channel length of the device is considered to be 12nm. The main device parameters such as thickness of the germanium channel (t_{ge}) and dielectric layer thickness (t_{ox}) are predefined to be 2nm and 1nm. Table-I describes the specification of design parameters used for simulation purpose.

Table I List of Design Parameters used for Ge-TM-SG-JL-TFET used during numerical simulation

Parameters	Symbol	Value
Channel Length	L	12 nm
Uniform Channel Doping (n-type)	$N_{D,Ge}$	$1 \times 10^{19} \text{ cm}^{-3}$
Germanium body thickness	t_{Ge}	8 nm
Tunneling gate Work function	ϕ_{M-1}	4.8 eV
Control gate Work function	ϕ_{M-2}	4.6eV
Auxiliary gate Work function	ϕ_{M-3}	4.4 eV
Radius of Germanium	$R(t_{Ge}/2)$	4 nm
Dielectric oxide thickness	$t_{\text{effox,SiO}_2/\text{HfO}_2}$	2 nm and 1 nm

Fig.2 indicates the surface potential contrast of both Ge-TMSG-JLTFET and Si-TMSG-JLTFET. The proposed Ge based TMSG-JLTFET has incorporated the effect of high-K material and renders superior value of surface potential compared to Si based device with silicon dioxide as their gate - oxide material.

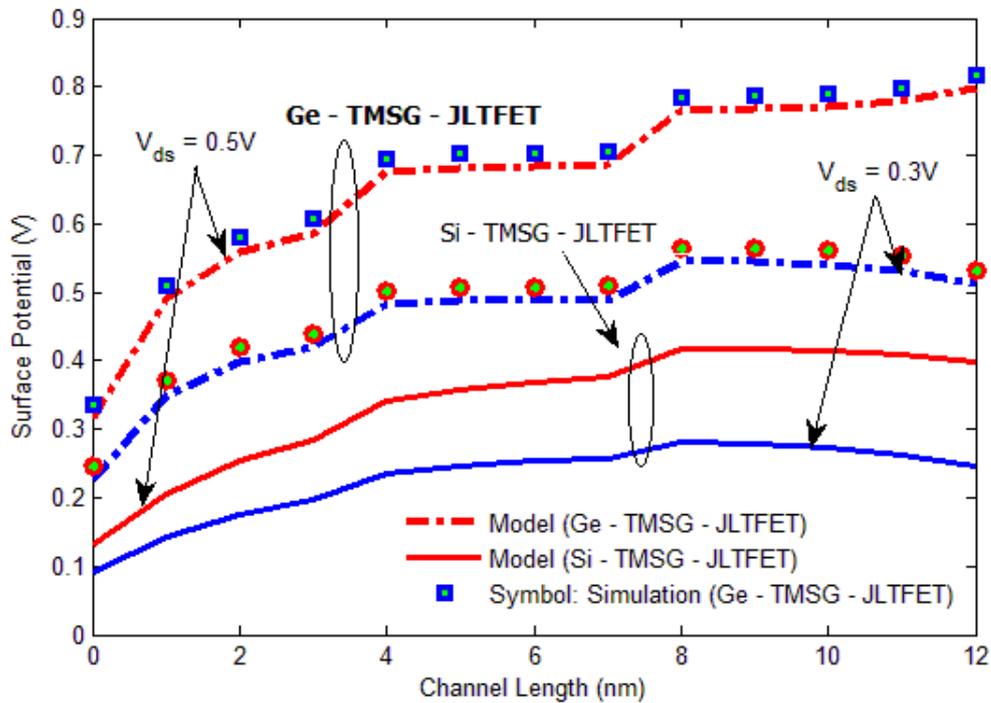


Fig.2. Surface potential distribution of Ge-TM-SG-JL-TFET and Si-TM-SG-JL-TFET with respect to different values of $V_{ds}=0.3V$ and $V_{ds}=0.5V$.

The surface potential distribution noticed in Fig.3 in the daintily doped drain tends to increase as the length of the channel increases. But it is obvious that the potential is considerably less for thinner $t_{ox}=1nm$ oxide thickness, relative to $t_{ox}=2nm$. In addition to this, a significant shift in potential is ascertained at the interface of the three gate metals due to varying work functions in the device. This transition in step is critically important for increasing the speed of the carriers and also for enhancing the efficiency of carrier transport.

Fig.4 depicts the surface potential trace of Ge-TMSG-JLTFET for distinct values of germanium thickness. It is clearly visible that, as the thickness of germanium decreases, the value of potential also decreases. This minimum potential shifts towards the source side, thus manifesting that applied gate bias has a high impact on the tunneling generation rate at the source end. The validity of the proposed analytical model is ascertained with TCAD results.

Fig.5 illustrates that lateral electric - field near tunneling junction (i.e. drain side) is condensed. It is also perceived that as drain-to-source voltage decreases, the value of lateral electric field is also reduced.

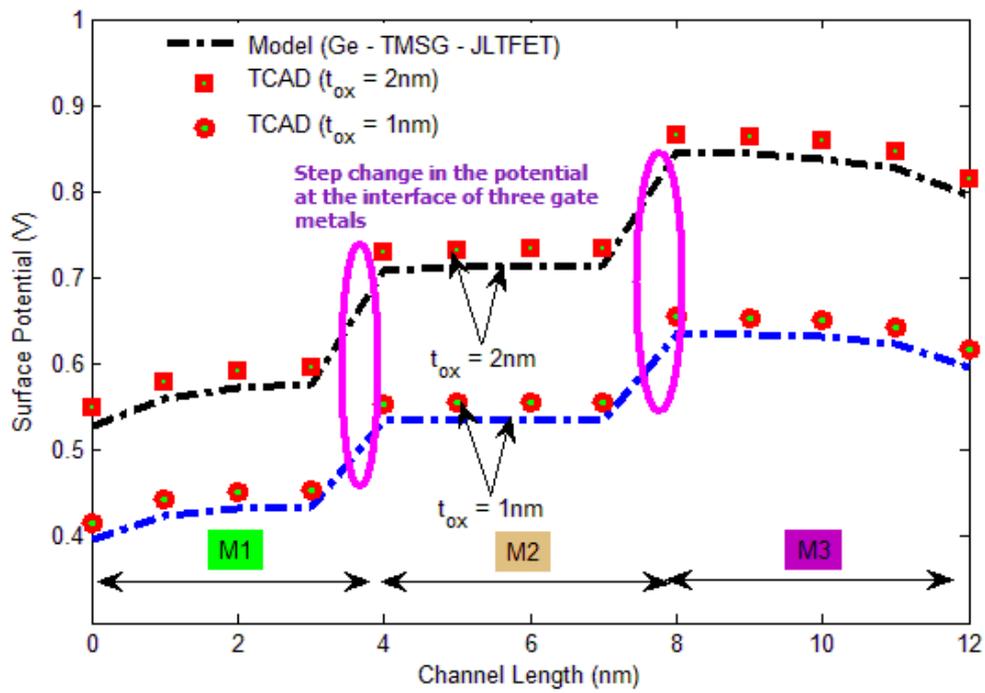


Fig.3. Surface potential profile of Ge-TM-SG-JL-TFET for values of oxide thickness, $t_{ox}=1\text{nm}$ and $t_{ox}=2\text{nm}$.

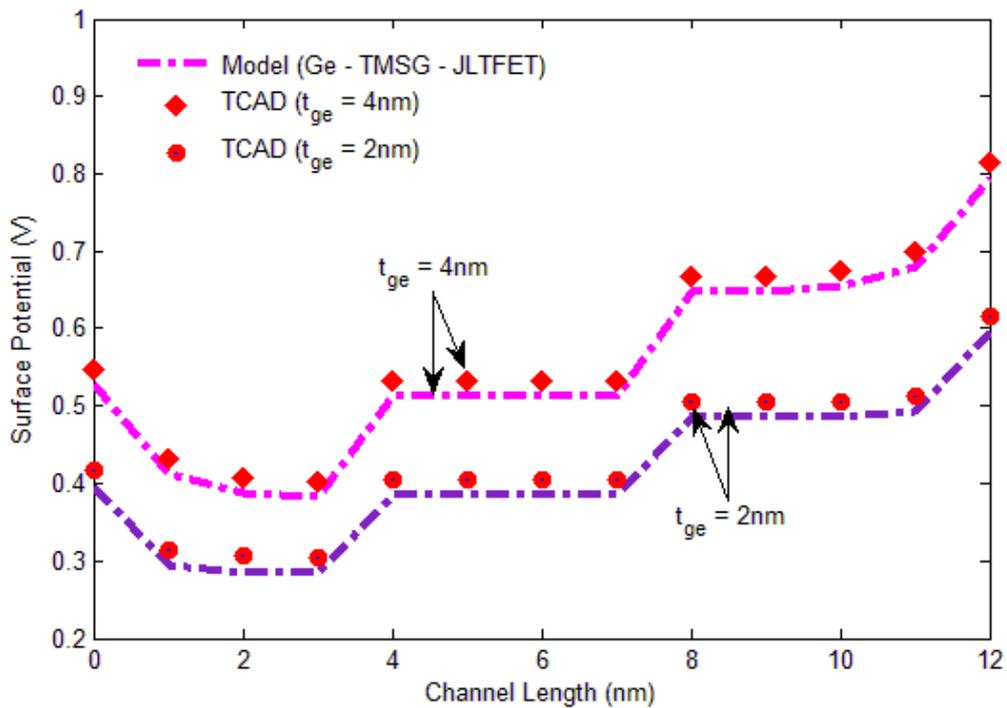


Fig.4. Surface potential profile of Ge-TM-SG-JL-TFET for distinct values of germanium thickness, $t_{ge}=2\text{nm}$ and $t_{ge}=4\text{nm}$.

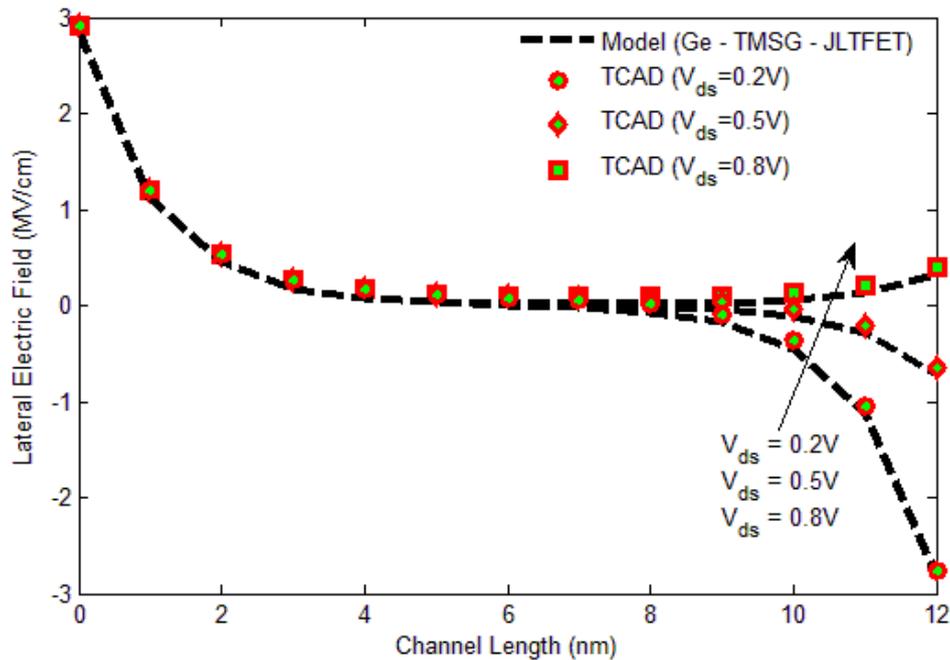


Fig.5.Lateral Electric Field distribution of Ge-TM-SG-JL-TFET for different values of $V_{ds}=0.2V$, $0.5V$ and $0.8V$.

Fig.6 outlines the distinction of lateral electric field between Ge-TMSG-JLTFET and Si-TMSG-JLTFET for distinct values of oxide thickness. Due to thinner oxide thickness ($t_{ox}=1nm$) and high-K dielectric material used (Titanium Oxide), the crest of the lateral electric - field is towards the source side. It is a clear notion that the Drain Induced Barrier Lowering (DIBL) is considerably reduced for Ge-TMSG-JLTFETs. But in case of Si-TMSG-JLTFET, a peak electric - field at the drain end may end up in constitution of extremely energetic and active “Hot Carriers”. These carriers can get lodged in the insulation region and root causes the device to just be weakened. Therefore, by shortening the thickness of the gate oxide layer, we can surmount the SCEs and strengthen the reliability.

The vertical electric field variance of Ge-TMSG-JLTFET is illustrated in Fig.7 with various values of $V_{ds}=0.3V$ and $0.5V$. The figure clearly demonstrates that a shift in the potential profile causes the electric - field lines at the intersection of three gate metals also to change. Independent gate metals are positioned so that the material has a lower work - function on the drain side than on the source side. The electrons near the source are then accelerated more strongly, leading to advancements in performance of the device. It is also inferred that the vertical electric field portion is minimal on the drain side with $V_{ds}= 0.3V$ and along the channel it becomes highly consistent. The model described here appears to match the data obtained from the TCAD simulation.

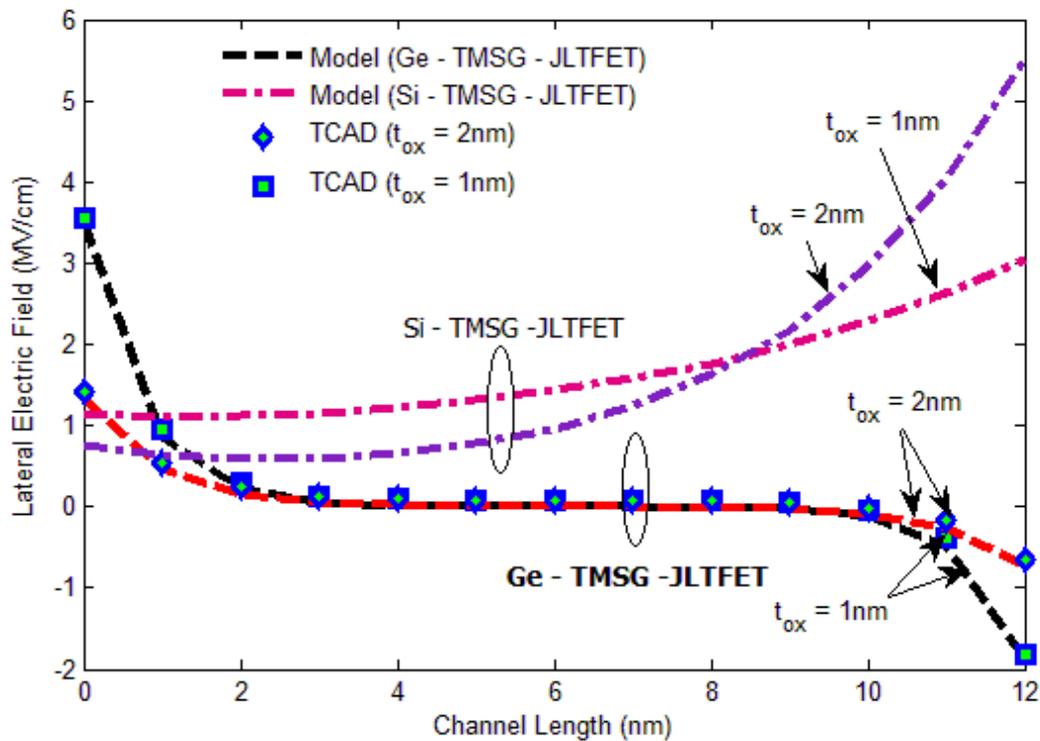


Fig.6. Variation of Lateral Electric Field of Ge-TM-SG-JL-TFET and Si-TM-SG-JL-TFET with respect to different values of oxide thickness, $t_{ox}=1\text{nm}$ and $t_{ox}=2\text{nm}$.

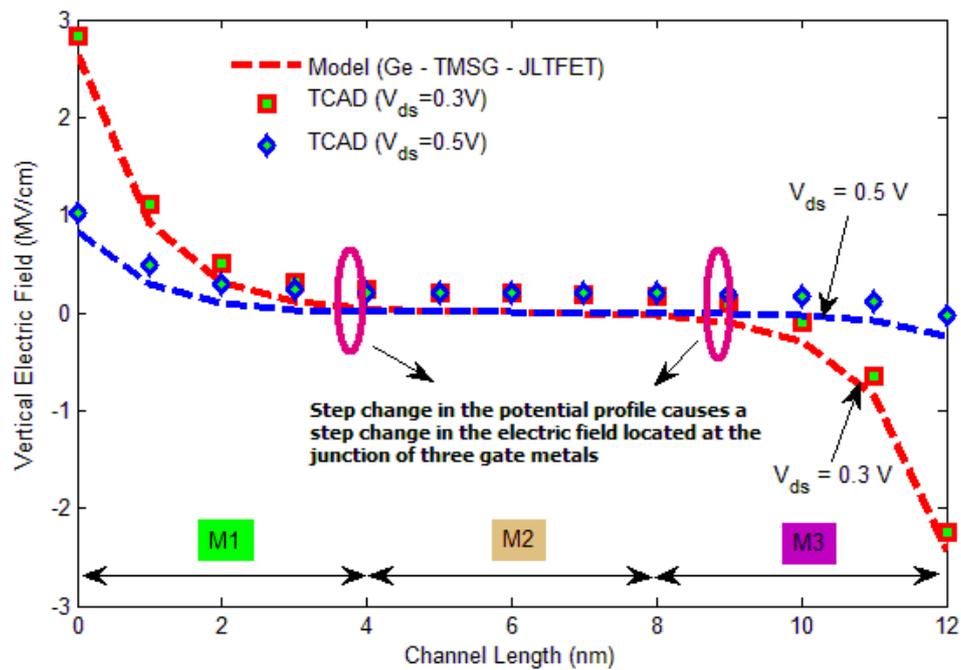


Fig.7. Plot of Vertical Electric Field shift of Ge-TMSG-JLTFET with various values of $V_{ds}=0.3\text{V}$ and 0.5V .

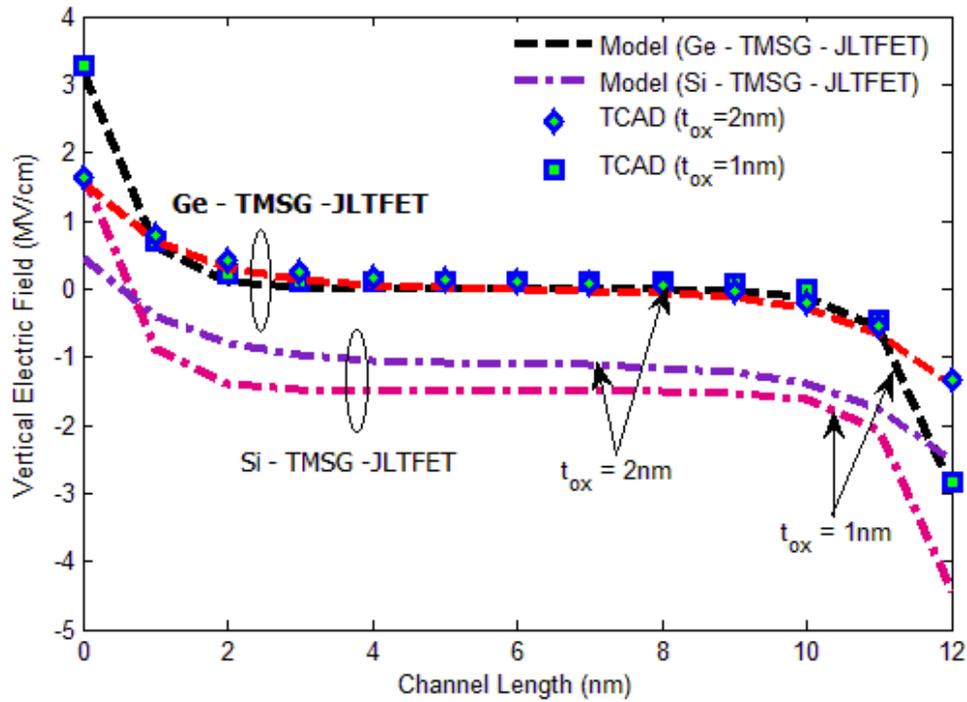


Fig.8. Variation of vertical electric field for Ge-TM-SG-JL-TFET and Si-TMSG-JLTFET for distinct values of oxide thickness, $t_{ox}=1\text{nm}$ and $t_{ox}=2\text{nm}$.

The comparisons of the Ge-TMSG-JLTFET and Si-TMSG-JLTFET vertical electric field patterns are included in Fig.8. The vertical field aspect of both models is minimal for thinner oxide thicknesses. However, for the proposed Ge-TMSG-JLTFET analytical model with titanium oxide as the dielectric gate, the strength of the electric field is better. With thin silicon dioxide layer, electrons can swiftly drift across the dielectric material and causes the gate threshold voltage to alter. Once threshold voltage is altered, this will lead to problems with instability in the structures of the device.

The threshold voltage variance of Ge-TMSG-JLTFET is shown in Fig.9 and Fig.10 for particular values of impurity doping concentration. It is visible that there is a decline in threshold voltage demonstrating a decrease in short channel effects for a given channel doping. Lower voltage circuits thereby look very attractive for mainstream memory applications which require low power and low leakage current.

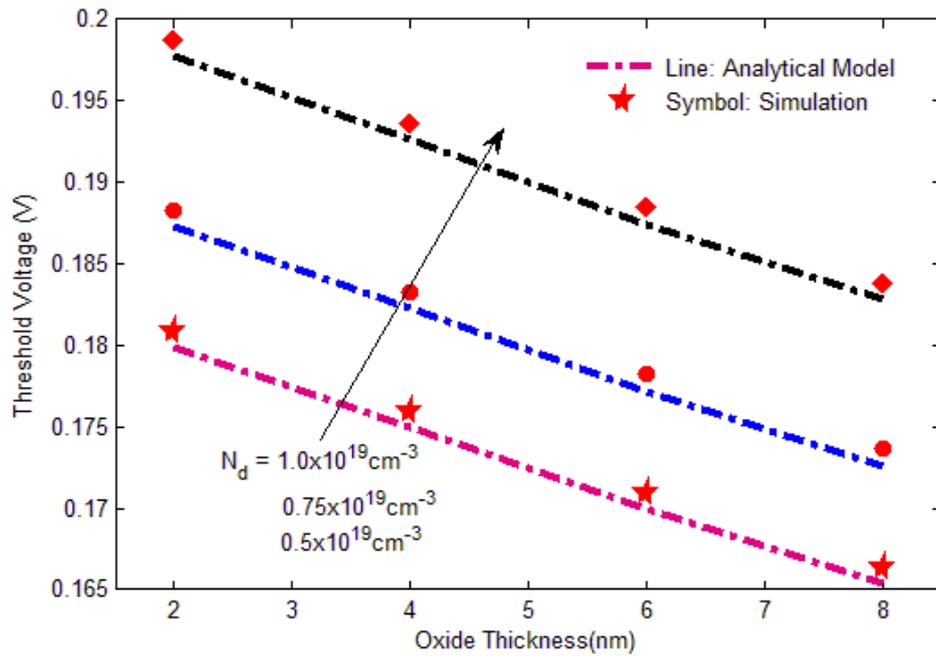


Fig.9. Plot of threshold voltage as a function of oxide thickness for various values of doping concentrations.

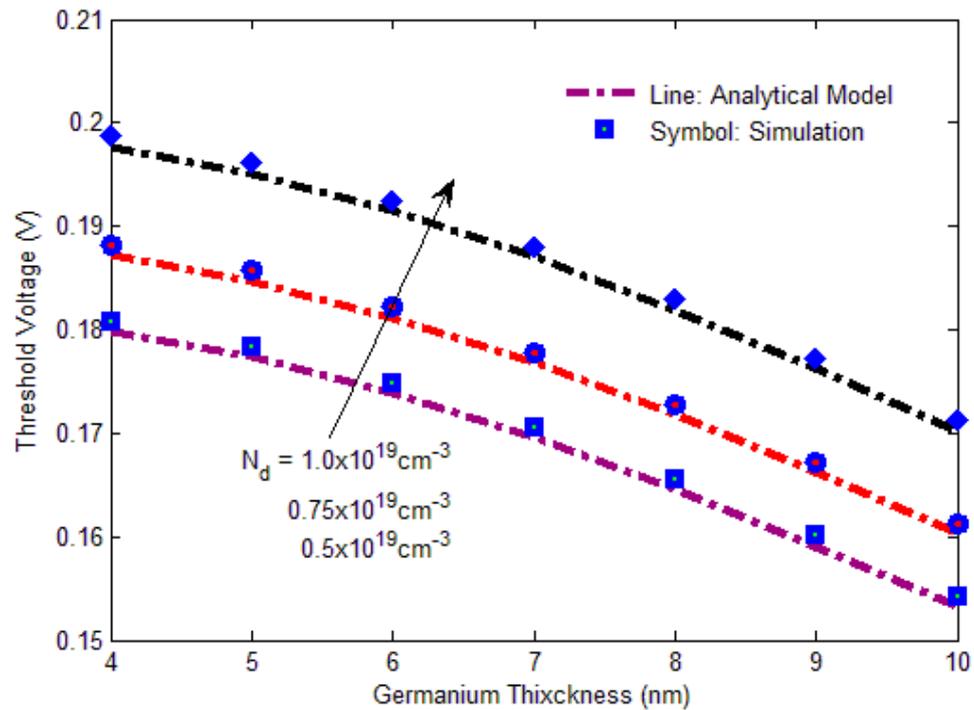


Fig.10. Threshold voltage variation of Ge-TM-SG-JLTFET for particular values of doping concentration.

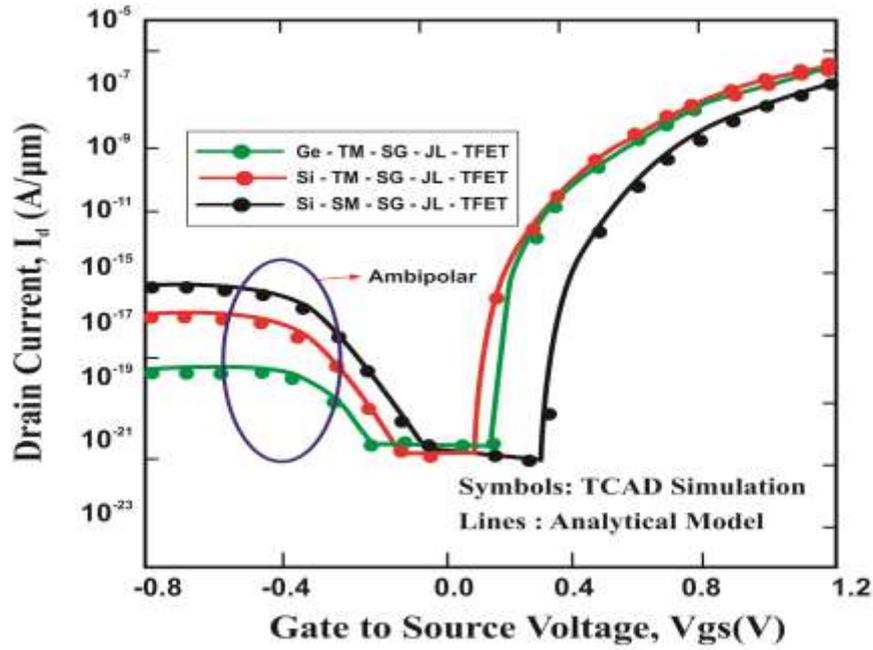


Fig.11. Ambipolar characteristics of proposed device structure with Si-TM-SG-JL-TFET and Si-SM-SG-JL-TFET at $V_{ds}=0.5V$.

Germanium-based TM-SG-JL-TFET ambipolar features are contrasted with Si-TM-SG-JL-TFET and Si-SM-SG-JL-TFET, and the system output restricting the ambipolarity is shown in Fig.11. The present structure exhibits greater ON current and reduces the ambipolar behavior due to the Ge based uniformly doped regions and high -K gate material compared to the equivalent structure of silicon based single and triple gate material. Analytical model results match well with Silvaco ATLAS TCAD simulator data and the precision of our ambipolar drain current model is verified.

3.1.6T Ge-TM-SG-JL-TFET SRAM Design

A novel 6T germanium-based TM-SG-JL-TFET SRAM has been introduced, which retains a sufficient number of transistors to form CMOS based memory cell is shown in Fig.12. Also, proposed 6T - SRAM maintains a proper read and write noise margins (RNM & WNM). Our design is composed of cross-connected inverters (INVERTER 1 and INVERTER 2) with BL and BLB bit lines connected to the Q node via T5 and T6 transistors. It is a programming technique that gives INVERTER 1 a virtual ground by writing "1" / "0" to node - Q. Simulated grounding technique tends to increase the WNM by disconnecting the cross-connected inverter (or decreasing the regenerative action).

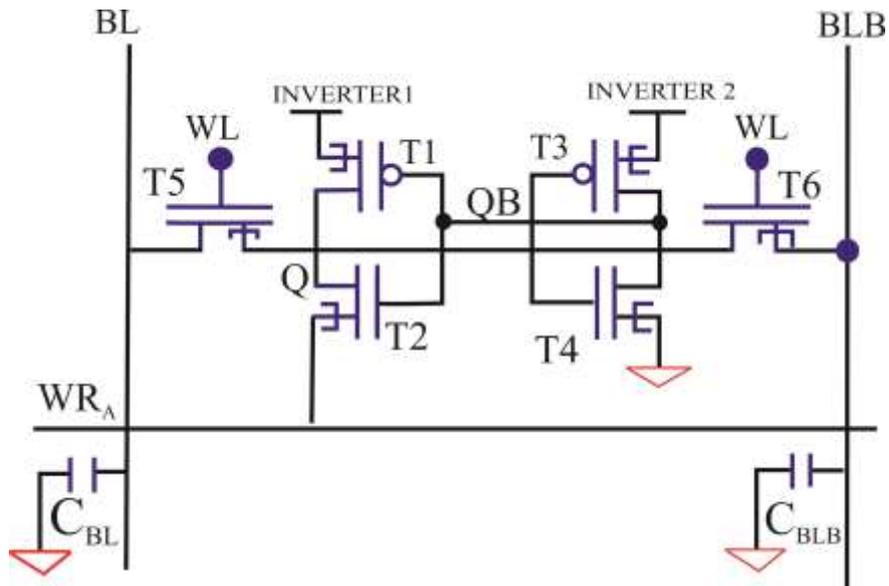


Fig.12. Proposed 6T Ge-TM-SG-JL-TFET SRAM

Metrics utilized to contrast the output of distinct SRAM designs are read - write delays. The read - delay is characterized as time - delay amidst the activation of 50 percent of the word line (WL) to 10 percent of the difference in pre-charged voltage among the bit lines. The reading delay of various SRAM designs could be seen in Fig.13. We infer that due to its high drive current, germanium-based TM-SG junctionless tunnel FETs outperform than CMOS-based SRAM design in the entire voltage range.

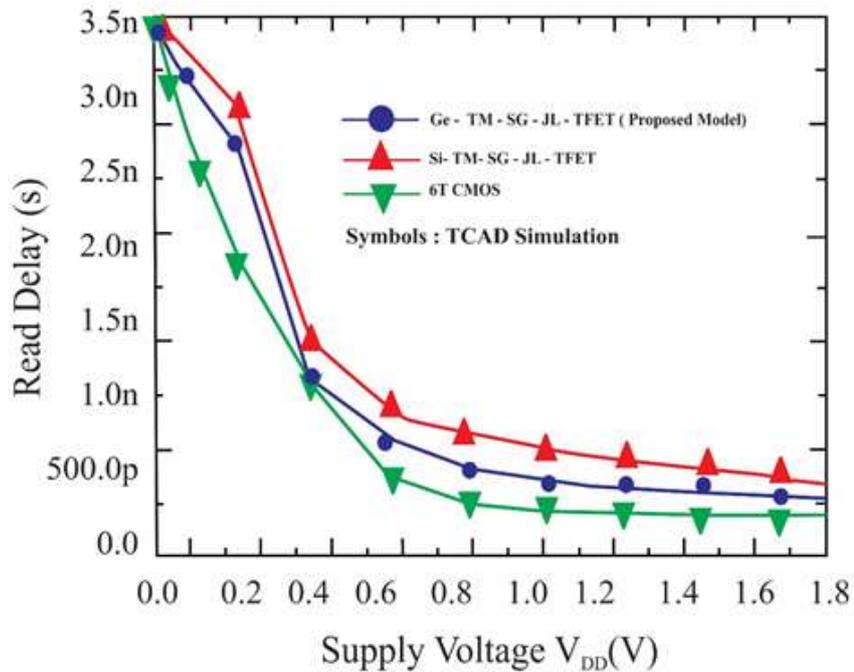


Fig.13. Read delay for various supply voltages, V_{DD}

Delay in writing is measured as time between the 50 percent activation of the word line (WL) to 90 percent of its lower voltages when internal - Q is flipped. As shown in Fig.14, the write delay of the proposed Ge-TM-SG-JL-TFET SRAM is substantially less than that of 6T CMOS and Si TM SG JL-TFET. Because of the cross-connected inverter configuration along with the Ge-TM-SG-JL-TFET, this allows for a faster writing speed than other designs. 6T CMOS and Si TM SG JL-TFET write delays are considerably higher than the proposed 6T germanium-based TM-SG-JL-TFET design at $V_{DD}=0.3V$.

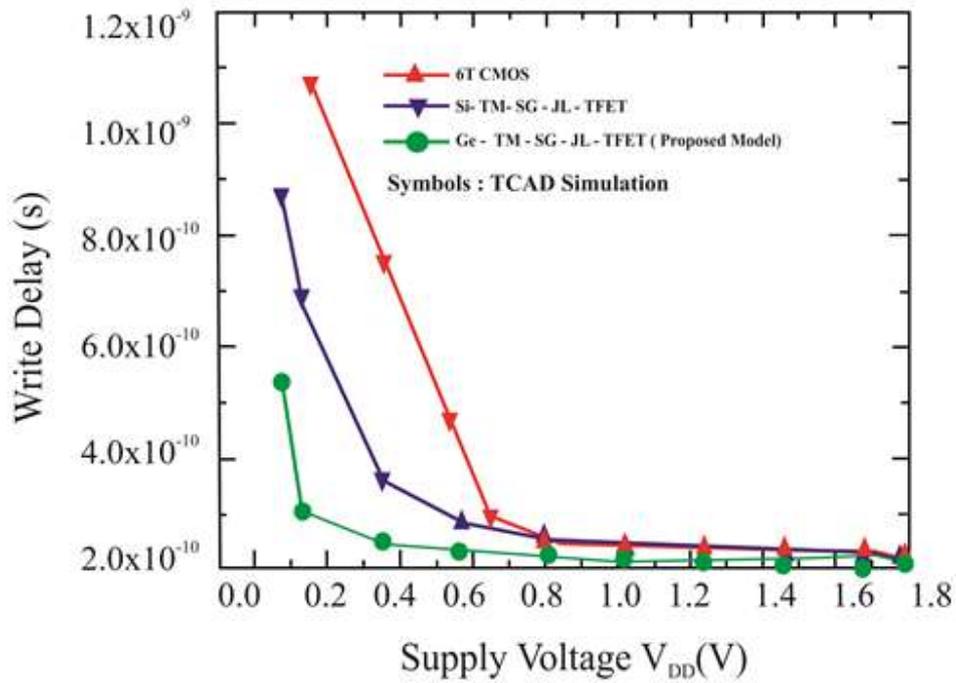


Fig.14. Write delay for various supply voltages, V_{DD}

Fig.15 depicts standby - leakage power per cell of various SRAM designs. The standby leakage power of 6T CMOS is higher than Ge TM SG JLTFET. The proposed model provides a much better leakage reduction over 6T CMOS designs at 0.3V and 0.5V V_{DD} . This reveals that conventional CMOS transistors can be well replaced by germanium-based TM-SG junctionless TFETs for low leakage memory computing applications.

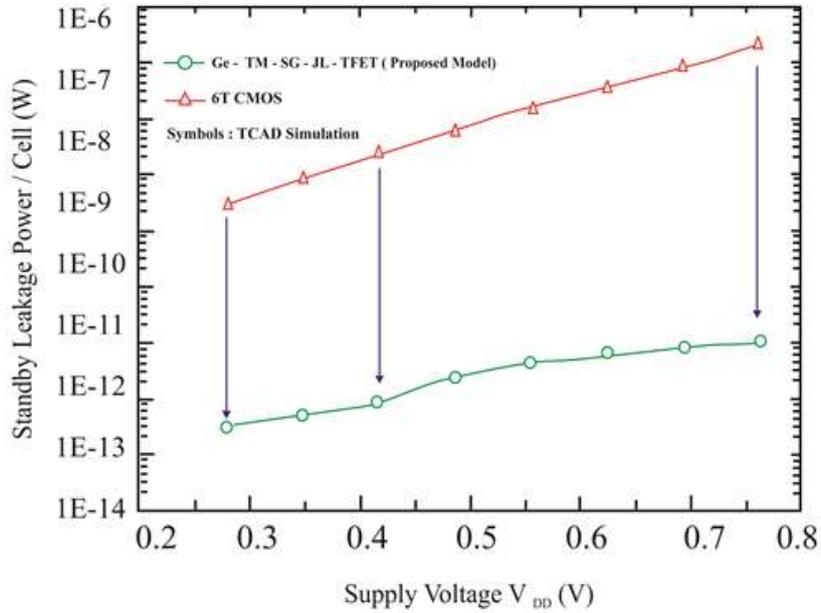


Fig.15. Standby leakage power per cell for CMOS and germanium based junctionless TFET SRAM design.

4. Conclusion

An analytical model for 12nm germanium based triple - material surrounding - gate junctionless tunnel FET is presented. To validate and verify our model, the proposed mathematical expressions have been related with silicon based TMSG-JLTFET and also with the results extracted from 3-D Silvaco ATLAS TCAD simulator. Strong correlation is observed amidst the proposed mathematical model and TCAD simulation data. With these findings, it is well established that Ge-TMSG-JL-TFET resembles to be the assuring device for low - power design of 6T SRAM. The combined dominance of germanium, titanium oxide (high-K dielectric), three distinct gate metals and the surrounding gate structure in the proposed model will hold a significant role in the future electronic framework. Most of the On-chip memory technologies embed these kind of powerful low – leakage Ge-TMSG-JL-TFET based 6T SRAM designs to mitigate the bottleneck involved in advanced scalable memory systems.

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Availability of Data and Material There are no linked research data sets for this submission. The following reason is given: No data was used for the research described in the article.

Code Availability – Not Applicable

Author's Contributions Author 1 (G. Lakshmi Priya): Conceived and design the analysis, contributed data and analysis tools, and wrote the paper. Author 2 (M. Venkatesh): Performed the analysis, calibrated the results, and wrote the paper. Author 3 (N. B. Balamurugan): Worked in TCAD portion of the proposed device, Experimental data analysis. Author 4 (T. S. Arun Samuel): Worked in TCAD simulation of SRAM design, and wrote the paper for the corresponding portion.

Compliance with Ethical Standards

Conflict of Interest All authors have participated in (a) conception and design, or analysis and interpretation of the data; (b) drafting the article or revising it critically for important intellectual content; and (c) approval of the final version. This manuscript has not been submitted to, nor is under review at, another journal or other publishing venue. The authors have no affiliation with any organization with a direct or indirect financial interest in the subject matter discussed in the manuscript.

Ethical Approval “All procedures performed in studies involving human participants were in accordance with the ethical standards of the institutional and/or national research committee and with the 1964 Helsinki declaration and its later amendments or comparable ethical standards.

Informed Consent “Informed consent was obtained from all individual participants included in the study.”

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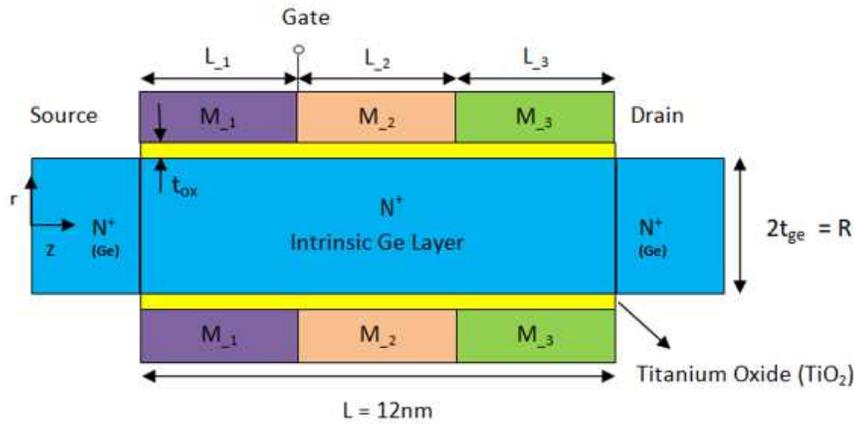
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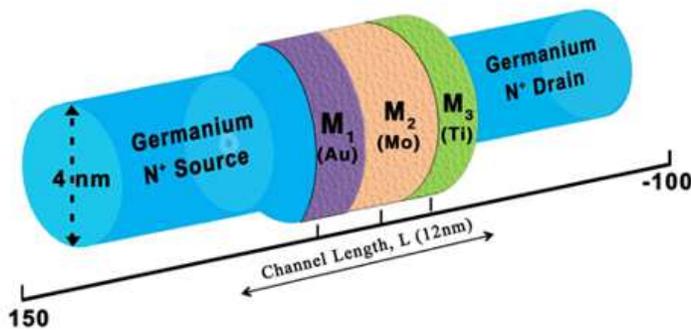
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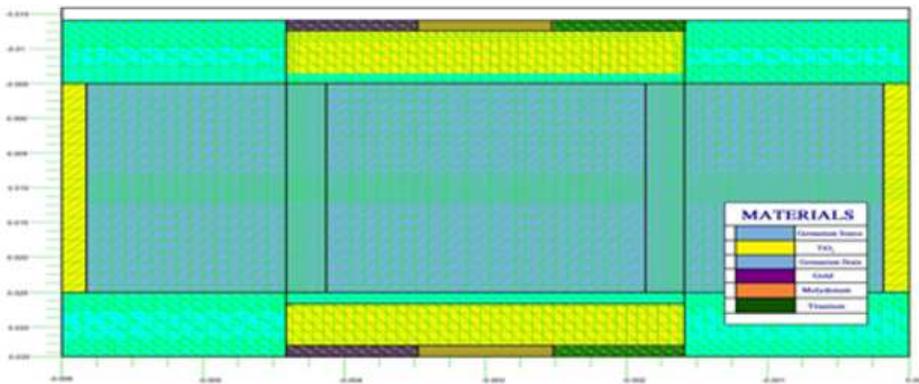
Figures



(a)



(b)



(c)

Figure 1

(a) 12nm Ge based Triple Material - Surrounding Gate - Junctionless - Tunnel FET (Ge-TM-SG-JL-TFET)– Cross sectional view (b) 3D ATLAS TCAD representation of the proposed device (c) Simulated mesh profile of Germanium based TM-SG-JL-TFET by Silvaco ATLAS.

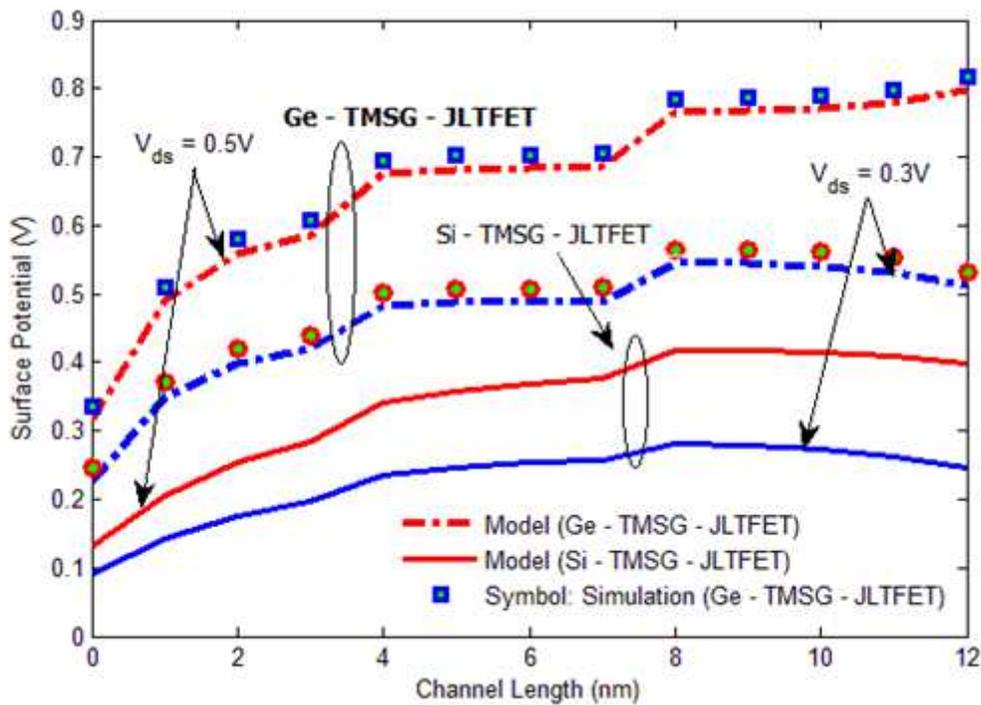


Figure 2

Surface potential distribution of Ge-TM-SG-JL-TFET and Si-TM-SG-JL-TFET with respect to different values of $V_{ds}=0.3V$ and $V_{ds}=0.5V$.

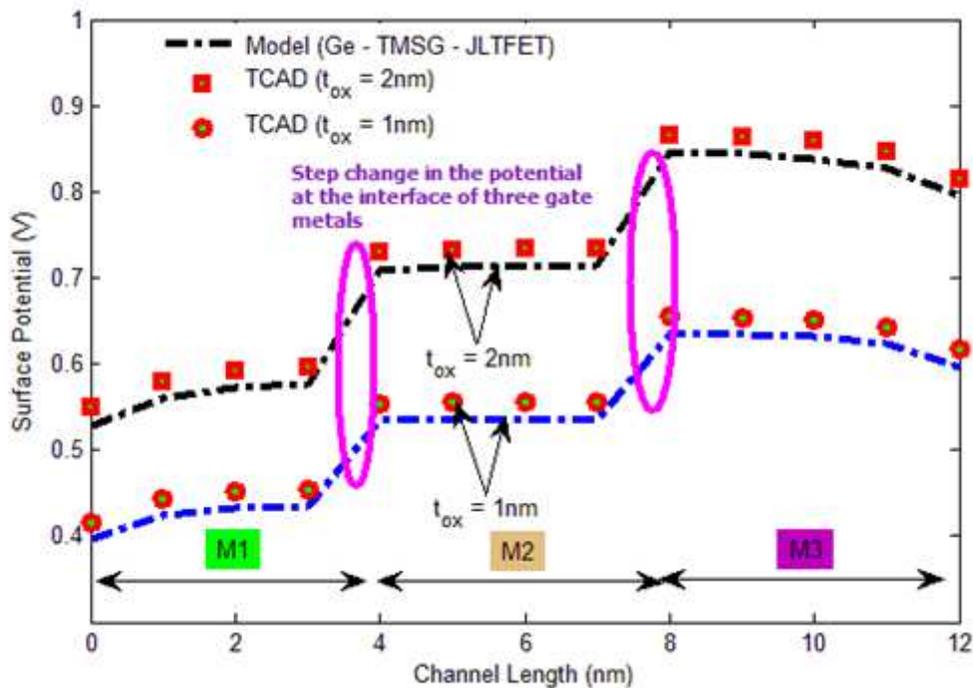


Figure 3

Surface potential profile of Ge-TM-SG-JL-TFET for values of oxide thickness, $t_{ox}=1nm$ and $t_{ox}=2nm$.

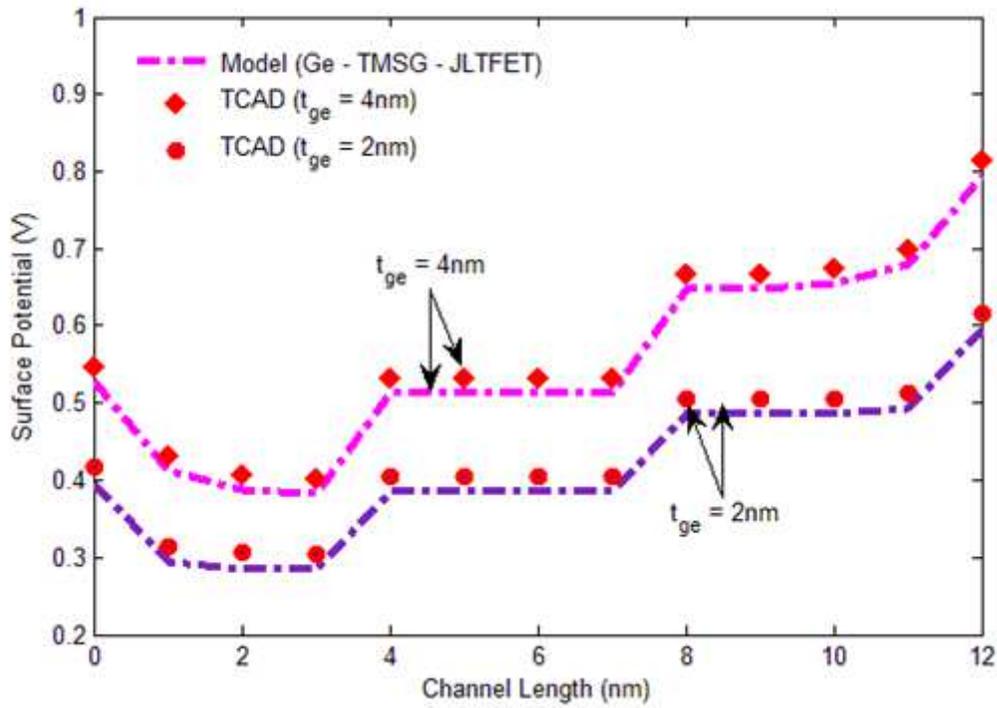


Figure 4

Surface potential profile of Ge-TM-SG-JL-TFET for distinct values of germanium thickness, $t_{ge}=2\text{nm}$ and $t_{ge}=4\text{nm}$.

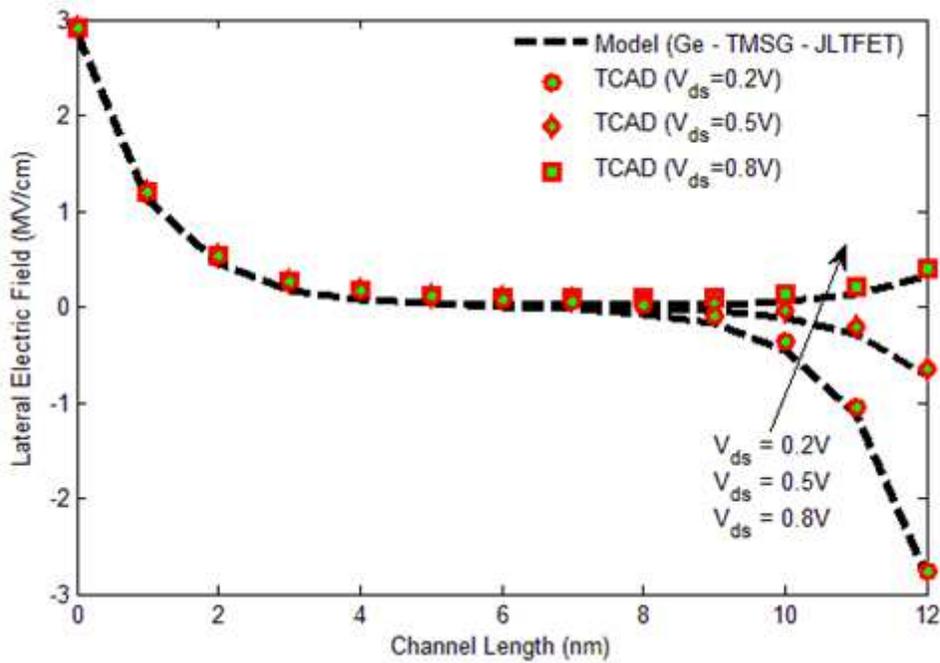


Figure 5

Lateral Electric Field distribution of Ge-TM-SG-JL-TFET for different values of $V_{ds}=0.2\text{V}$, 0.5V and 0.8V .

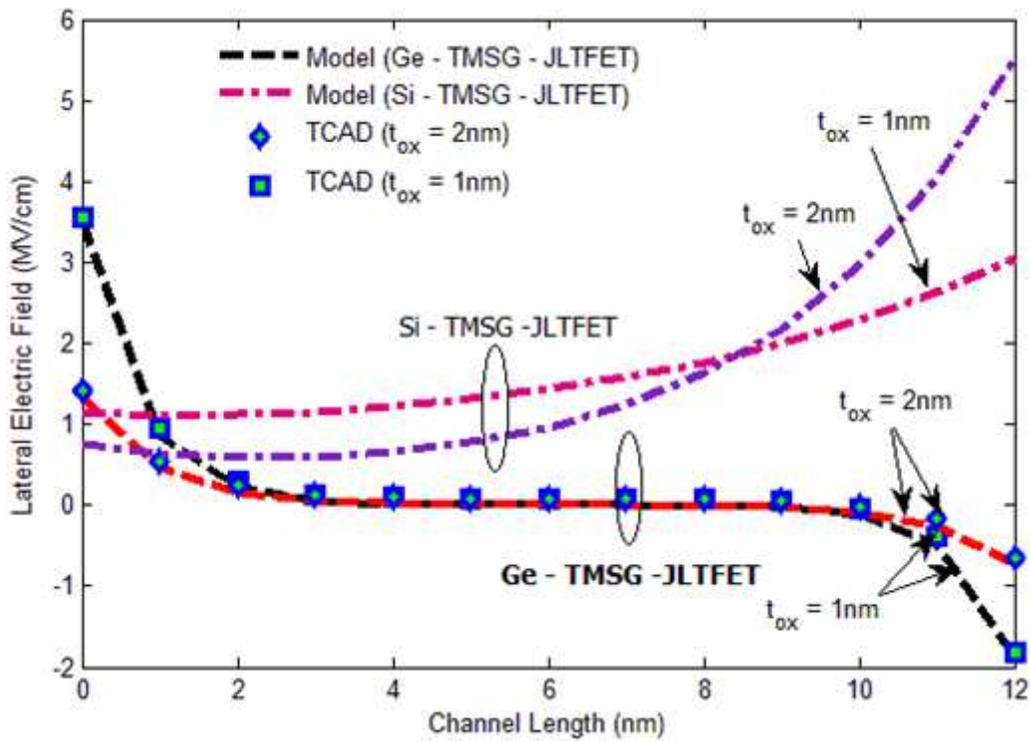


Figure 6

Variation of Lateral Electric Field of Ge-TM-SG-JL-TFET and Si-TM-SG-JL-TFET with respect to different values of oxide thickness, $t_{ox}=1\text{nm}$ and $t_{ox}=2\text{nm}$.

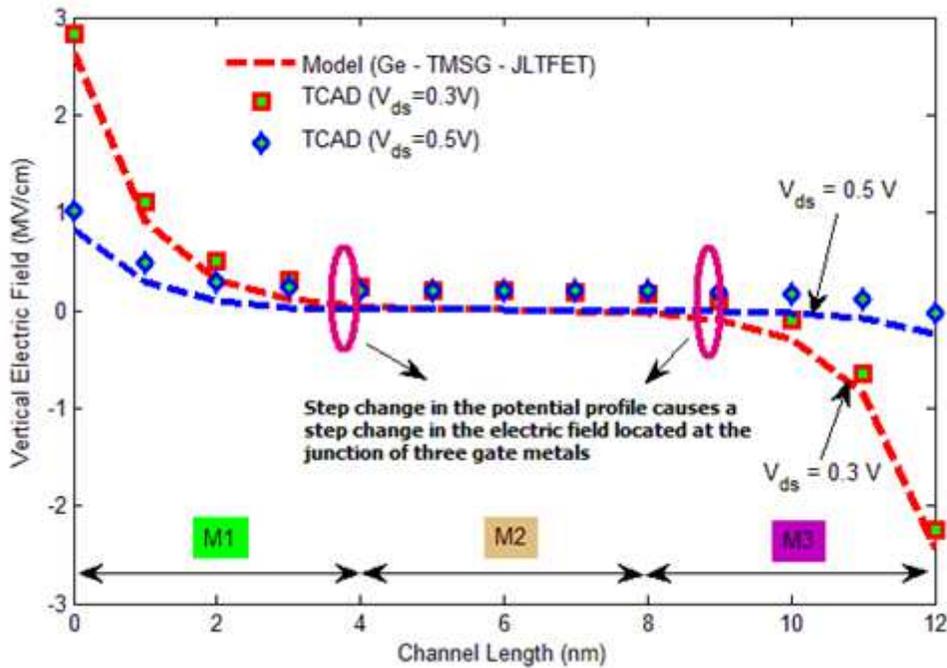


Figure 7

Plot of Vertical Electric Field shift of Ge-TMSG-JLTFET with various values of $V_{ds}=0.3\text{V}$ and 0.5V .

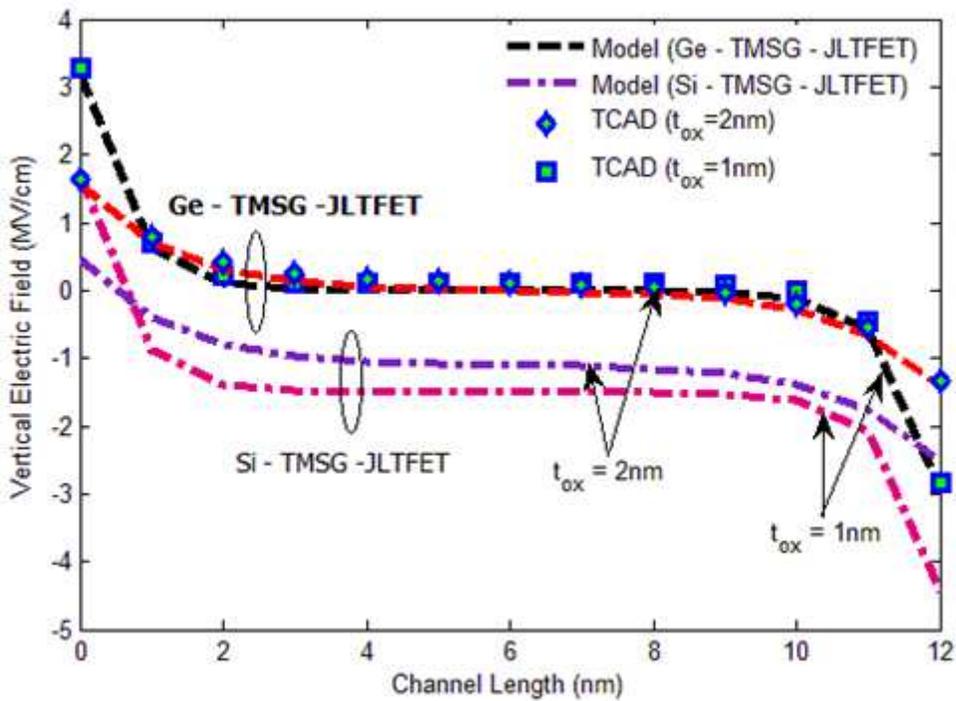


Figure 8

Variation of vertical electric field for Ge-TM-SG-JL-TFET and Si-TMSG-JLTFET for distinct values of oxide thickness, $t_{ox}=1\text{nm}$ and $t_{ox}=2\text{nm}$.

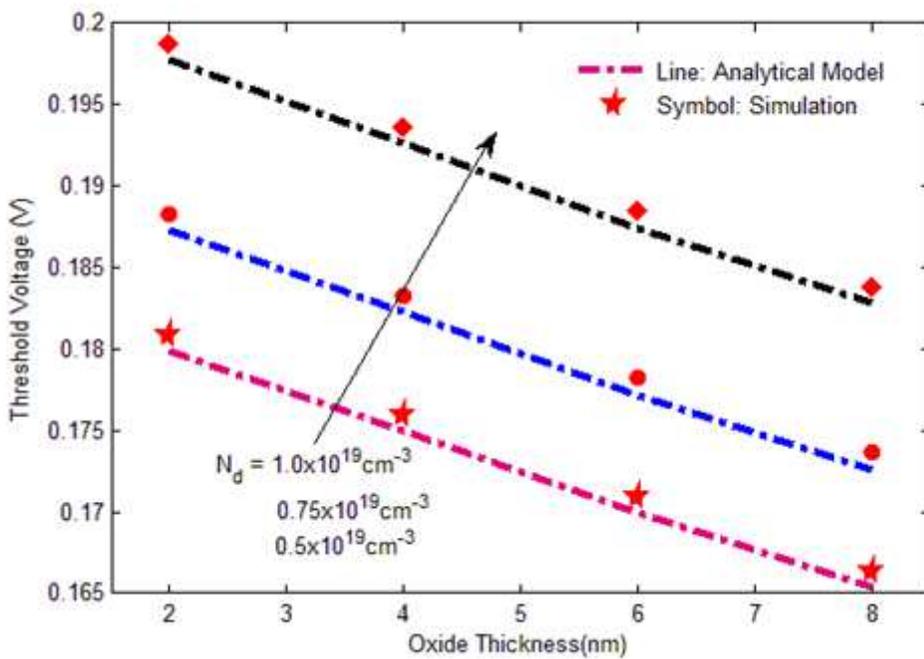


Figure 9

Plot of threshold voltage as a function of oxide thickness for various values of doping concentrations.

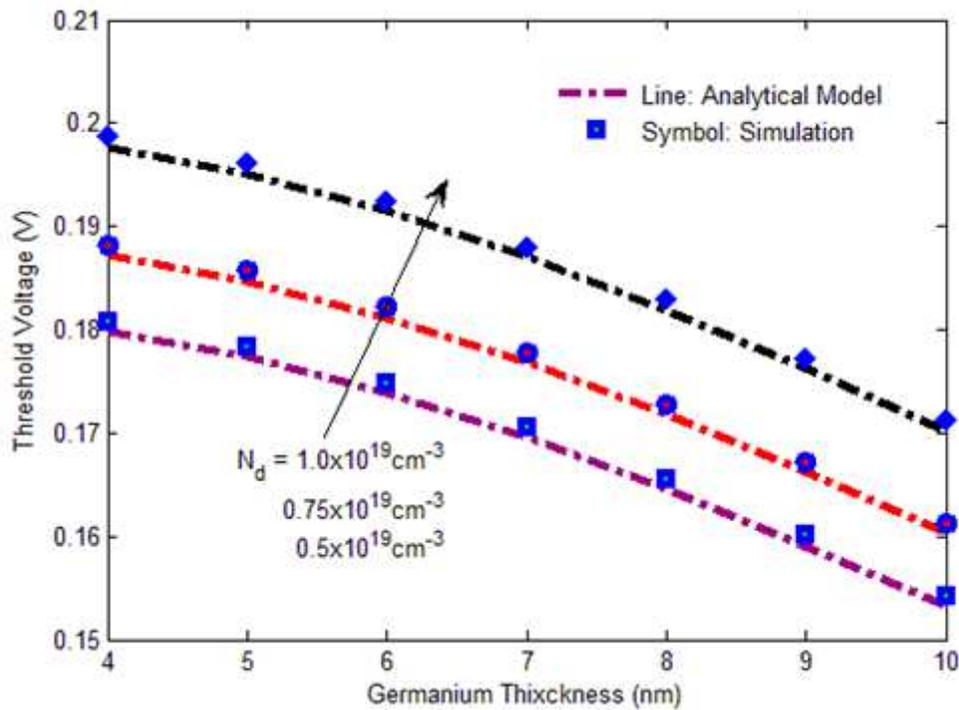


Figure 10

Threshold voltage variation of Ge-TM-SG-JLTFET for particular values of doping concentration.

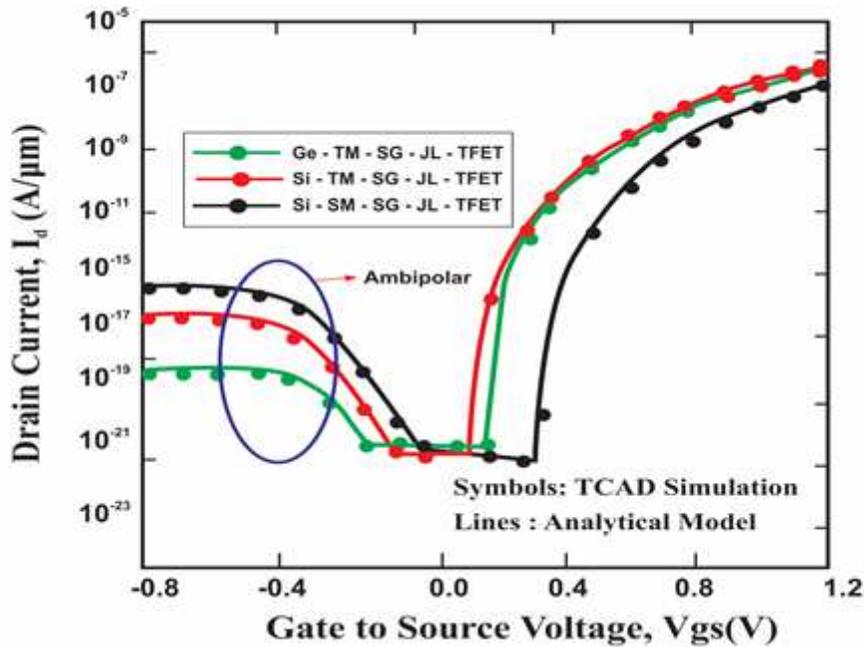


Figure 11

Ambipolar characteristics of proposed device structure with Si-TM-SG-JL-TFET and Si-SM-SG-JL-TFET at $V_{ds}=0.5V$.

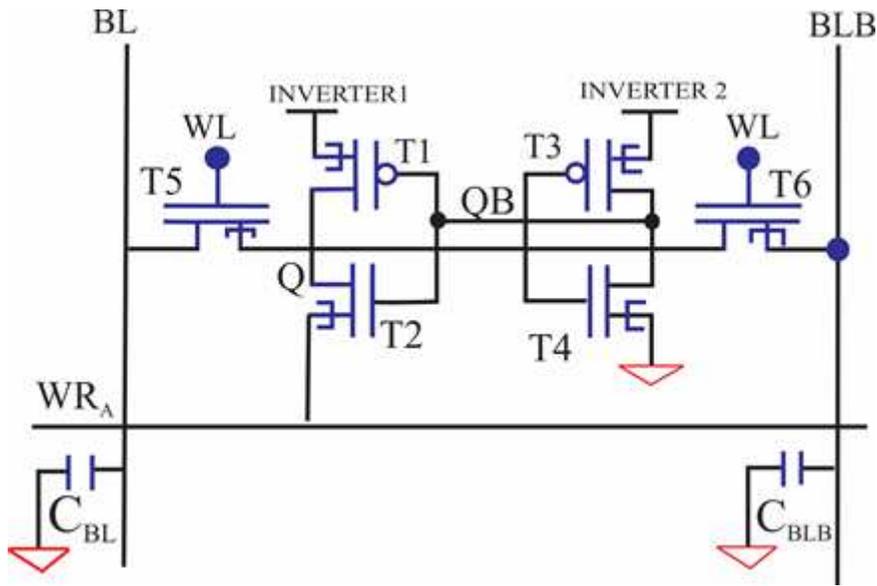


Figure 12

Proposed 6T Ge-TM-SG-JL-TFET SRAM

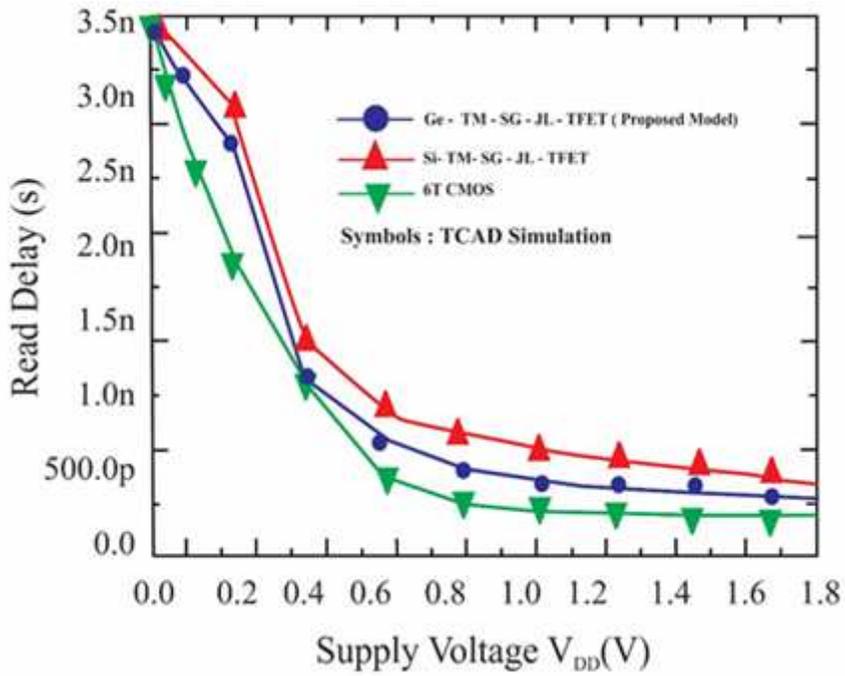


Figure 13

Read delay for various supply voltages, VDD

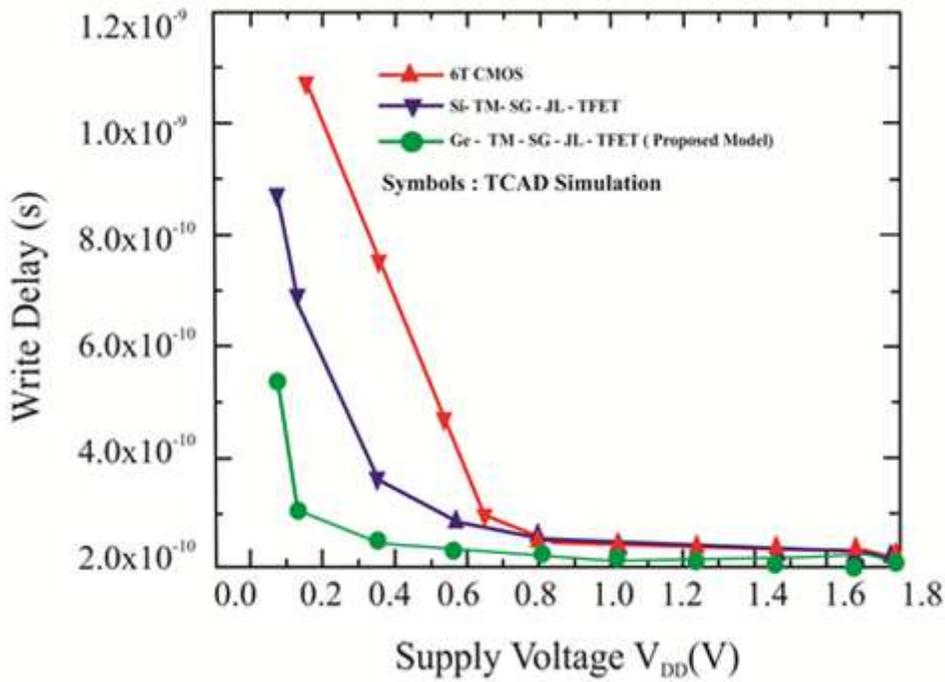


Figure 14

Write delay for various supply voltages, VDD

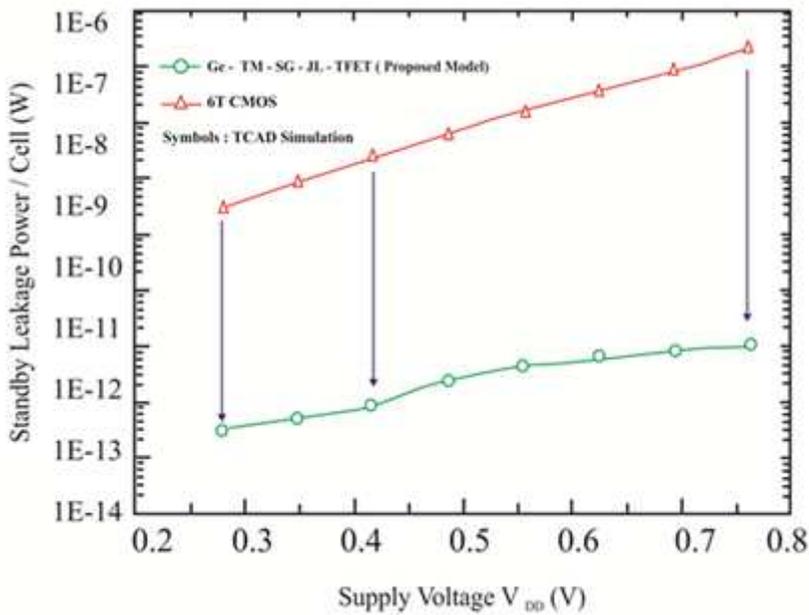


Figure 15

Standby leakage power per cell for CMOS and germanium based junctionless TFET SRAM design.