Optimizing of Communications Systems Power Efficiency Considerations: Efficient Implementing Approach of Hamming Codes Utilizing FS-GDI

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Research Article

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Abstract

Due to the power efficiency importance of digital signal processing and data protection in different communications systems, this paper proposes an efficient design of different Hamming Codes utilizing Full Swing- Gate Diffusion Input (FS-GDI) approach. The proposed codes design aims to improve the power efficiency and the required area through reducing the required number of transistors. FS-GDI is a new low power VLSI design approach, it is a power effective approach for realizing the different logic gates. In this work, the Hamming codes (7, 4) and (11, 7) are designed by utilizing the original GDI, FS-GDI and the traditional CMOS approaches. The amount of consumed power, delay time, Power Delay Product (PDP) and hardware simplicity-Number of Transistors (No.Ts) are employed as a metrics for evaluating the efficiency of the proposed design compared to the traditional design. The design simulation experiments are executed utilizing Cadence Virtuoso simulator package under 65nm technology. The simulation experiments revealed these proposed codes achieve delay time reduction by 52.91% and 10% for Hamming codes (7, 4) and (11, 7), respectively On the other hand, the Hardware (H/W) of these codes became more simple where the H/W simplicity of the used Hamming codes is reduced 50 % CMOS approaches respectively. From the results analysis, the proposed design achieves efficient power and the delay optimizing of Hamming codes utilizing the FS-GDI approach. On the other hand, the power consumption and area in communications systems due to the encoding process can be reduces.

1. Introduction

The channel coding techniques play important role in the transmitted data protection over the wireless communications channels. The amount of consumed power limits the utilizing of error coding techniques and the powerful data security techniques due to its computational complexity [1]. In this paper, low power error control hamming codes design is proposed using FS-GDI approach. The FS-GDI approach is power efficient low power VLSI logic style compared to the traditional approaches [2-10].

In [11] the complexity in the wireless communications due to the amount of the transmitted data encoding is analyzed based on the used error control code is the Convolutional codes and the Hamming code. The presented analysis in this paper proved that the complexity is related to the amount of required/consumed power. That means with increasing the computational complexity, the consumed power increases. On the other hand. the power efficiency of the communications systems is considered in several research papers [12-19]. The power is main constraint for the application of the data protection techniques. Hence, design low power error control schemes using the power efficient approach will be increasing the capability of data protection techniques using and enhancing the power efficiency of the systems in general [20].

In this paper, different Hamming codes design is proposed based on GDI and FS-GDI approaches. The proposed codes design is compared with the traditional CMOS approach utilizing different metrics such as the delay time, consumed power, Power Delay Product (PDP) and number of transistors which are required for implementing the Hamming codes by the different traditional CMOS, GDI and FS_GDI

approaches. The simulation experiments prove the superiority of the proposed Hamming code design using FS-GDI compared to the traditional approach. The software package which is used for performing the design and the simulation experiments is Cadence Virtuoso simulator [21-24].

In the following, the rest of paper is presented as follows: section 2 presents the low power VLSI approaches and its sub-approaches. GDI approach Development and Versions are introduced in section 3. In section 4, the complexity due to the encoding process is discussed. The proposed work description of different Hamming implementation and experiments codes are presented in section 5. In section 6, result analysis is presented. the conclusion is introduced in section 7.

2. Low Power Vlsi Approaches Overview

The different styles of the VLSI are presented in this section. In the following, the different approaches advantages and disadvantages are discussed. Figures 1 and 2 give AND and XOR logic gates realizing using the different approaches, respectively.

The Complementary symmetry metal-oxide-semiconductor CMOS is the most popular approach, it has several advantages such as, low noise margin, high speed, low power, easy to develop, common in most chips design of VLSI. Also, it suffers some problems such as, high power dissipation, large number of transistors/area, long delay time, power consumption high. The second common approach is the Pass Transistor Logic (PTL), it is popular as CMOS approach, its features as decreased silicon area, speed, reduced power consumption, slower at reduced power, significant power dissipation [25-28].

The third approach is the Transmission Gate (TG), its feature is less transistor for implementing complex gates, PMOS and NMOS combination avoid noise margin, power dissipation, switching, require control, limited TG cascade. The fourth approach is the Complementary Pass-Transistor logic- (CPL), (N-MOSFET approach), its advantages is high speed, low i/p capacitance and easy to implement complex logic by NMOD net. It is drawbacks is drop in threshold voltage, static power consumption and delay increases with long pass-transistor chains. The Double Pass-transistor Logic (DPL) approach is the modified of CPL approach, it has some advantages as well-balanced input capacitance No drop voltage, no need buffers, full swing and low power, its main problems are large area and inverters need [29-32].

3. Gdi Approach Development And Versions

A long fourteen years, Morgenshtein et al. presented the GDI approach for low power VLSI implementing. In 2002, 2010 and 2014, the original cell of GDI, modified GDI and Full Swing GDI have been presented, respectively by Morgenshtein. Gate diffusion input (GDI) is a new low power technique using small silicon chip area for digital VLSI design compared to another logic style proposed by Morgenshtein. This approach aimed to improve the power consumption and area as well as propagation time of the logic gates implementing compared to the traditional approaches [33-35].

In 2001, the GDI approach was invented, it allowed complex gate implementing by two transistors. This method is suitable for the design of fast, low-power circuits, using a reduced number of transistors (as compared to CMOS and existing PTL techniques) as shown in Table 1 [33]. As shown in this table the different logic gates hardware can be simplified by reducing the number of transistors to be more power efficient.

Table 1 Transistors count between GDI and CMOS for various functions.

Different Realized Function	CMOS Approach	GDI Approach
F1=B	6	2
F2=+B	6	2
OR	6	2
AND	6	2
NAND	4	4
NOR	4	4
MUX	12	2
NOT	2	2

Figure 3 shows the GDI approach versions from 2001 to 2014. Fig. 2a gives the original cell of GDI, Fig. 2b presents the modified cell, while the last version of GDI approach is shown in Fig. 2c. Using GDI technique allowed improvement in power consumption, propagation delay and area of VLSI digital circuits compared to CMOS and pass transistor logic (PTL) techniques. PTL and GDI both suffered from reduced voltage swing at their outputs due to threshold drops. Problems of the first GDI cell are solved by Morgenshtein in 2014 through proposing the Full Swing GDI (FS-GDI) based on a single swing Restoration Transistor (SR) as an alternative to another method. The SR transistor ensures full swing operation [35].

The logic gates such as AND, OR and XOR gates can be implemented with full swing operation can be achieved but with increasing the transistor count from 2 to 3 compared to the original GDI design. In [36], Shoba and et al proposed a new design of AND, OR and XOR logic gates based on full swing GDI technique, which are used to implement three designs of full adder [36]. However, the three full adders are successfully realized using full swing gates with a significant improvement in their performance [37-38].

4. Encoding Process Complexity

As mentioned in section 1, the computational complexity is the amount of operations in the systems for perfuming its function. The complexity is directly related to the amount of the required power and the process time, it is called also time complexity. The error control codes utilizing for data protection is

essential issue. The computational complexity of these codes differs according to its type and capabilities. The block codes such as Hamming codes complexity is determined based on its data-word (k) and codeword (n) length, in general it simpler than the Convolutional codes. The Convolutional codes encoding/decoding have high complex compared to the block codes [40]. In this paper, the simpler block codes (Hamming codes) are chosen for evaluating the proposed design of data protection techniques by the FS-GDI approach.

The complexity basis of error control codes is presented in this section. Block codes complexity is limited and lower than Convolutional codes [20]. Mostly, complexity of block codes is controlled by two factors, which are the input length of the encoder and the codeword the output of the encoder. In the block codes the length of the processed data is not important factor, the packet already segmented to small parts each one of them has length of data word. In the Convolutional codes, the complexity is controlled by many factors, length of input it is the processed data in the same time interval, the length of output, the length of the processed data "packet length" and finally, length of the memory in Convolutional encoder. In fact, the computational complexity of the Convolutional codes increases with the constraint length increasing [41-42].

In this table, the extra computational complexity related to the proposed technique is considered and the complexity related to the memory length of the convolutional encoder also. As shown in the numerical analysis of the hardware complexity of the traditional CMOS approach and FS-GDI approach Hamming codes in Table 4, it proves that the superiority of the proposed technique complexity especially with the longer data-word packets processing.

5. The Proposed Scheme Description

In this section, the different Hamming codes (7, 4) and (11, 7) implementation approaches are presented. The FS-GDI approach are proposed for implementing the Hamming codes as an approach for achieving power efficient data encoding tool.

5.1 The Proposed FS-GDI Hamming Code (7,4) Design Implementing

In this section, simple data protection Hamming code (7, 4) error control scheme is implemented and realized by the FS-GDI approach for enhancing its power efficiency and hardware simplicity. In this error control code, 7 number represents the number of output of Hamming encoder bits it is 7 bits. The number 4 refers to the number of bits encoder input, it is 4 bits in this encoder.

Hamming Algorithm mechanism:- The Hamming code algorithm is working as described following steps:

- The parity bits (P) are generated and added to (k) bits data-word to form the code-word of (n)n=k+P bits.

- The P bits are generated by the simple equations from the input data (data-word).

The data-word is the input of the encoder circuit, it performs XOR operations on the k data-word, hence the required (p) parity bits generated. Parity bits and data bits together form the code word. An encoder circuit of Hamming code for 4-bit data word is shown Fig. 4. Following this circuit pattern, we can design an encoder circuit of hamming code for 7-bit data word and it is implemented in cadence virtuoso tool.

Fig. 4 consists of 4-bit data word, parity bit generator and 7-bit code word. The 4-bit data word is applied as an input to the encoder circuit, now the encoder output consist of 7-bits i.e. 4-data bits D_1, D_2, D_3 & D_4 and 3-parity bits P_1, P_2 & P_4, as in Eqs (1-3):

$$P_1=D_1 \oplus D_2 \oplus D_4 \quad (1)$$

$$P_2=D_1 \oplus D_3 \oplus D_4 \quad (2)$$

$$P_4=D_2 \oplus D_3 \oplus D_4 \quad (3)$$

The Codeword : $D_4D_3D_2P_4D_1P_2P_1$

The data word is applied as an input to the encoder circuit which performs XOR operations on the given data word thus the required parity bits are generated from the parity bit generator. Parity bits and data bits together form the code word. An encoder circuit of hamming code for 4-bit data word is shown in Fig. 4. The Hamming encoder consists of 4-bit data word, parity bit generator and 7-bit code word. The 4-bit data word is applied as an input to the encoder circuit, now the encoder output consists of 7-bits i.e. 4-data bits D_1, D_2, D_3 & D_4 and 3-parity bits P_1, P_2 & P_4, as in Eqs (1-3).

a. Testing the Proposed design of Hamming Encoder (7, 4) Performance

Simulations were done using the spectre based Cadence Virtuoso simulator with a power supply of 1V and frequency 100M HZ, the size of PMOS is twice the NMOS transistor size Wp/L=240/60, Wn/L=120/60 (PMOS and NMOS) respectively to achieve the best power and delay performance. Each component is analyzed in terms of propagation delay, power dissipation, and their product. The propagation delay is measured by accounting the time taken from 50% of the input voltage swing to 50% of the output voltage swing for each transition. Table 2 shows the values of the evaluating metrics of the proposed implementing approach of Hamming code (7, 4).

Table 2 Metrics values of the proposed Hamming Encoder (7,4) design with respect to the different approaches: Proposed & Traditional

Utilized Approach	Metrics of Performance Evaluation			
	Power(uw)	Delay(ps)	Energy (PDP)	No.T
Hamming Encoder with CMOS	34.4	72		72
Hamming Encoder with GDI	30	80		40
Hamming Encoder with FS-GDI	19	33.9		36

5.2 The Proposed FS-GDI Hamming Code (11,7) Design Implementing

The second implemented Hamming code by the FS-GDI for a 7-bit data word, the code word consists of 11-bits i.e. 7-data bits D1, D2, D3, D4, D5, D6, D7 and 4- parity bits P1, P2, P4 & P8 as shown in Table 2. The parity bits calculated for 7-bit data is as follows in Eqs (4-6):

$P1=D1\oplus D2\oplus D4\oplus D5\oplus D7$ (4)

$P2=D1\oplus D3\oplus D4\oplus D6\oplus D7$ (5)

$P4=D2\oplus D3\oplus D4$ (6)

$P8=D5\oplus D6\oplus D7$ (7)

The Codeword :. $D_7D_6D_5P_8D_4D_3D_2P_4D_1P_2P_1$

a. Performance Evaluating of the Proposed Hamming Encoder (11, 7) Design

Table 3 Metrics values of the proposed Hamming encoder (11, 7) design with respect to the different approaches: Proposed & Traditional

Utilized Approach	Metrics of Performance Evaluation			
	Power(uw)	Delay(ps)	Energy (PDP)	No.Ts
Hamming Encoder with CMOS	52	100		144
Hamming Encoder with GDI	45	127		96
Hamming Encoder with FS-GDI	38	90		72

Table 3 shows the values of the evaluating metrics of the proposed implementing approach of Hamming code (11, 7). As shown in the previous experiments which are devoted for evaluating the performance of the proposed design of the different Hamming codes with the various data-word and codeword lengths.

The values of the utilized metrics which are measured in these experiments clear the superiority of the Hamming codes implementation based on the FS-GDI compared to the CMOS approach based.

6. The Results Analysis

In this section, the previous experiments results are analyzed numerically. By considering the metrics results of the CMOS approach scenario is the standard and traditional approach, the improving percentage denotes by +, This + symbol means there is amount of improvement. On the other hand the (-) symbol means there is not improving. In Table 4, the results are analyzed numerically as cleared.

Table 4 Metrics values analyzing of the proposed implementing of Hamming codes based FS-GDI approach compared to the traditional approach

Hamming Codes & Implementation Approaches		**Amount of Improving compared to Traditional COMS Implementation**		
		Consumed (P)%	Delay(ps)%	H/W Simplicity %
Hamming Code (7, 4)	Original GDI Approach	+12.78%	-11.11%	+44.44%
	FS-GDI Approach	+44.77%	+52.91%	+50%
Hamming Code (11, 7)	Original GDI Approach	+13.46%	-27%	+33.33%
	FS-GDI Approach	+26.93%	+10%	+50%

As shown in Table 4, the proposed Hamming codes implementing using the FS-GDI achieves power efficiency 44.77% and 26.93% for the Hamming codes (7, 4) and (11, 7), respectively compared to the CMOS approach. While these proposed codes achieve delay time reduction by 52.91% and 10% for Hamming codes (7, 4) and (11, 7), respectively. These results clear the efficiency of the presented approach for implementing the different error control techniques. In general, the utilizing these proposed implementation approach reduces the power consumption of the data encoding. On the other hand, the Hardware (H/W) of these codes became more simple where the H/W simplicity of the used Hamming codes is reduced 50 % as shown in the results analysis table.

7. Conclusion

This paper proposes the FS-GDI approach for implementation the error control schemes for enhancing the power efficiency of the data encoding process. The paper presents proposed implementation of Hamming codes (7, 4) and (11, 7) using FS-GDI approach. The proposed design and simulation experiments are carried out using Cadence Virtuoso simulator package. There are different metrics are utilized for measuring the performance of the proposed FS-GDI based Hamming codes. The simulation experiments results prove the superiority of the proposed data encoding tool compared to the traditional

approach. The proposed approach for Hamming codes implementation achieves 50 % H/W simplicity. Also, the power efficiency of the proposed Hamming codes is improved by 44.77% and 26.93% for the Hamming codes (7, 4) and (11, 7), respectively compared to the CMOS approach. On the other hand, the delay time is optimized in the proposed Hamming codes implementation approach compared to the traditional CMOS approach. Finally, the proposed Hamming codes in this research paper presents a method for high efficient power data encoding process. This approach can be suitable for implementing the complex error control schemes.

Declarations

Conflict of Interest:

- Author 1: Mohsen A. M. El-Bendary declares that he has no conflict of interest. Author 2: O. El-Badry declares that he has no conflict of interest.

Declaration:

- Authors declare and confirm that there is no funding was received for this work.

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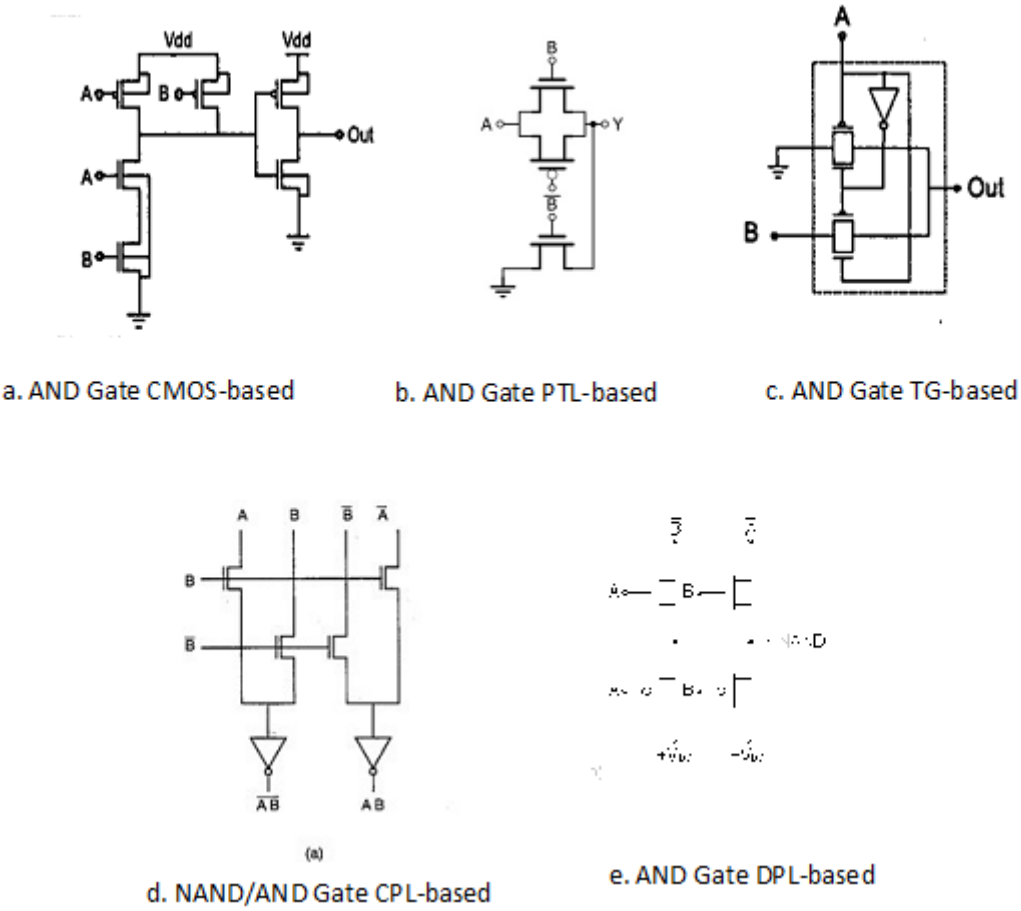
Figures



a. AND Gate CMOS-based

b. AND Gate PTL-based

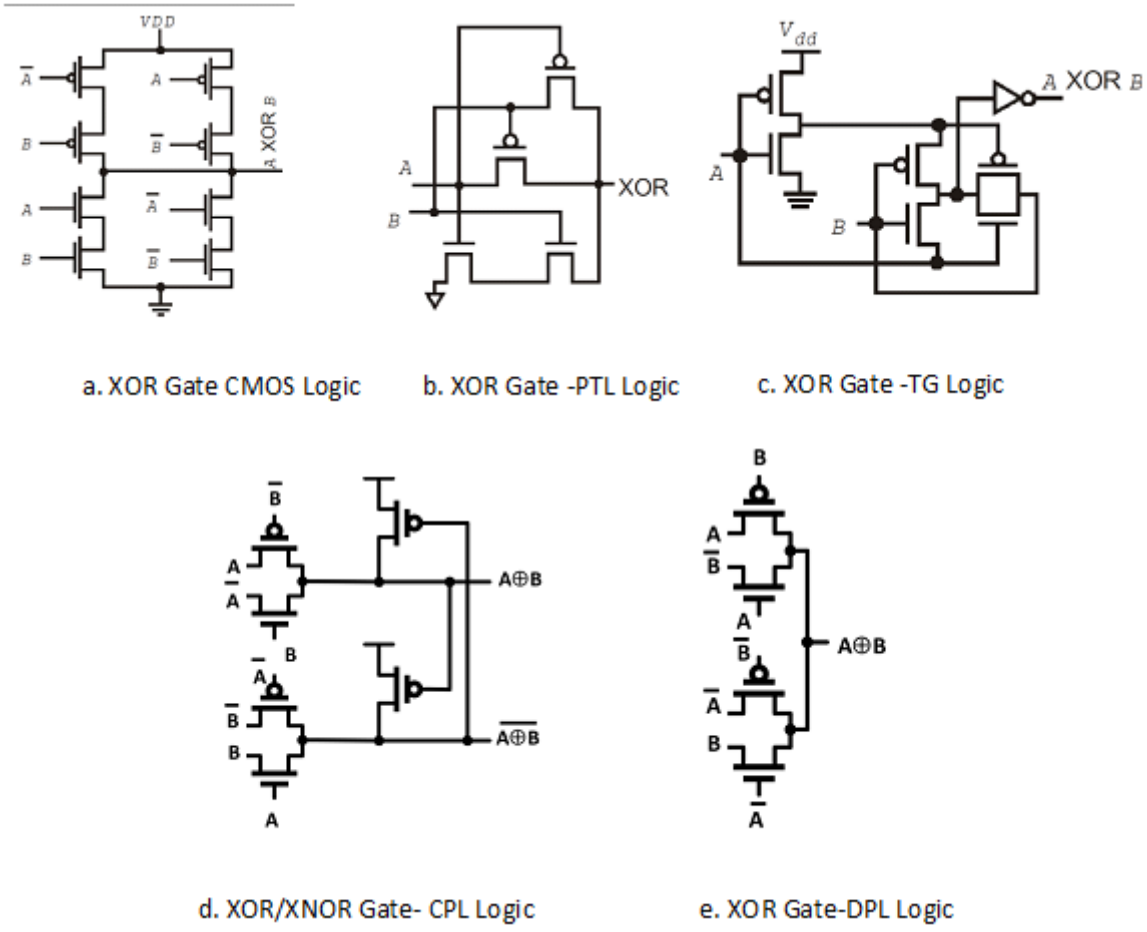
c. AND Gate TG-based

d. NAND/AND Gate CPL-based

e. AND Gate DPL-based

Figure 1

Different traditional approaches for realizing AND logic gate.



a. XOR Gate CMOS Logic b. XOR Gate -PTL Logic c. XOR Gate -TG Logic

d. XOR/XNOR Gate- CPL Logic e. XOR Gate-DPL Logic

Figure 2

XOR Gate Realizing using Different approaches

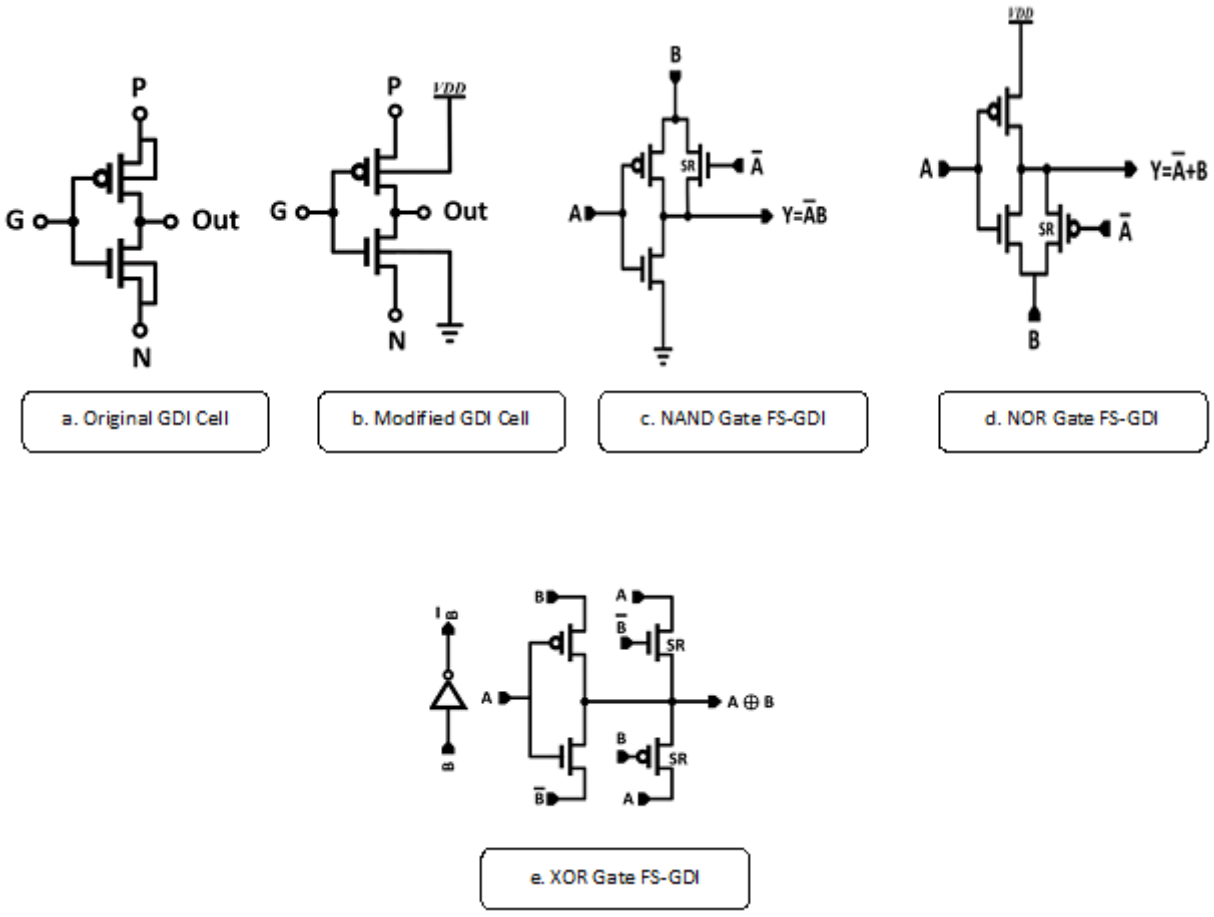


Figure 3

Cell of GDI approach developing, a-Original GDI cell, 2001, b-Modified GDI cell 2010, and d-FS-GDI, 2014.

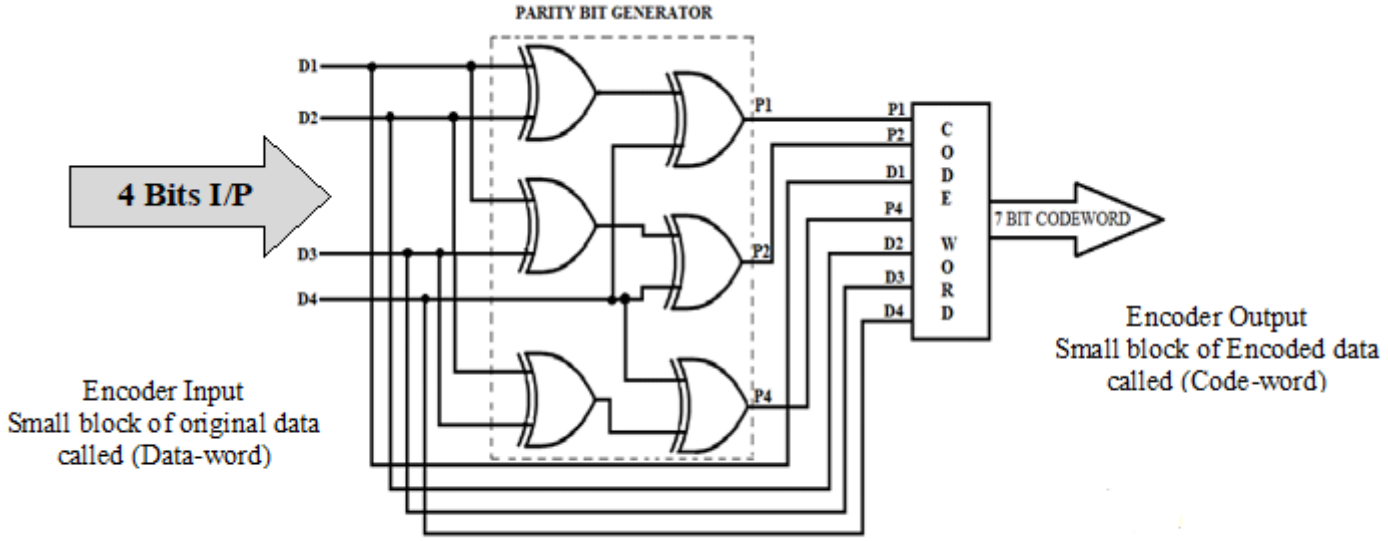


Figure 4

Hamming Encoder Circuit(7, 4) Contents