A low power injection-locked CDR using 28 nm FDSOI technology for burst-mode applications

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Abstract

In this paper, a low-power Injection-Locked Clock and Data Recovery (ILCDR) using 28 nm FDSOI technology is presented. The back-gate auto-biasing of UTBB-FDSOI transistors allows us to create a QRO (Quadrature Ring Oscillator) reducing both size and power consumption. By injecting a digital signal into this circuit, we realize an Injection-Locked Oscillator (ILO) with low jitter. Thanks to the good performance of this oscillator, we can propose a low power ILCDR with low jitter and fast locking time for burst-mode applications. The main novelty consists in the implementation of a complementary QRO based on back-gate control using FDSOI technology in order to realize a simple and efficient ILCDR circuit. With a Pseudo-Random Binary Sequence ($2^7$ PRBS) at 868Mbps, the recovered clock jitter is 18.5 ps (1.6%UI$_{pp}$) and the recovered data jitter is 18.7 ps (1.6%UI$_{pp}$). With a 0.6 V power supply, the power consumption is 4.67 mA (2.8 mW). The estimated Chip size is around 6600 µm$^2$.

1. Introduction

Generally, synchronous data transmission systems send only the data signal to reduce the bandwidth and power consumption. The receiver has to implement a CDR circuit to perform both the extraction of the transmitted data sequence from the noisy received signal and the recovery of the associated clock timing information [1]. The data must be retimed to remove the jitter accumulated during transmission. The clock generated must have a frequency equal to the data rate and a small jitter because it is the main contributor to the retimed data jitter. To have an optimum sampling of the bits, the rising edges of the restored clock must coincide with the midpoint of each bit. In this case, the sampling occurs farthest from the previous and following data transitions, providing a maximum margin for jitter [2].

Indeed, FDSOI 28nm technology allows us to create a complementary inverter by using the back-gate of the transistor to symmetrize its outputs [3]. Complementary inverters allow us to implement back-gate auto-biasing feedback and to realize a QRO with an even number of inverters. By injecting a signal into this circuit, we create an ILO with low jitter [4]. Thanks to the good performance of this oscillator, we can propose a low-cost and low-power ILCDR with a fast-locking time and good jitter for burst-mode applications.

This paper is organized as follows: Section 2 introduces and compares the various types of open-loop CDR. Section 3 presents the circuit implementation of the injection complementary QRO based on the UTBB-FDSOI technology. The proposed ILCDR architecture and the simulation results are described in Section 4, followed by a conclusion of this work in Section 5.

2. Cdr Architectures

CDR can be classified into two major categories. The first structures are using feedback phase tracking like Phase Locked Loop (PLL) or Delay Locked Loop (DLL). These closed-loop architectures are the most
used essentially for their low jitter [1, 2, 5, 6]. The second ones are open loop structures with low power, fast locking time, simple and low-cost design [7].

Open-loop CDR structures aim at local area network, passive optical networks and Serializer/Deserializer applications in which jitter accumulation is not a major problem but need a burst-mode operation to extract a synchronous clock and recover the received data quickly for each asynchronous packet [1, 7, 8, 9].

An open-loop CDR is usually based on a gated oscillator, a high-Q bandpass filter, or an ILO circuit [7]. These circuits are very similar, just one block changes as shown in Fig. 1.

Driven by the recovered clock, the flipflop retimes the incoming data. The variable delay buffer provides an adjustable delay of the input data to align it with the clock edge (the best time is the midpoint of each bit). It can be controlled externally to correct the Process, Temperature, and Voltage (PVT) variations. The edge detector is generally an XOR that will generate pulses at the input data bit frequency that commands the oscillator.

The high-Q filter-based CDR, such as an LC filter, directly samples the clock but its integration on a chip is difficult and there is no input jitter rejection [1, 7]. The gated oscillator circuit aligns this phase by every input data transition, so it also has no input jitter rejection and a strong sensitivity to PVT variations [1].

We propose an ILCDR to enable a fast acquisition time and good jitter tolerance. Indeed, this kind of CDR has an input-jitter-filtering nature as opposed to CDRs based on high-Q filter or gated oscillator [7, 10]. Moreover, when the edge detector output is injected into the ILO, it will force it to lock onto this frequency, allowing some process variation in the oscillator design and thus a better PVT variations tolerance. Indeed, the injection of a periodic signal into an oscillator leads to pulling or locking phenomena [11]. Injection locking means that if an oscillation source is affected by an interference signal whose frequency is very close to its own, its output frequency will be locked at the frequency of the interference signal instead of its own free oscillation frequency [4]. The principle of a simple injection structure is shown in Fig. 2.

A three-stage ring oscillator oscillates at the frequency $f_0$. The introduction of a phase shift $\phi_0$ in this loop modifies the oscillation frequency because the system phase deviates by a value equal to $\phi_0$. Figure 2.(b) shows the change in the oscillation frequency from $f_0$ to $f_1$ induced by the effect of $\phi_0$. Assuming that $\phi_0$ is generated by an injection voltage $V_{inj}$, the system then oscillates at the injection frequency $f_{inj}$ [4].

The ILCDR structure can have a closed-loop, generally built with a PLL, to perform a frequency tracking of the input data and adjust the free-running frequency of the ILO as shown in Fig. 3.

This input frequency tracking system improve the BER of the ILCDR in case of a long sequence of 0 or 1 because the difference between the input data frequency and the free running frequency of the ILO is reduced [7]. Adding a PLL increases the complexity, the cost, the die area, and the power consumption of
the CDR. In this work, we propose to improve the jitter of the standard architecture of the open-loop ILCDR without adding a PLL to remain in the case of a low-power and low-cost design.

3. Injection Complementary QRO

3.1. RO Design

To perform a quadratic demodulation, it is necessary to have at least two 90° phase shifted signals. A VCO enables this operation to be carried out [12]. LC tanks are the most popular circuits to realize a VCO. On the contrary, RO is known to exhibit high phase noise, but this design will address aggressively the size and power consumption reduction. We have proposed a new inverter topology to realize a VCO using FDSOI technology [13].

The access to UTBB (Ultra-Thin Body & Box) transistor Back-Gates offers an extended control of the threshold voltages of the transistors (cf. Figure 4) [14], opening new opportunities to exciting performances. We have proposed a new complementary structure based on a pair of Back-gate cross-coupled inverters offering a fully symmetrical operation of complementary signals, as shown in Fig. 5.

The main idea is as follows: frequently, the NMOS transistor, the faster one, is going to accelerate the conduction of the slower PMOS transistor, and reciprocally. So, connecting the output of each inverter to the back-gate of the other, the faster stage will accelerate the slower one, realizing a symmetrization of the two stages. The complementary outputs are crossing at $V_{DD}/2$. Monte Carlo (MC) simulations exhibit a mean value of $V_{DD}/2 = 500$ mV, and the standard deviation is about $\sigma = 2.7$ mV [13].

This new complementary inverter will offer two other advantages very important for ring oscillator realization. The first one concerns the duty cycle, which has to be close to 50% and low jitter [14]. Secondly, this topology enables an oscillator with an even number of inverters (cf. Figure 6). This latter feature makes it easy to perform a QRO: four identical outputs with the same amplitude and same frequency but with different phases (0°, 90°, 180°, and 270°).

The transient result is shown in Fig. 7, where the complementary outputs are crossed at VDD divided by 2. The 8 single-ended outputs are plotted which produces a clock equally spaced by 45 °. In CDR, the 8-phase output provides the ability to create a variable delay.

3.2. Injection complementary QRO

Figure 8 shows the schematic of the proposed design. The QRO may not oscillate automatically, so it needs a startup design. The complementary signal output for a complementary inverter is a necessary condition for the oscillator to start. The use of NMOS transistors can only pull the voltage down to 0, and the complementary signal can be obtained from the output of the next stage inverter, so a two-stage complementary inverter should be considered to study the start of the oscillator [15].
To make the QRO oscillates normally and obtains a complementary signal pair, the initialization configuration should be to initialize one output of the first stage and the other output of the second stage. At the same time, the injection signal is also transmitted through the two NMOS transistors to obtain the complementary signals.

To make the Reset signal and the injected signal work together and not interfere with each other, it is necessary to use these two signals as the two input signals of a NAND gate. In practice so as not to unbalance the different outputs of the QRO, the same capacitance values C of the Reset transistor will be added to all the other outputs.

According to the principle of injection locking, this structure can expand the range of oscillation frequency. The circuit starts to oscillate when $V_{DD}$ is 0.4 V, and as $V_{DD}$ increases, the locking range becomes larger.

When the oscillation frequency is 868 MHz, the injection locking range can be expanded from 517 MHz to 1.16 GHz, as shown in Figure 9.

Figure 10 compares the relationship between oscillation frequency and phase noise with or without injection signal. Due to thermal noise and flicker noise, the phase error of a free-running QRO will increase randomly compared to an ideal QRO. The injection pulse forces the edge of the output signal to move back to the correct position every injection period, so the phase error no longer accumulates, and the phase noise can be reduced. In contrast, the phase noise measured at 1 MHz is -130 dBc/Hz, which is 45 dB less than the phase noise of no injection signal.

### 3.3. QRO implementation and measurements

The QRO was implemented in 28 nm FDSOI technology (PMOS: 9.1 µm/30 nm, NMOS: 7 µm/39 nm). The layout has been studied with specific care on the symmetries between each inverter, but also on global symmetry regarding QRO outputs using a common centroid design, as depicted in Fig. 11.

Figure 12 illustrates the layout the QRO with a size of 60*40 µm² and Fig. 13 illustrates the complete layout and micrograph of test chip with two QRO and one QCVRO (Quadrature Voltage Controlled Ring Oscillator) not presented in this paper [13].

The test chip measurements exhibit an oscillation frequency of 2.14 GHz for the nominal power supply $V_{DD} = 1$V with a power consumption of 5.9 mA. Figure 14 illustrated the measured complementary outputs of an inverter of the QRO. This result exhibits a 190 MHz oscillation frequency when $V_{DD} = 0.5$V with a power consumption of 0.25 mA (125 µW).

Figure 14 shows that the mean value of the duty cycle is equal to 49.7% (very close to 50%). The symmetrization of the two complementary outputs is quite good. For UHF applications at 868 MHz, the needed power supply is around 0.7 V as shown in Fig. 15. For the final implementation of the receiver, a current starved ring oscillator will be used.
For this first test chip, the oscillation frequency is controlled by the power supply ($V_{DD}$). The tuning range of the oscillation frequency in function of $V_{DD}$ is presented in Fig. 15. We can observe a tuning range linear part from $V_{DD} = 0.6$ V to $V_{DD} = 1$ V, corresponding respectively to an oscillation frequency of $f_{min} \approx 480$ MHz and $f_{max} \approx 2.14$ GHz. The central frequency $f_0 \approx 1.3$ GHz is obtained with $V_{DD} = 0.8$ V for a power consumption of $2.88$ mA (2.3 mW). So, we can deduce the gain of the QRO: $K_{QRO} = 4.3$ GHz/V.

For each value of $V_{DD}$ (i.e. oscillation frequency), we have also measured the power consumption, depicted in Fig. 16. This result shows that this circuit is very efficient for low frequency applications. For example, when $V_{DD} = 0.5$ V for a frequency of 190 MHz, the power consumption is only $0.25$ mA, then $125$ µW. Finally, for ISM 868 MHz applications, the power consumption is around $1$ mW (0.7 V and 1.5 mA).

With the existing layout of the QRO, the area of the ILCDR chip is estimated to be about $6600$ µm² based on the structure of the CDR and the size of the MOS transistors.

4. Proposed ILCDR

4.1. Timing analysis of the proposed ILCDR

Figure 17 depicts a simplified block diagram of the injection CDR. The input signal is a Pseudo-Random Binary Sequence ($2^7$ PRBS) at 868Mbps. After the pulse generator, a pseudo-random pulse signal is obtained at the rate multiplied by 2, which is 1.736 Gbps. After injecting the pulse signal into the complementary oscillator, it outputs a periodic signal with a frequency of 868 MHz, which is the recovered clock signal. The recovered data signal is the output signal with a rate of 868 Mbps after sampling.

Equation 1 indicates the behavior of the injection current pulse:

\[
    x(t) = \begin{cases} 
    I_{injection} & 0 < t < \gamma \\
    0 & \gamma < t < T 
    \end{cases} 
\]  

(1)

where $\gamma$ denotes the pulse width and $T$ denotes the period of the injected pulse [16]. Experimental results on the 8 quadrature-phase output signals of the complementary RO show that the maximum value of $\gamma$ needs to be less than $0.5T$ to achieve an acceptable jitter. Indeed, injection intensity is related to the duty cycle of the injection signal, which affects the injection performance. The best pulse signal width obtained to minimize the jitter of the ILCDR system is equal to a quarter bit period ($T_B/4$) as shown in Fig. 18.

4.2. Architecture

Figure 19 illustrates the architecture of the proposed full-rate ILCDR, which includes a pulse signal generation block consisting of a DFF and an XNOR gate, an injection block, and a complementary RO block. The incoming data, NRZ code, whose power spectral density is zero at the frequency component of the clock or its multiples, the clock signal cannot be extracted. By passing the NRZ data through a DFF
and an exclusive-OR gate, RZ data can be obtained from which the clock frequency components may be extracted [17]. Injecting the pulse signal into a complementary ring oscillator, it outputs eight periodic signals with the same rate and different phases. One of these 8-phases signals is selected as the clock signal which contains a variable phase, so a variable delay consisting of several inverters is no longer required, which could simplify the circuit structure and thus reduce the power consumption and the chip size of the ILCDR. One of the 8 phases is manually selected in the simulation stage and is sent to the flipflop. A binary selector and an 8-to-1 MUX will be used to select the phase for the fabrication stage. The principle of manual selection is to obtain smaller jitter. Indeed, the output signal makes the injection pulse width matches Tbit/4 minimizing the jitter of CDR circuit. The input data is XNORed with the output signal of the DFF to obtain a pulse signal with 2 times the bit rate. The recovery data is obtained after the decision circuit DFF.

In general, the QRO takes advantage of the back-gate control structure that reduces the error in each transition. Random jitter (thermal noise, flicker noise, etc.) can be corrected periodically using injection techniques. Furthermore, a DFF was used to implement the functions of pulse signal generation and recovery data sampling simultaneously.

4.3. Simulated results with a periodic input signal

The transistor-level model was implemented using STMicroelectronics 28nm UTBB-FDSOI. The proposed ILCDR achieves a wide operation range of 868Mbps in a Cadence Analog Design Environment with a 0.6V supply voltage. Continuous and burst input data at the same rate are tested respectively.

Figure 20 shows the eye diagram of the recovered clock signal at 868 MHz with the injection using transient simulation by more than 10,000 cycles. The recovered clock peak-to-peak jitter for continuous input is 11.2 ps (1.0%UI). Considering signals without errors, the locking range of this ILCDR is 762 M-1194 Mbps (49.8% of 868 Mbps). The results show the jitter is successfully reduced and a wide locking range is realized thanks to the symmetrization of the outputs signals of the QRO in the ILCDR.

Figure 21 shows the peak-to-peak jitter in the function of the frequency deviation. Within the range of frequency variation of 20 MHz, p-p jitter less than 3.8%UI is feasible. Figure 22 illustrates phase noise with or without injection periodic signal. Phase noise for the injection circuit is -118 dBc/Hz@1MHz, which is a reduction of 44 dB. The rms jitter of the clock signal is 1.5ps by phase noise conversion. The circuit consumes 3.0 mW of total power, of which 0.2 mW is dissipated in the QRO, 0.5 mW in the DFF and the logic gates, and 2.3 mW in the buffer circuit.

4.4. Simulated results with a random input signal

Based on over 10,000 cycles of transient simulations, Fig. 23 shows the jitter of the recovered clock and recovered data for the PRBS7 input data. The jitter is 18.5 ps (1.6%UI) of the clock and 18.7 ps (1.6%UI) of the PRBS7 data.
The recovered clock and data can meet the p-p jitter requirements of 5.3% UI and 2.5% UI, respectively, within the frequency error of 5 MHz indicated in Fig. 24. The locking range is 850–925 Mbps without errors of the input PRBS7, which is 8.6% of 868 Mbps. In the case of random signal input, the power consumption of the total circuit is 2.8 mW, of which the oscillator consumes 0.2 mW, the buffer circuit consumes 2.3 mW and the other modules consume 0.3 mW.

TABLE II CDR PERFORMANCE SUMMARY AND COMPARISON

<table>
<thead>
<tr>
<th>[18]</th>
<th>[19]</th>
<th>[20]</th>
<th>[21]</th>
<th>[22] *</th>
<th>This work</th>
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<td>Technology (nm)</td>
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<td>28</td>
<td>40</td>
<td>28</td>
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<td>Half rate</td>
<td>Half rate</td>
<td>Half rate</td>
<td>Full rate</td>
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<td>Injection</td>
<td>PLL</td>
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<td>Injection</td>
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<td>Supply Voltage (V)</td>
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<tr>
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<td>p-p Jitter (ps)</td>
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<td>Power Dissipation (mW)</td>
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<td>Power efficiency (pJ/bit)</td>
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<tr>
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<td>0.03</td>
<td>N/A</td>
<td>N/A</td>
<td>0.10</td>
</tr>
</tbody>
</table>

* Clock recovery circuit
** Estimated value

5. Conclusion And State Of The Art Comparisons

Table II summarizes the performance of this work and some other CDRs recently published in the literature.

Thanks to FDSOI technology, we proposed to implement a novel cross-coupled back-gate technique to improve analog and mixed signal cells to decrease the surface of the integrated circuit. Thanks to this technique, we have implemented a QRO based on complementary logic and complementary inverters. This kind of QRO is very efficient for low power and low frequency applications. Based on the back-gate structure, the proposed ILCDR simplifies the design significantly and therefore greatly reduces power consumption and surface. The ILCDR extracts an 868 MHz clock signal for the same bit rate as random...
input data. Featuring back-gate and injection technology, it exhibits a desirable jitter performance. The peak-to-peak jitter is 18.5 ps and 18.7 ps for the recovered clock and data signal, respectively. The power consumption for the ILCDR is 2.8mW. It dramatically reduces the power consumption and the surface area and performs with remarkable energy efficiency. The next step is to implement an external reference frequency PLL to improve the stability of the circuit in the fabrication process.

**Declarations**

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**Declaration of competing interest**

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

**Editor requirements**

Moreover, the email address mentioned in the submission system and in the manuscript file is the same.

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Yuqing Mao wrote the main manuscript text and prepared all figures. All authors reviewed the manuscript.

**References**


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Architecture of the proposed ILCDR

dx : 11.24ps
Figure 20

Eye diagram of recovered clock at 868 MHz

![Eye diagram of recovered clock at 868 MHz](image)

Figure 21

The peak-to-peak jitter vs frequency deviation
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Phase noise of CDR in the function of relative frequency
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