A Novel Approach to Model Threshold Voltage and Subthreshold Current of Graded-Doped Junctionless-Gate-All-Around (GD-JL-GAA) MOSFETs

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A novel approach to model Threshold Voltage and Subthreshold Current of Graded-Doped Junctionless-Gate-All-Around (GD-JL-GAA) MOSFETs

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Abstract- This present article interprets the analytical models of central channel potential, the threshold voltage, and subthreshold current for Graded-Doped Junctionless-Gate-All-Around (GD-JL-GAA) MOSFETs. The parabolic approximation equation with appropriate boundary conditions has been adopted to solve the 2D Poisson's equation for determining the central channel potential. The minimum channel potential is obtained by potential channel expression, and it is utilized to determine the threshold voltage and subthreshold current by using the Drift-Diffusion method. The behaviour of GD-JL-GAA MOSFETs has been examined by varying physical device parameters such as doping concentration (N_{Dn}), channel thickness (t_{si}), oxide thickness (t_{ox}), and channel length ratio ($L_1: L_2$). The mathematical analysis shows that the nominal gate leakage current in GD-JL-GAA MOSFETs due to high graded abrupt junction inside the channel region. The analytical model results have been verified with simulation data extracted from a TCAD simulator.

Keywords- Junctionless MOSFETs, Gate-all-around (GAA), Graded Doping (GD), Threshold Voltage (V_{TH}), and Subthreshold Current.

1. Introduction

The junctionless (JL) field-effect transistor (FET) has been studied as a most promising alternative device for MOSFETs in nanometre regime [1-2]. Junctionless MOSFET is a device that has no junctions between source/drain and channel. By the merit of their junction free nature, JL devices mitigate process demurs such as abrupt junctions and low thermal budget. The working principle of JL MOSFET is based on the bulk conduction mechanism instead of surface conduction as in conventional MOSFETs. The junctionless transistor has several advantages such as reducing short channel effects (SCEs), high I_{ON}/I_{OFF} ratio, nearly ideal subthreshold slope (60mv/decade), and offer low series resistance between the source and drain [3]. The multigate structure has been proposed to improve gate control over channels and diminished SCEs, such as double gate, triple gate, surrounding gate, and π gate [4].

Multigate JLFETs acquire enhanced mobility, better scalability, higher driving current, good switching characteristics, and better trans-conductance than the conventional MOSFETs. Consequently, many researchers [5-14] have proposed junctionless Double-gate (JL-DG) FETs. Chiang et al. [5] investigated the bulk conduction-based analytical threshold voltage model for double-gate short channel (JL-DG) FETs. It was illustrated that JL-DG FETs exhibit better performance than junction based DG-MOSFETs in terms of DIBL, threshold voltage roll-off, and subthreshold slope. Jin et al. [6] proposed a subthreshold current model for symmetric and asymmetric short channel DG-JL-MOSFETs. They demonstrated the variation of subthreshold characteristics caused by structure asymmetry. The enhancement of carrier transport efficiency is found in the dual-material gate-engineering device [7]. Dual material gate (DMG)-based devices are constructed using different metals with different work functions as gate electrodes. DMG structures have been proposed in DG-JL and surrounding gate all around JL FETs to optimized electrical characteristics [8-9]. Wang et al. [10] proposed the subthreshold current model for DM-DG-JLFETs. Agarwal et al. [11] derived a 2D analytical model for the surface potential of DM-DG-JLFETs. Furthermore, they have derived the expression of threshold voltage for the device. Kumari et al. [12] investigated a 2D analytical model for the subthreshold current of asymmetric DM-DG-JLFETs. Further, they have illustrated the analog and digital performance of DM-DG-JLFETs. Singh et al. [13] reported DG – JLFETs that incorporate dielectric pockets at the source and drain side. They have demonstrated that DP-DG-JLFETs exhibit improved ION/IOFF drain current ratio, subthreshold swing characteristics, and DIBL over conventional DG-JLFETs. Gola et al.

[14] investigated the effect of substrate bias voltage and induced surface potential on the threshold-voltage of Tri-gate junctionless FETs (TG-JLFETs). In specific, gate-all-around junctionless FETs (GAA-JLFETs) have been reported as promising structures for high-performance devices that considered their gate voltage controllability, exciting scalability, and improved carrier transport mechanism [15-16]. Trivedi et al. [17] investigated reliability issues of dual gate material (DMG) and single gate metal (SGM) junctionless accumulation mode surrounding gate (JAM-SG) FETs. They have reported an effect of interface charges on the device performance of SGM and DGM-JAM-FETs for different temperature variations by simulation results. Abhinav et al. [18] investigated surface potential for junctionless cylindrical surrounding gate (JL-SCG) FETs.

The kinds of literature discussed above are based on uniform doping concentration. Various channel engineering has been reported in JLFETs to deal with SCEs, mobility, and hot carrier degradation effects [5-14]. Kumari et al. [19] analyzed an empirical model for non-uniform doped symmetrical JL-DG MOSFETs. They explored different parameters such as threshold voltage, drain current, subthreshold slope, and DIBL for different peak doping concentrations. Kumari et al. [20] proposed the subthreshold model of Gaussian doped channel double gate JLFETs, including source/drain depletion length. All discussed channel engineering is based on the vertical channel doping profile. Few researchers have reported lateral channel engineering structures to deal with SCEs, mobility, and hot carrier effects [21-22]. Duksh et al. [23] formulated an analytical model of Graded Channel Double gate JLFETs (GC-DG-JLFETs). They derived the expression of subthreshold current, subthreshold swing, and threshold voltage. Based on a literature survey, till now, the analytical modeling of central channel potential, the Threshold voltage (V_{TH}), and Subthreshold current of Graded-Doped Junctionless-Gate-all-around (GD-JL-GAA) MOSFETs have not been derived.

This article has proposed the analytical modeling of Centre channel-potential of Graded-Doped Junctionless-Gate-all-around (GD-JL-GAA) MOSFETs using the Poisson Equation with suitable novel boundary conditions. There is the minimum centre channel potential found in the L_1 channel region due to low doping concentration. The Threshold voltage (V_{TH}) and Subthreshold current are obtained using the minimum centre channel potential. The analytical modeling results have been verified through the TCAD simulation results, where they found excellent agreement between mathematical and simulation results. In

section II, our proposed device structure is defined with physical parameters. The analytical modeling of Centre channel Potential, Threshold Voltage (V_{TH}), and Subthreshold Current are derived in Section III. The model variation is written in Section IV and, in the end, concluded our proposed structure in Section V.

2. Device Structure

The schematic view of the GD-JL-GAA MOSFET structure is shown in Fig. 1. The channel region is wrapped by a thin oxide layer and over deposited the gate metal. The channel region is divided into two equal parts of length L_1 and L_2, as shown in Fig. 1(b). The channel length L_1 and L_2 are doped with two different doping concentrations, N_{D1} and N_{D2}, respectively. The drain side L_2 region doping concentration is higher than the source side L_1 region doping concentration in this device. The physical parameters of the proposed GD-JL-GAA MOSFET are listed in table 1.

3. Modeling details

3.1 Channel potential modeling:

The channel potential shows no variations with the angular (θ) axis. The channel potential $\psi(r,z)$ of the GD-JL-GAA MOSFET can be obtained by solving the 2D Poisson's equation in the cylindrical coordinate as [24]:

$$\frac{\partial^2\phi_n(r,z)}{\partial r^2}+\frac{1}{r}\frac{\partial^2\phi_n(r,z)}{\partial r^2}+\frac{\partial^2\phi_n(r,z)}{\partial z^2}=-\frac{qN_{Dn}}{\epsilon_{si}} \quad (1)$$

Where, $n = 1\ and\ 2$ are used for channel regions 1 and 2, respectively. The potential distribution in all the two-channel regions are written as a parabolic approximation:

$$\phi_n(r,z) = C_{0n}(z) + C_{1n}(z)r + C_{2n}(z)r^2 \quad (2)$$

The coefficients $C_{0n}(z), C_{1n}(z)$, and $C_{2n}(z)$ are obtained by using following the boundary conditions.

$$\frac{\partial\phi_n(r,\ z)}{\partial r}\Big|_{r=\frac{t_{si}}{2}}=\frac{\varepsilon_{ox}}{\epsilon_{si}}\frac{V_{Gn}-\psi_n(z)}{t_{eff}} \quad (3)$$

$$\frac{\partial \phi_n(r,\ z)}{\partial r}|_{r=\frac{t_{si}}{2}} = 0 \tag{5}$$

Where,

$$t_{eff} = \frac{t_{si}}{2}\ln\left(1+\frac{2t_{ox}}{t_{si}}\right) \tag{6}$$

$$V_{Gn} = V_{gs} - V_{fbn} \tag{7}$$

$$V_{fbn} = \phi_M - \left(\chi_{Si} + \frac{E_g(si)}{2} - \mathrm{q}ln\left(\frac{N_{Dn}}{n_i}\right)\right) \tag{8}$$

Now, the parabolic approximation equation coefficients are obtained by using the Eq. (2) and above boundary conditions for nth channel potential as:

$$C_{0n}(z) = \phi_n(z) \tag{9}$$

$$C_{1n}(z) = 0 \tag{10}$$

$$C_{2n}(z) = \frac{\varepsilon_{ox}}{\epsilon_{si}t_{si}t_{eff}}\left(V_{Gn} - \frac{(\phi_n(z)+\frac{\varepsilon_{ox}t_{si}}{4\epsilon_{si}t_{eff}}(V_{Gn})}{1+\frac{\varepsilon_{ox}t_{si}}{4\epsilon_{si}t_{eff}}}\right) \tag{11}$$

By utilizing the above Eqs. (9) – (11) in Eq. (2), and solving the Eq. (1) using the obtained condition from Eq. (2) as $\phi_{Cn}(z)$:

$$\frac{\partial^2\phi_{Cn}(z)}{\partial z^2} - \frac{(\phi_{Cn}(z)-\alpha_n}{\lambda^2}=0 \tag{12}$$

Where,

$$\lambda = \sqrt{\frac{\epsilon_{si}t_{si}+\epsilon_{ox}}{4\epsilon_{ox}}} \tag{13}$$

$$\alpha_n = \frac{qN_{Dn}\lambda^2}{\epsilon_{si}} + V_{Gn} \tag{14}$$

By solving the Eq. (12), the channel potential of the channel regions L_1 and L_2 can be obtained as:

$$\phi_{C1}(z) = A_1 e^{\frac{z}{\lambda}} + B_1 e^{-\frac{z}{\lambda}} + \alpha_1 \tag{15}$$

$$\phi_{C2}(z) = A_2 e^{\frac{(z-L_1)}{\lambda}} + B_2 e^{\frac{-(z-L_1)}{\lambda}} + \alpha_2 \tag{16}$$

The above equations' coefficients are obtained (for n=1 and 2) using the following boundary conditions.

$$\phi_{C1}(0,0) = Vbi_1 \tag{17}$$

$$\phi_{C2}(0, L) = Vbi_2 + V_{ds} \tag{18}$$

$$\phi_{C1}(0, L_1) = \phi_{C2}(0, L_1) \tag{19}$$

$$\frac{\partial \phi_{C1}(z)}{\partial z}|_{z=L_1} = \frac{\partial \phi_{C2}(z)}{\partial z}|_{z=L_1} \tag{20}$$

Where,

$$Vbi_1 = V_t ln\left(\frac{N_{D1}}{n_i}\right) \tag{21}$$

$$Vbi_2 = V_t ln\left(\frac{N_{D2}}{n_i}\right) \tag{22}$$

$$A_1 = \frac{(Vbi_2 + V_{ds} - \alpha_2) - (\alpha_1 - \alpha_2) cosh\left(\frac{L_2}{\lambda}\right) - (Vbi_1 - \alpha_1) e^{-\frac{L}{\lambda}}}{2 sinh(\frac{L}{\lambda})} \tag{23}$$

$$B_1 = \frac{(Vbi_1 - \alpha_1) e^{\frac{L}{\lambda}} - (Vbi_2 + V_{ds} - \alpha_2) + (\alpha_1 - \alpha_2) cosh\left(\frac{L_2}{\lambda}\right)}{2 sinh(\frac{L}{\lambda})} \tag{24}$$

$$A_2 = A_1 e^{\frac{L_1}{\lambda}} + \frac{(\alpha_1 - \alpha_2)}{2} \tag{25}$$

$$B_2 = B_1 e^{-\frac{L}{\lambda}} + \frac{(\alpha_1 - \alpha_2)}{2} \tag{26}$$

The minimum channel potential location (z_{min}) in the z direction can be obtained as:

$$\frac{\partial \phi_{Cn}(z)}{\partial z} = 0; \tag{27}$$

$$Z_{min} = \frac{\lambda}{2} ln(\frac{B_n}{A_n}) \tag{28}$$

Using the Eq. (28) into Eqs. (15) and (16), the minimum channel potential $\psi_{Cn(Z_{min})}$ can be found as:

$$\psi_{Cn(Z_{min})} = 2\sqrt{A_n B_n} + \alpha_n \tag{29}$$

3.2 Threshold Voltage (V_{TH}) formulation:

The minimum gate voltage is required to apply in the device to become in ON-state is known as the threshold voltage. The threshold voltage (V_{TH}) for the GD-JL-GAA MOSFETs has been formulated when the minimum channel potential equals the Fermi potential value (V_{bi}) [23, 25]. According to equation (29), the minimum channel potential occurred in region 1. Thus, the threshold voltage (V_{TH}) expression can be written as:

$$\phi_{C1(z_{min})|_{V_{gs}=V_{TH}=Vbi_1}} \tag{30}$$

$$V_{TH} = \left[\frac{-q+\sqrt{q^2-4pr}}{2p}\right] \tag{31}$$

Where,

$$p = \frac{2-2cosh\left(\frac{L}{\lambda}\right)}{sin^2h(\frac{L}{\lambda})} \tag{32}$$

$$q = \frac{(a_1-a_2)(e^{\frac{L}{\lambda}}-1)+(a_1-a_2+a_3-1)(1-e^{-\frac{L}{\lambda}})}{sin^2h(\frac{L}{\lambda})} - (2a_3) \tag{33}$$

$$r = \frac{(a_1-a_2)^2+2(a_1-a_2)a_3 cosh(\frac{L}{\lambda})+{a_3}^2}{sin^2h(\frac{L}{\lambda})} + (a_3)^2 \tag{34}$$

$$a_1 = Vbi_2 + V_{ds} - \frac{qN_{D2}\lambda^2}{\epsilon_{si}} + V_{fb2} \tag{35}$$

$$a_2 = \left(\frac{qN_{D1}\lambda^2}{\epsilon_{si}} - \frac{qN_{D2}\lambda^2}{\epsilon_{si}} + V_{fb2} - V_{fb1}\right) cosh(\frac{L_2}{\lambda}) \tag{36}$$

$$a_3 = \frac{qN_{D1}\lambda^2}{\epsilon_{si}} - Vbi_1 - V_{fb1} \tag{37}$$

3.3 Subthreshold Current:

The calculation of subthreshold current based on minimum channel potential (similar from [26]) can be evaluated by using the drift-diffusion equation as:

$$I_{ds} = \frac{2\pi q \mu \frac{t_{si}}{2} N_i V_t \left(1 - e^{-\frac{V_{ds}}{V_t}}\right)}{\int_0^{L_1} \frac{dz}{\int_0^{\frac{t_{si}}{2}} e^{\left(\frac{q\psi_{C1}(z_{min})}{KT}\right)} dr} + \int_{L_1}^{L} \frac{dz}{\int_0^{\frac{t_{si}}{2}} e^{\left(\frac{q\psi_{C2}(z_{min})}{KT}\right)} dr}} \quad (38)$$

4. Model validation and Discussion:

In this section, the proposed analytical modeling of GD-JL-GAA MOSFETs have been presented and validated with TCAD device simulator results. The following models are incorporated in the proposed GD-JL-GAA MOSFETs structure during the simulation at room temperature. Such as Concentration-dependent mobility model, High field-saturation mobility model, Lombardi (CVT) mobility, Fermi-Dirac, and Shockley-Real-Hall (SRH) recombination with auger models [27]. The quantum effects have been ignored in this work, as the results are unnecessary for more comprehensive than 5nm channel thickness and 10nm channel length [28]. The constant current method is used for the threshold voltage extraction. Fig. 2 demonstrates the electrostatic channel potential along the channel length for graded-doped and uniformly doped JL-GAA MOSFETs. As we observe from the figure, central channel potential is found to pull down in graded channel devices, suggesting that the source side barrier height increased. It is also expressed that the minimum potential transfers towards the source side in the graded-doped (GD) device. As a result, the GD-JL-GAA MOSFETs should have better immunity for short channel effects (SCE's) than uniformly doped JL-GAA MOSFETs. Fig. 3 illustrates the variations of central channel potential along the channel length for various ratios of L_1:L_2. It is executed from the figure that the source channel's barrier height increases with the change in the ratio of L_1:L_2. It occurred due to an increase in the length of L_1. The minimum central potential moves towards the drain side because of increased doping concentrations on the drain side. Thus, the L_1:L_2 ratio may be useful as an extra parameter for optimizing the device's threshold voltage. Fig. 4 shows the variation of central channel potential against the channel length. It is seen that the barrier height increases at the source end as channel length increases because the gate control over the channel charges increased. Thus, the long channel length

shows better immunity towards SCE's. Fig. 5 displays the channel potential variation against the channel length for distinct values of channel thickness. It has been observed from the figure, when the channel thickness increases, the minimum channel potential is pulled up, which indicates that the gate control over the channel losses gradually. It happened because a smaller thickness of the channel would be more efficient in achieving volume depletion at zero gate voltage. Thus, GD-JL-GAA MOSFETs have better immunity towards SCE's for a channel having a low thickness. Fig. 6 demonstrates the channel potential with the channel length for different values of oxide thickness. It is noticed that the source channel barrier height lowers as the oxide thickness increments, which indicates that the gate control over the channel charges losses gradually with the thickness of the oxide. Thus, the minimum oxide thickness is better for immunity towards SCE's. Fig. 7 present the variation in threshold voltage along the channel length for unlike value of doping concentration in region 1 of the channel, N_{D1}. It has been observed from figure 7 that the threshold voltage is higher at a lower doping concentration of region 1. Higher threshold voltage indicates a more considerable barrier height between the source and channel for low doping concentration of region 1 than high doping concentration. As a result, GD-JL-GAA MOSFETs are more towards the SCE's mitigation. Fig. 8 illustrates the threshold voltage against the channel length for various values of channel thickness (t_{si}). As we have discussed in figure 5, as the t_{si} increases, the gate gradually loses its control over the channel charge. This effect attributes to a reduced threshold voltage for a higher t_{si}, as demonstrated in figure 8 that degrades subthreshold characteristics. Thus, a thinner channel is required to diminish leakage current. Fig. 9 shows the variation of threshold voltage with oxide thickness along the channel length. This figure reflects that the gate control over the channel charges decreases as oxide thickness increases, leading to the reduced threshold voltage. Fig. 10 displays the subthreshold current with gate voltage for the uniformly doped and graded-doped (GD) JL-GAA MOSFETs. It is observed from figure 10 that the OFF-state current (I_{OFF}) reductions with a drop in the doping concentration of region 1 of the channel, N_{D1}. It happened because of the higher source to channel barrier height for the channel-modulated device, as seen in figure 2. Hence, the leakage current is insignificant in GD-JL-GAA MOSFETs. Fig. 11 demonstrates the variation of subthreshold current against gate voltage for distinct channel length values. This plot reflects that the I_{OFF} significantly decreased when the channel length is increased from 20nm to 40nm. It occurred due to the barrier height being raised between the source and channel. Hence, the SCE is immune at a longer channel length. Fig. 12 illustrates the

variation of subthreshold current against gate voltage, unlike channel thickness values for graded channels. It is noticed that the gate loses its control over the channel for the thicker channel, and it is leading to a higher gate leakage current. Further, it is also observed from Fig. 13 that more increased oxide thickness leads to a significant gate leakage current due to loss of gate controllability.

5. Conclusion

In this article, the channel potential, the Threshold voltage, and Subthreshold current of Graded-Doped Junctionless-Gate-all-around (GD-JL-GAA) MOSFETs have been presented. The impact of different device physical parameters such as L_1 region doping concentration, channel length, channel thickness, oxide thickness, and channel length ratio L_1:L_2 have been examined. The L_1 region doping concentration and channel length ratio L_1:L_2 have been found as essential physical parameters that can be changed for optimizing device performance. Simulation results have validated the model results.

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Conflict of Interest

The authors declare that there is no conflict of interest regarding the publication of this paper.

Author Contribution

All authors have made substantial contributions to the conception and design, or acquisition of data, or analysis and interpretation of data; have been involved in drafting the manuscript or revising it critically for important intellectual content; and have given final approval of the version to be published. Each author has participated sufficiently in the work to take public responsibility for appropriate portions of the content. All authors read and approved the final manuscript.

Availability of data and material

The data and material are available within the manuscript.

Compliance with ethical standards

The authors declare that all procedures followed were in accordance with the ethical standards.

Consent to participate

All the authors declare their consent to participate in this research article.

Consent for Publication

All the authors declare their consent for publication of the article on acceptance.

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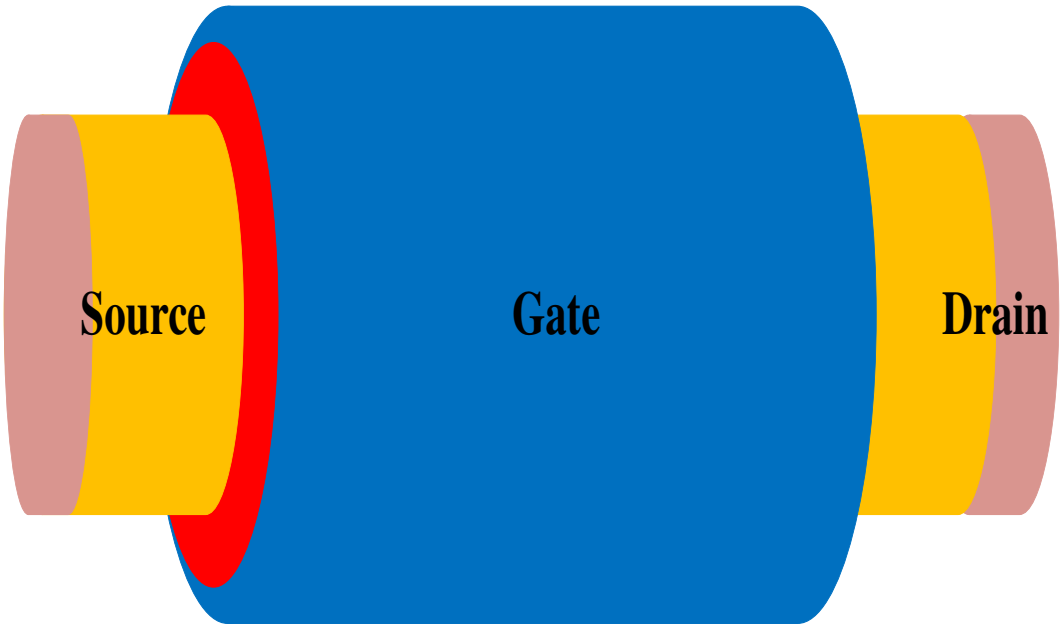
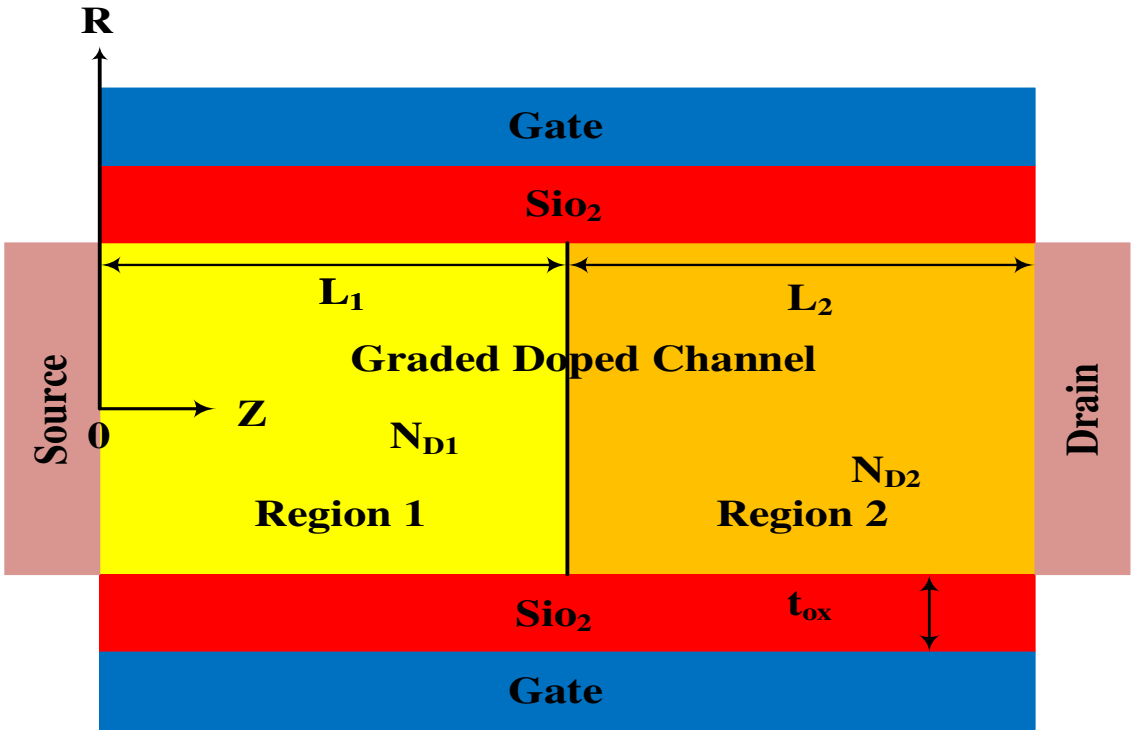


(a)



(b)

Fig 1: Schematic structure of (a) 3D-view and (b) 2D-view of GD-JL-GAA MOSFETs

Table- I: The physical parameters of GD-JL-GAA MOSFET device used for the simulations and analytical models.

Symbol	Parameter	Value
L_{ch}	Channel Length	20-40nm
t_{si}	Channel Thickness	8-12nm
t_{ox}	Oxide Thickness	1-3nm
N_{D1}	Source side doping concentration	$6\times10^{18}cm^{-3}$-$1\times10^{19}cm^{-3}$
N_{D2}	Drain side doping concentration	$1\times10^{19}cm^{-3}$
n_i	Intrinsic carrier concentration	$1.45\times10^{10}lcm^{-3}$
ϕ_M	Gate Metal-work function	5.1eV

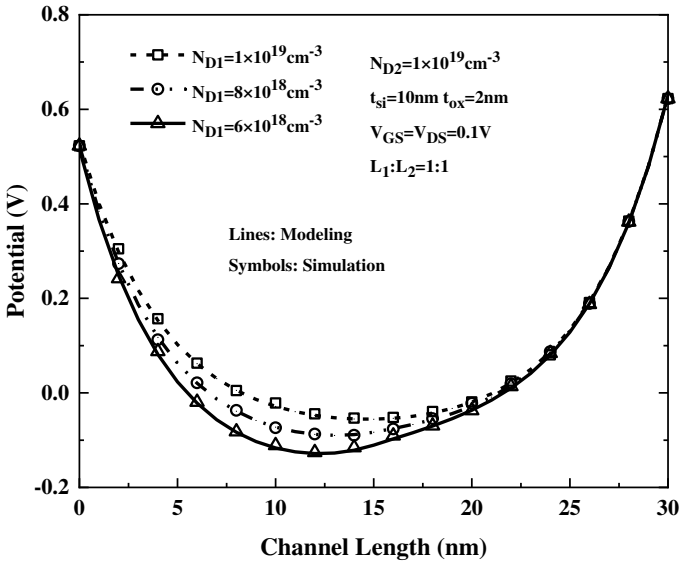


Fig. 2: Channel potential variation along the channel length for different doping concentrations.

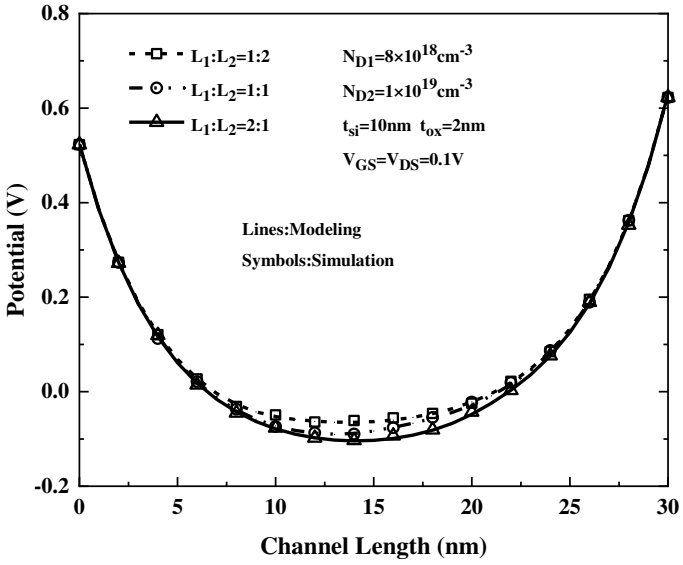


Fig. 3: Channel potential variation along the channel length for different channel length ratio L1:L2.

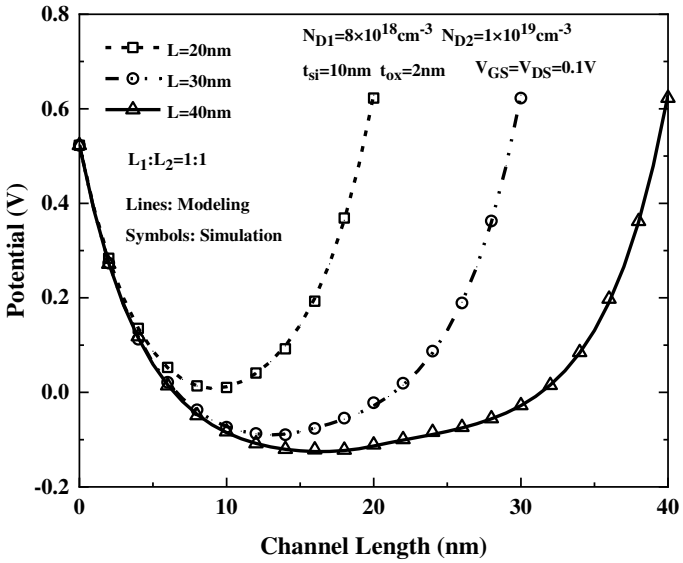


Fig. 4: Channel potential variation along the channel length for various channel length.

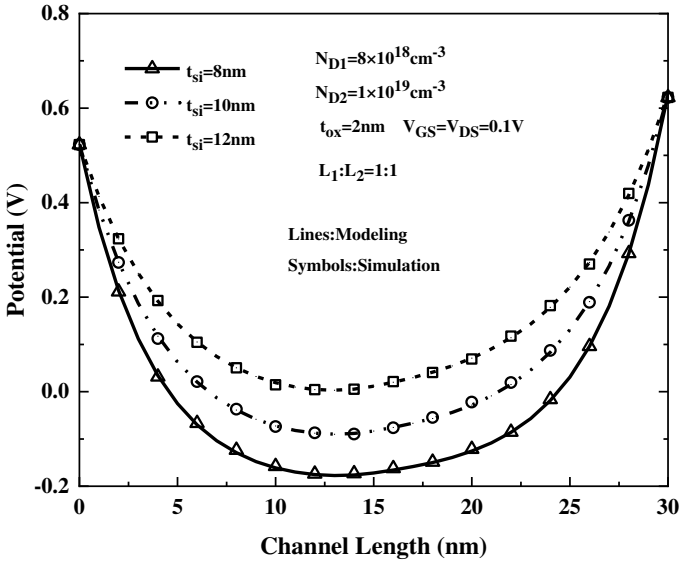


Fig. 5: Channel potential variation along the channel length for different channel thickness.

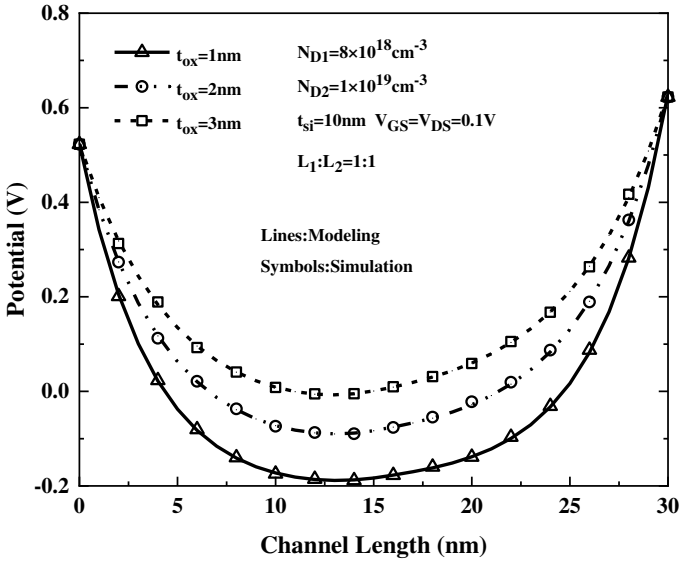


Fig. 6: Channel potential variation along the channel length for different oxide thickness.

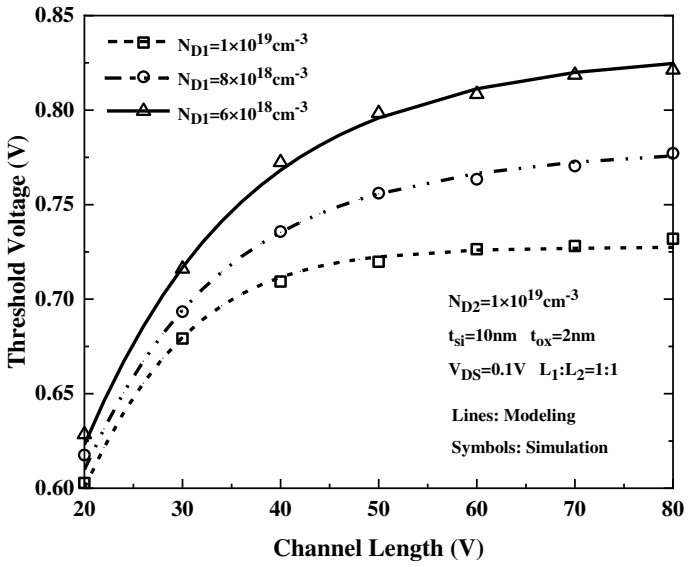


Fig. 7: Threshold voltage variation along the increasing channel length for different doping concentrations

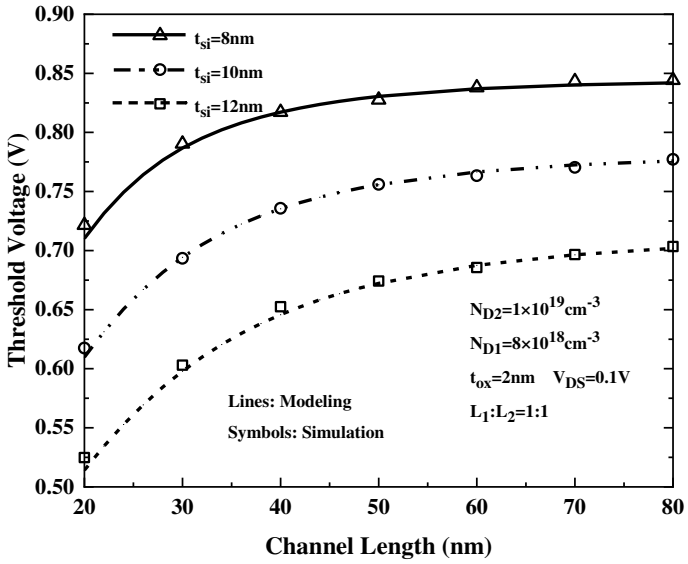


Fig. 8: Threshold voltage variation along the increasing channel length for different channel thickness

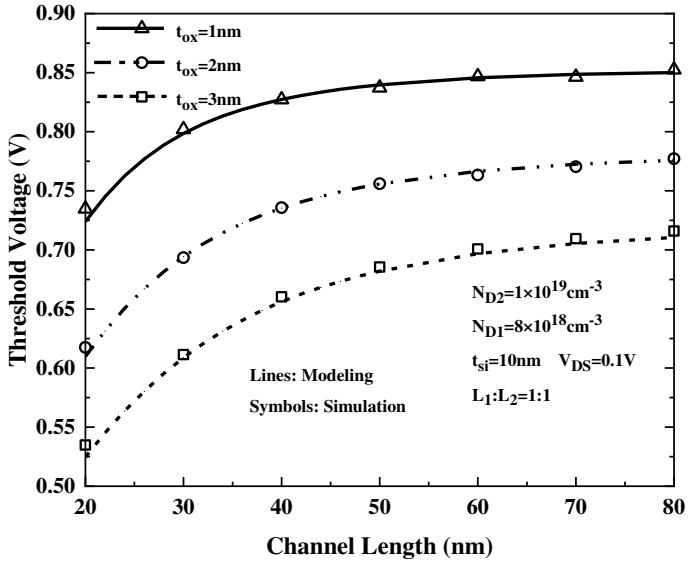


Fig. 9: Threshold voltage variation along the increasing channel length for different oxide thickness

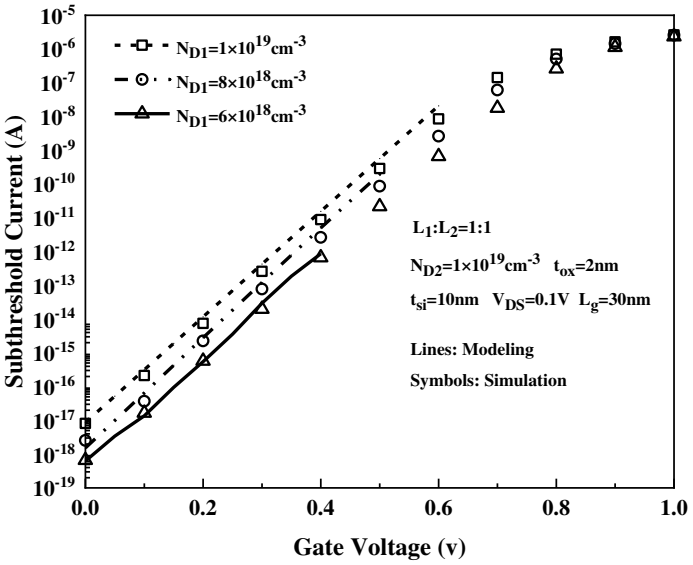


Fig. 10: Variation of Subthreshold current (I_{DS}) with gate voltage (V_{GS}) for different doping concentrations

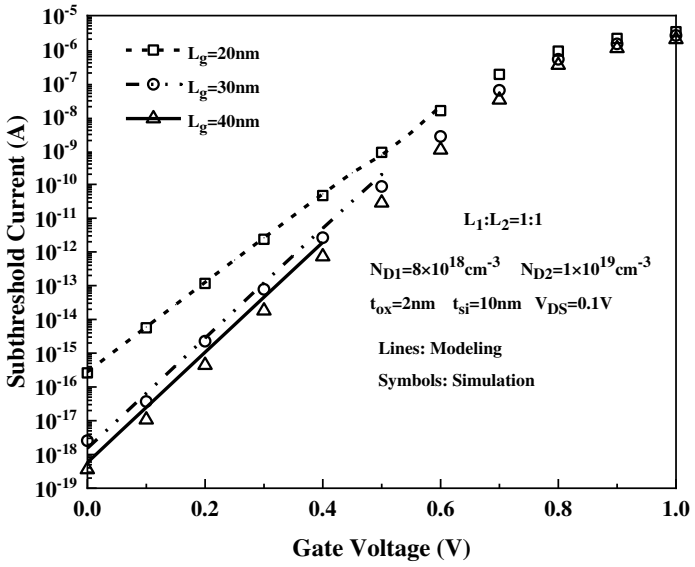


Fig. 11: Variation of Subthreshold current (I_{DS}) with gate voltage (V_{GS}) for different channel length

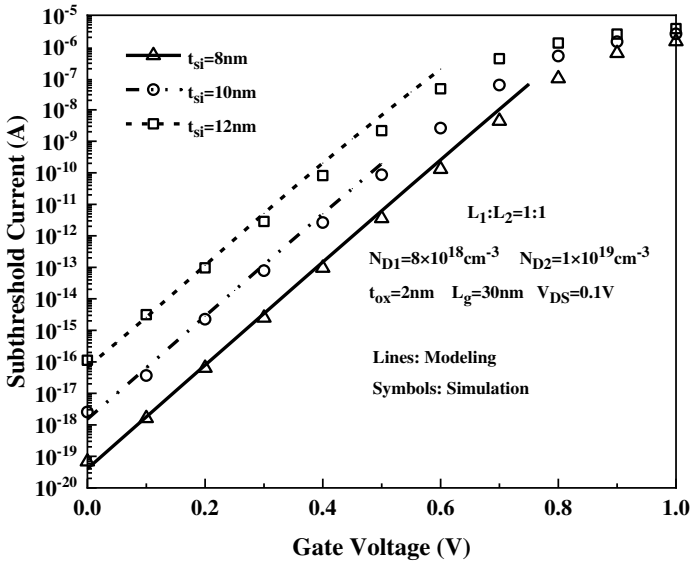


Fig. 12: Variation of Subthreshold current (I_{DS}) with gate voltage (V_{GS}) for different channel thickness

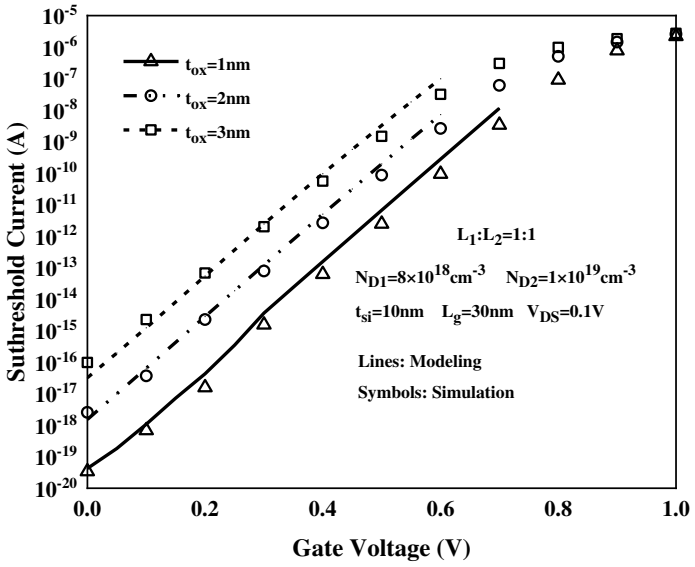


Fig. 13: Variation of Subthreshold current (I_{DS}) with gate voltage (V_{GS}) for different oxide thickness

Figures

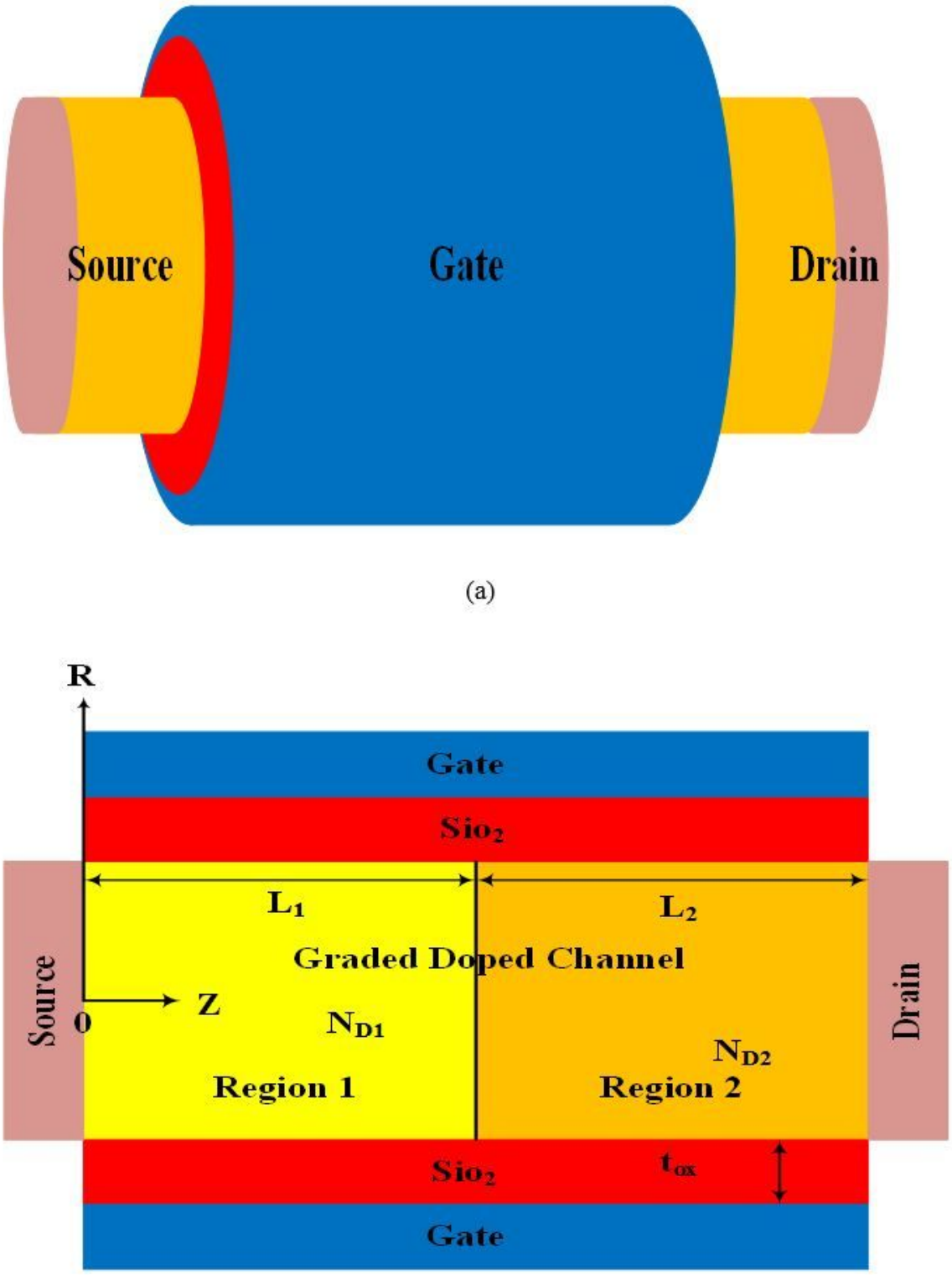


Figure 1

Schematic structure of (a) 3D-view and (b) 2D-view of GD-JL-GAA MOSFETs

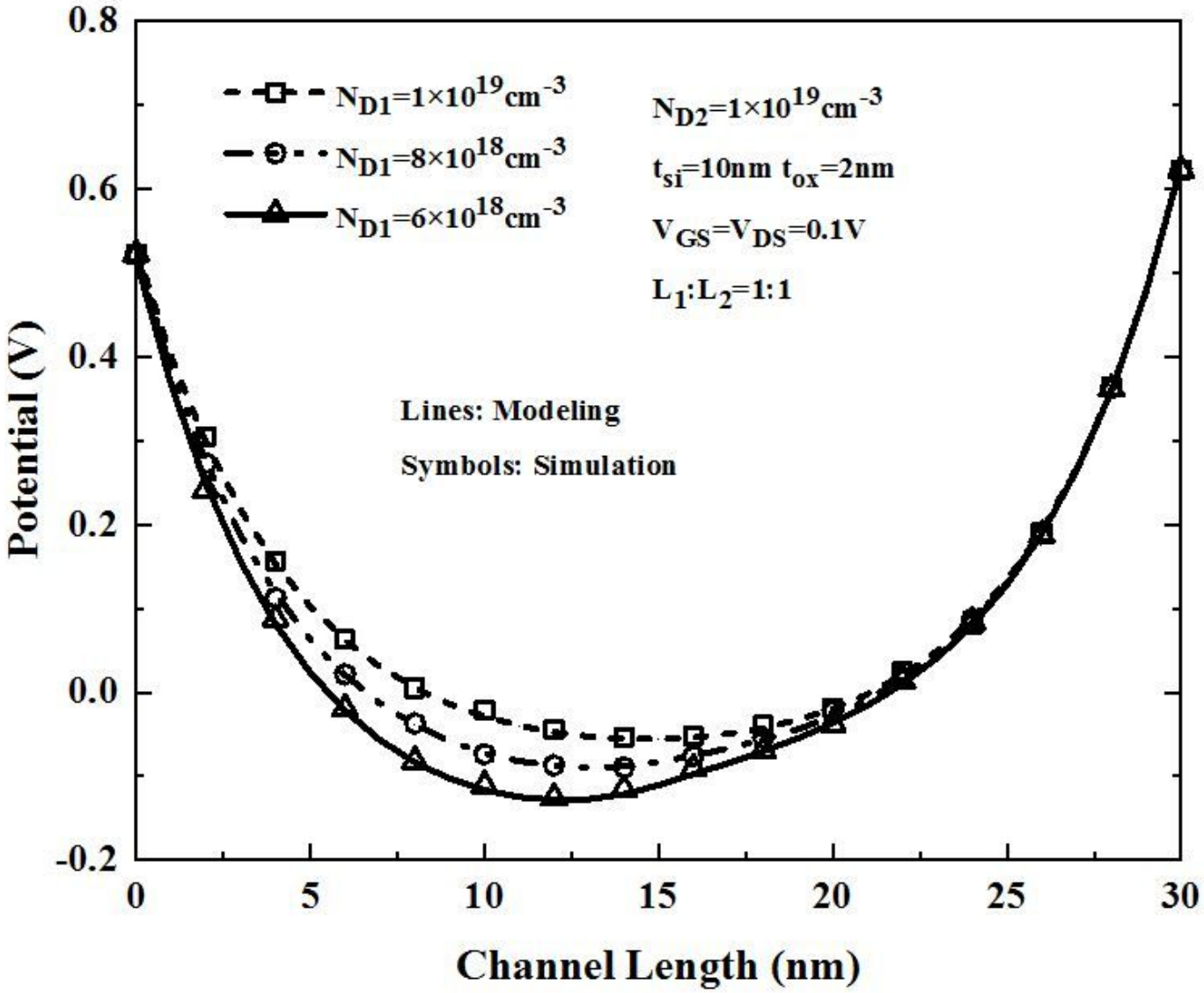


Figure 2

Channel potential variation along the channel length for different doping concentrations.

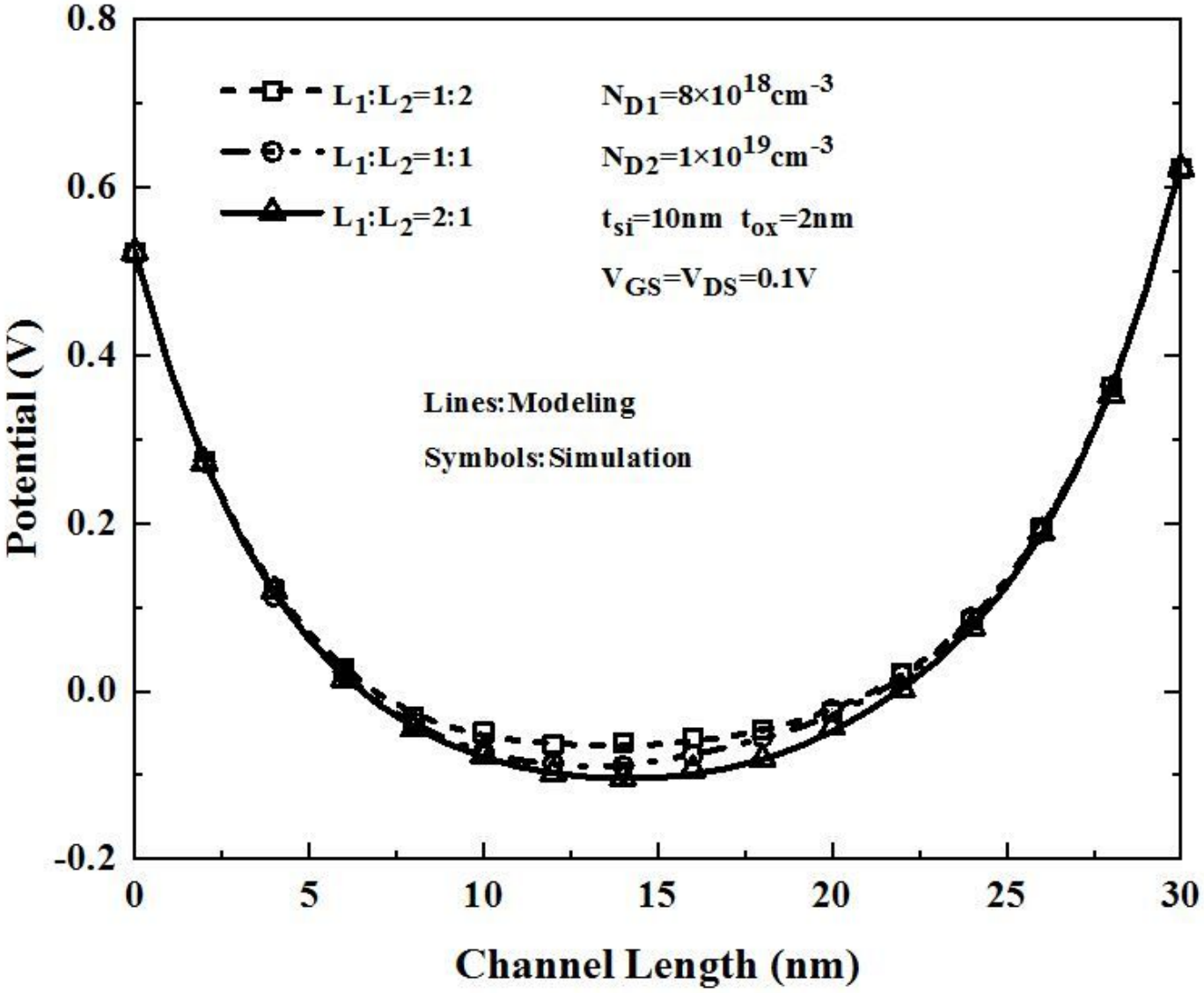


Figure 3

Channel potential variation along the channel length for different channel length ratio L1:L2.

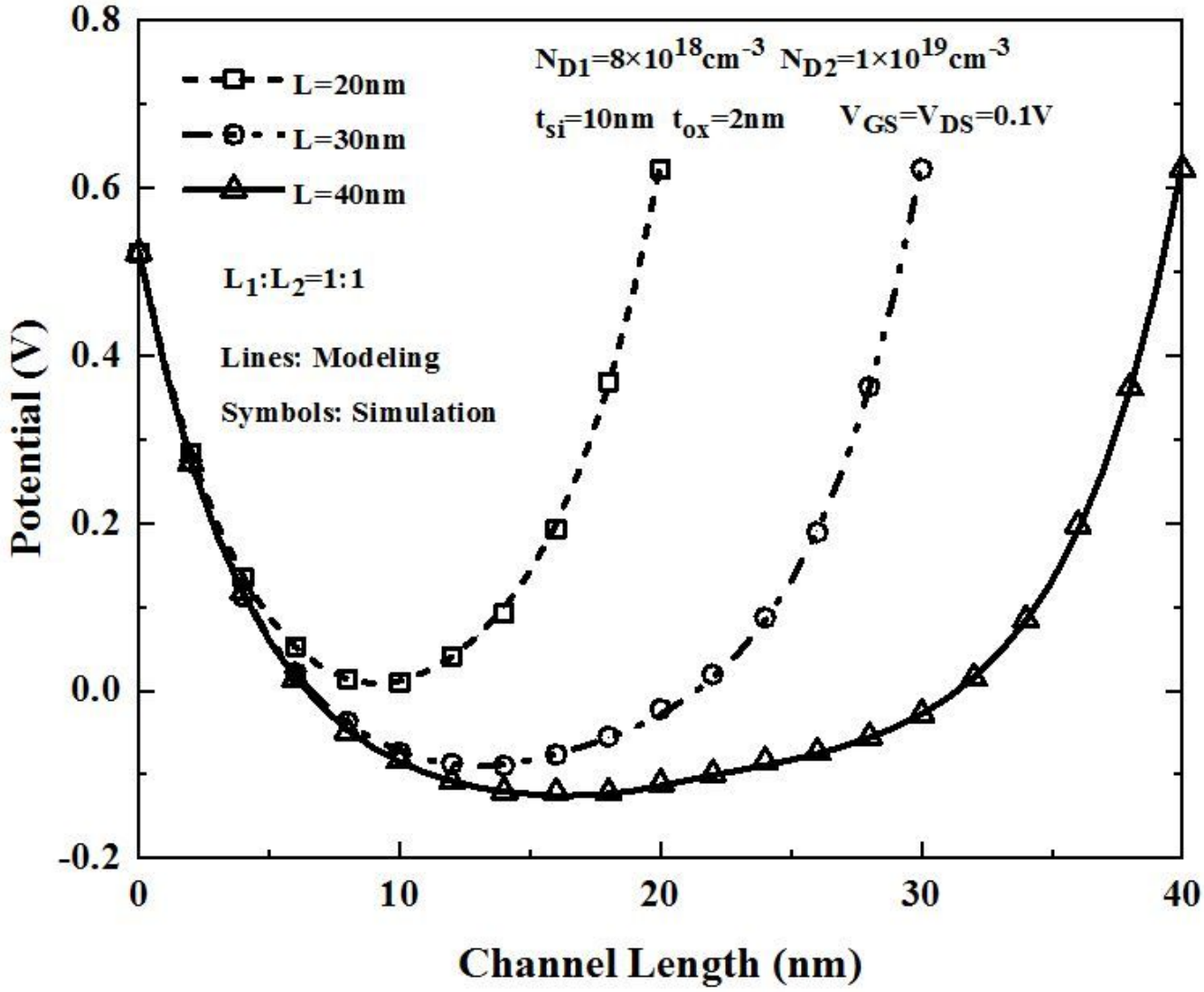


Figure 4

Channel potential variation along the channel length for various channel length.

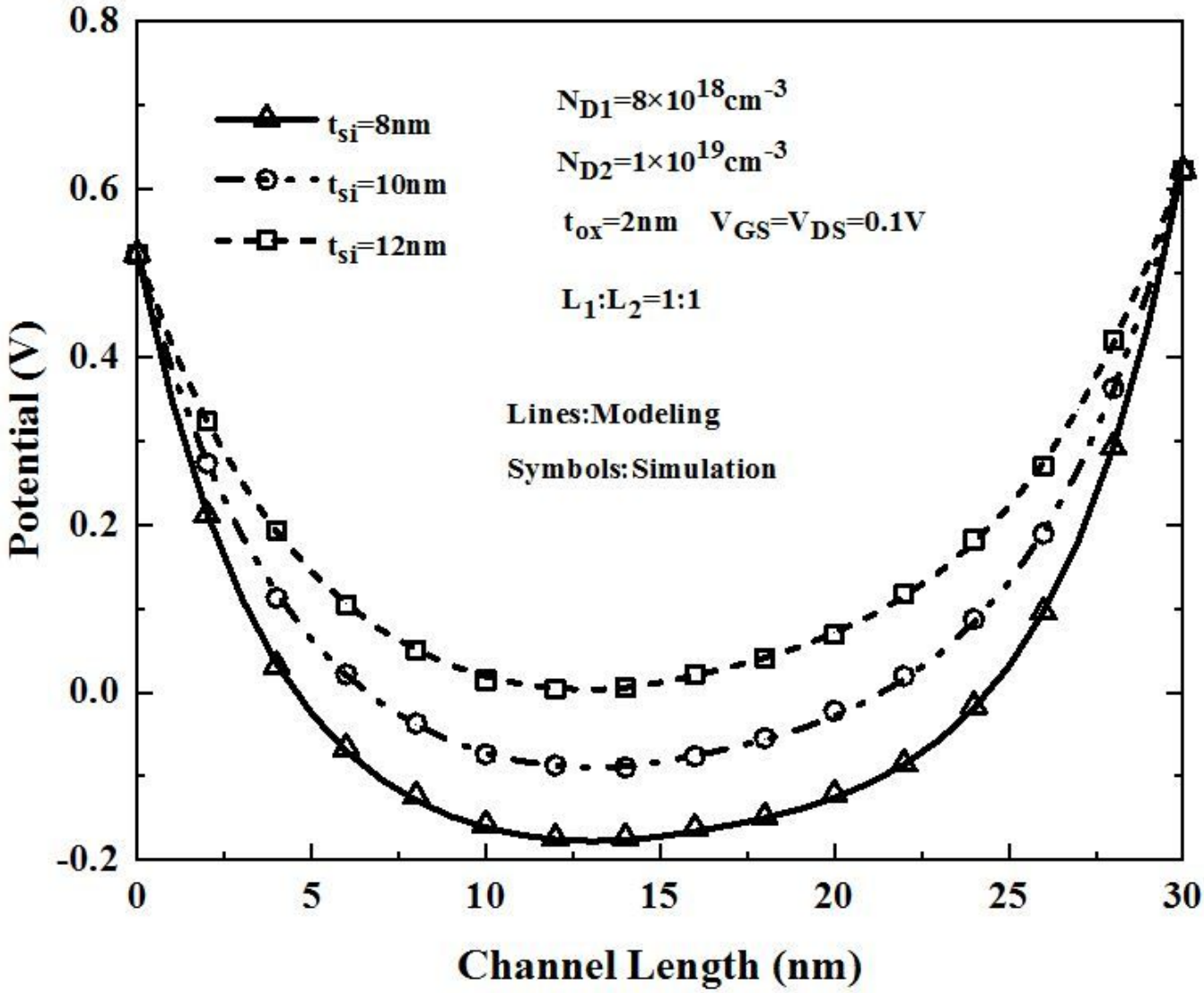


Figure 5

Channel potential variation along the channel length for different channel thickness.

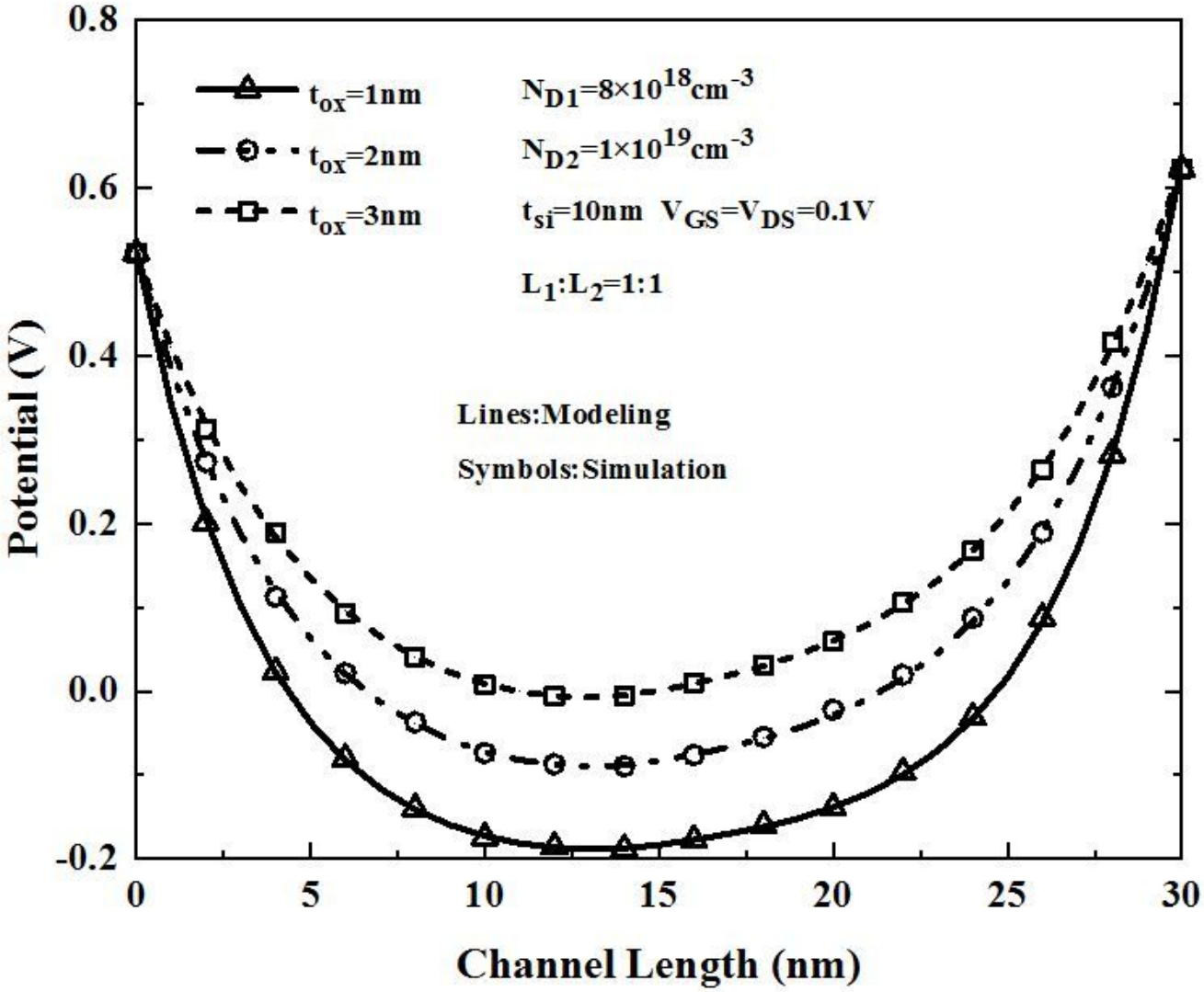


Figure 6

Channel potential variation along the channel length for different oxide thickness.

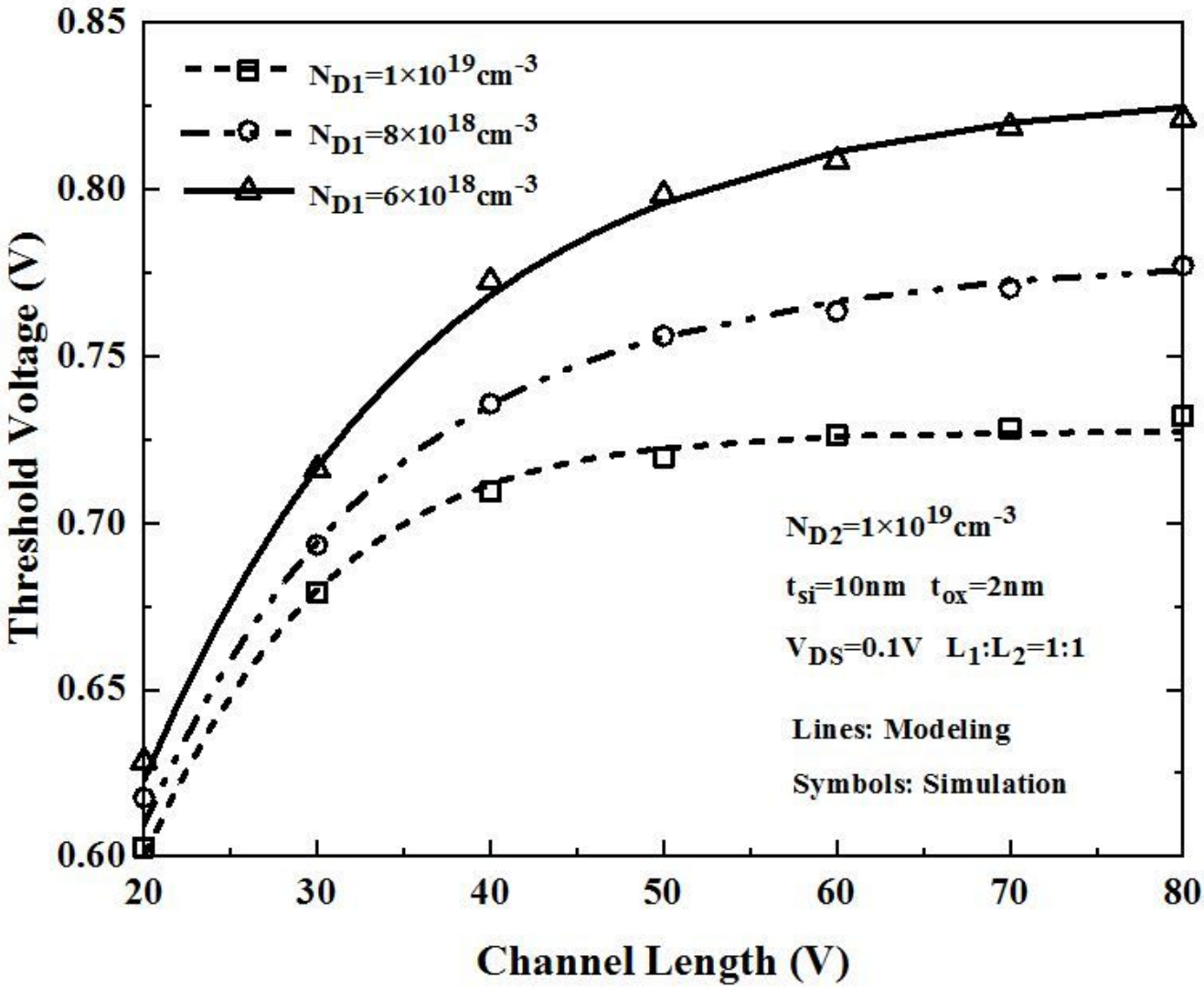


Figure 7

Threshold voltage variation along the increasing channel length for different doping concentrations

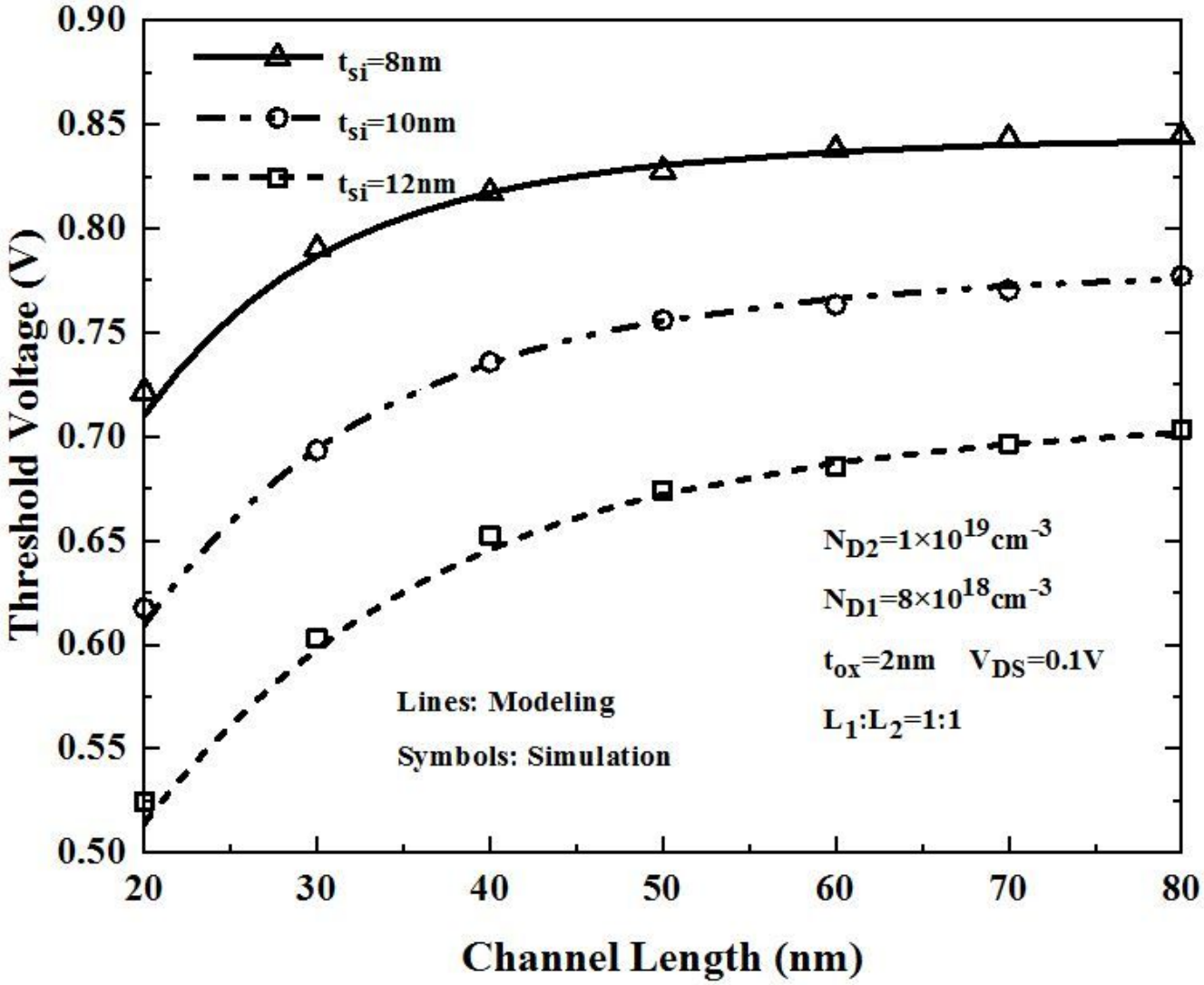


Figure 8

Threshold voltage variation along the increasing channel length for different channel thickness

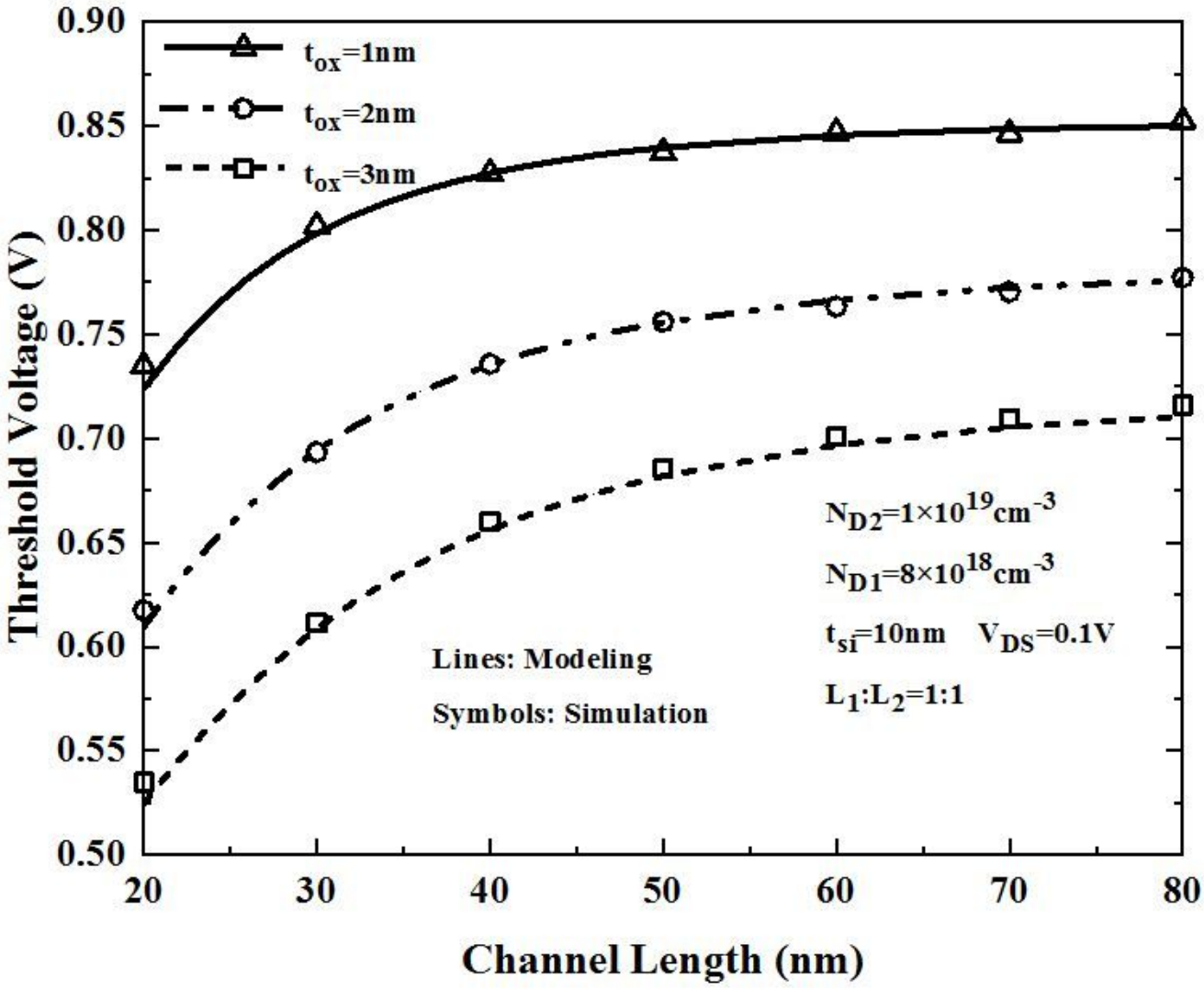


Figure 9

Threshold voltage variation along the increasing channel length for different oxide thickness

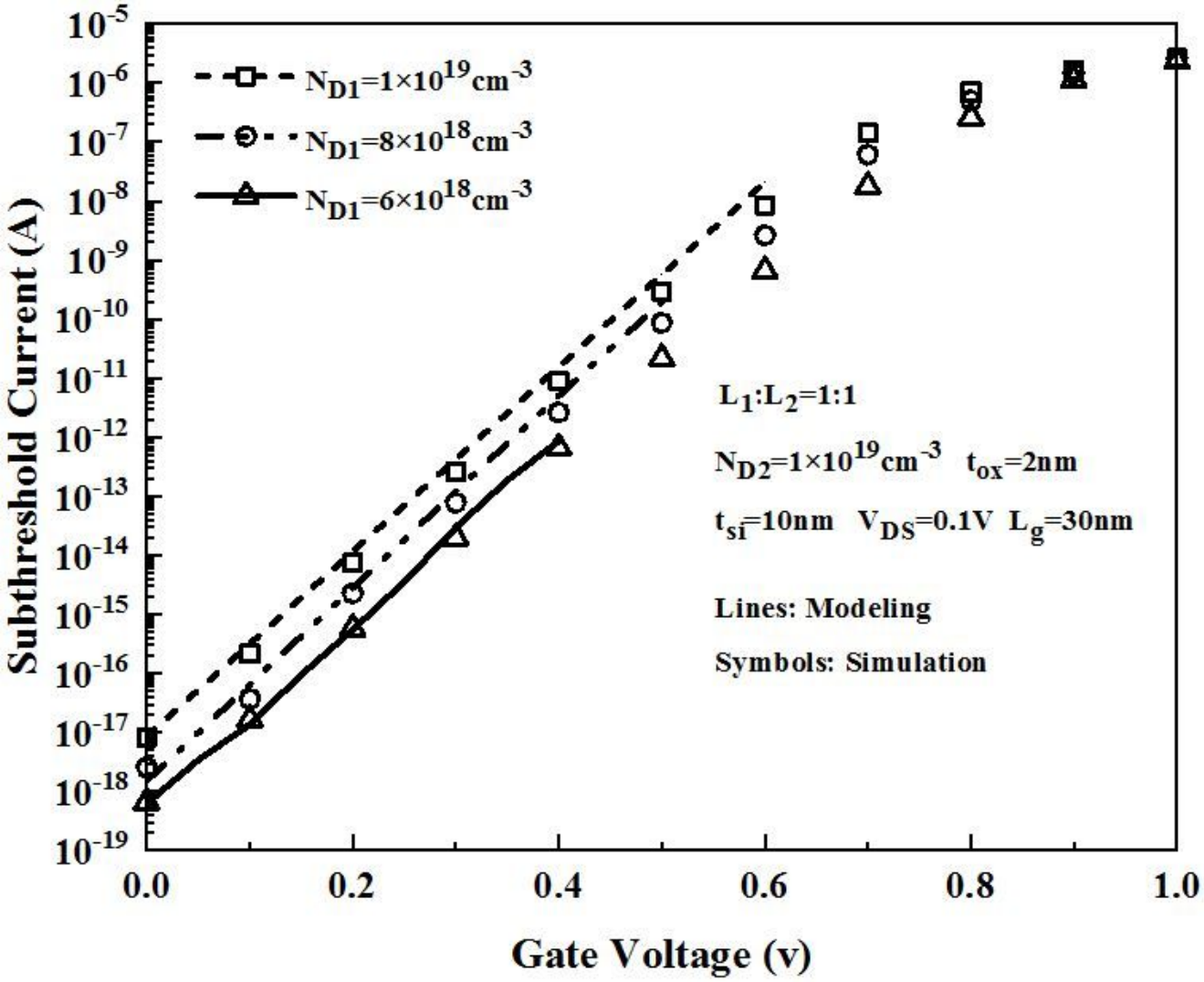


Figure 10

Variation of Subthreshold current (IDS) with gate voltage (VGS) for different doping concentrations

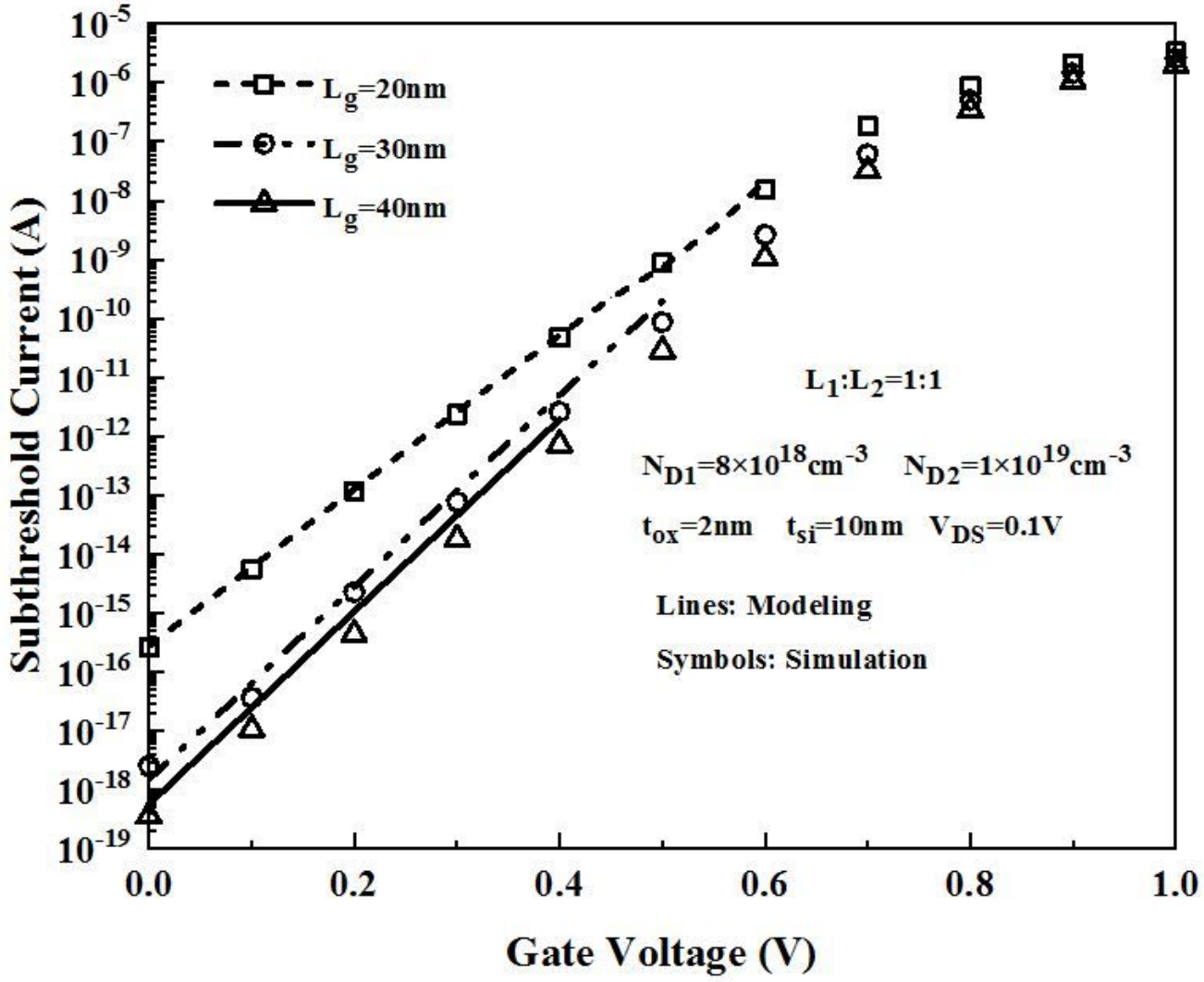


Figure 11

Variation of Subthreshold current (IDS) with gate voltage (VGS) for different channel length

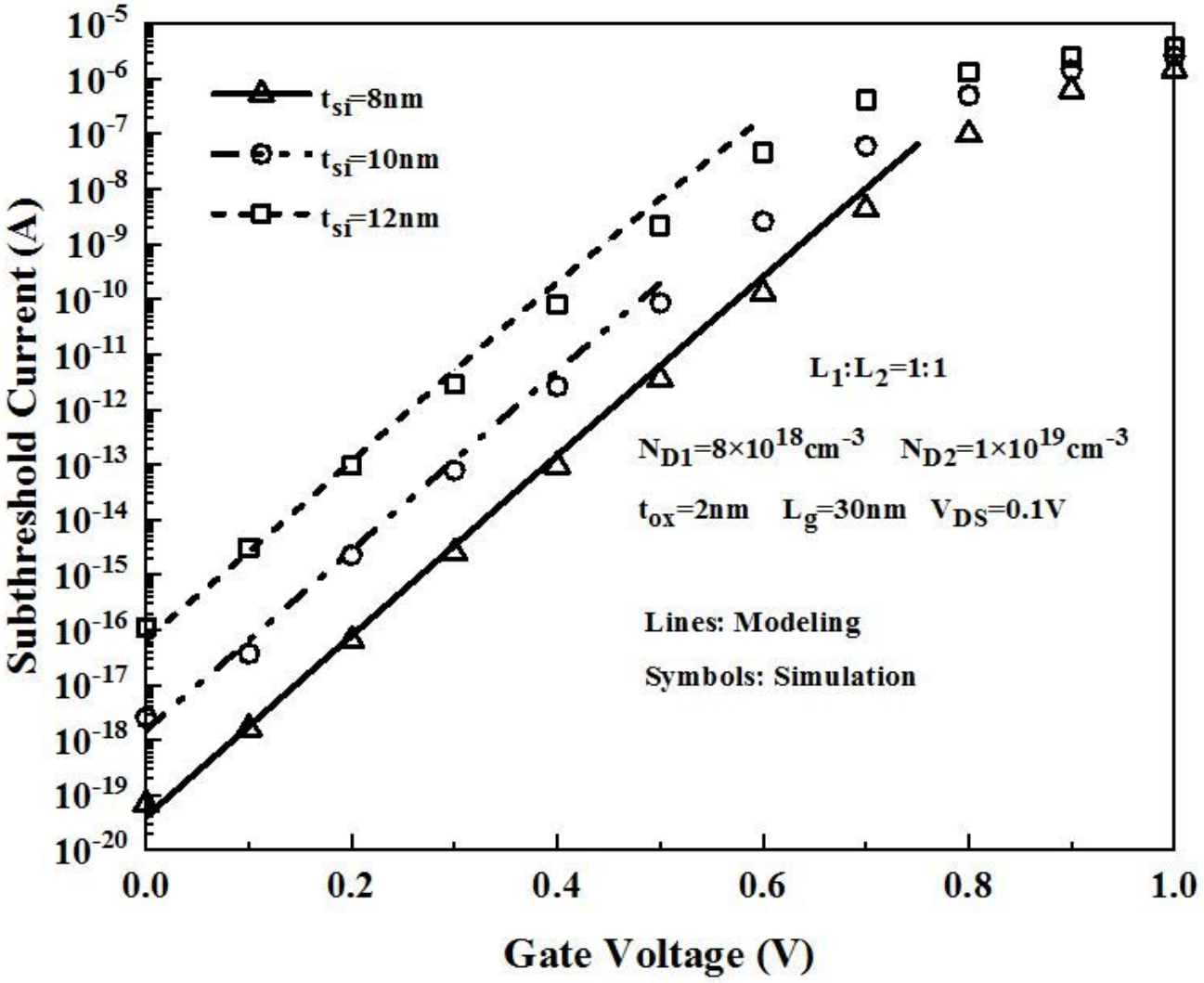


Figure 12

Variation of Subthreshold current (IDS) with gate voltage (VGS) for different channel thickness

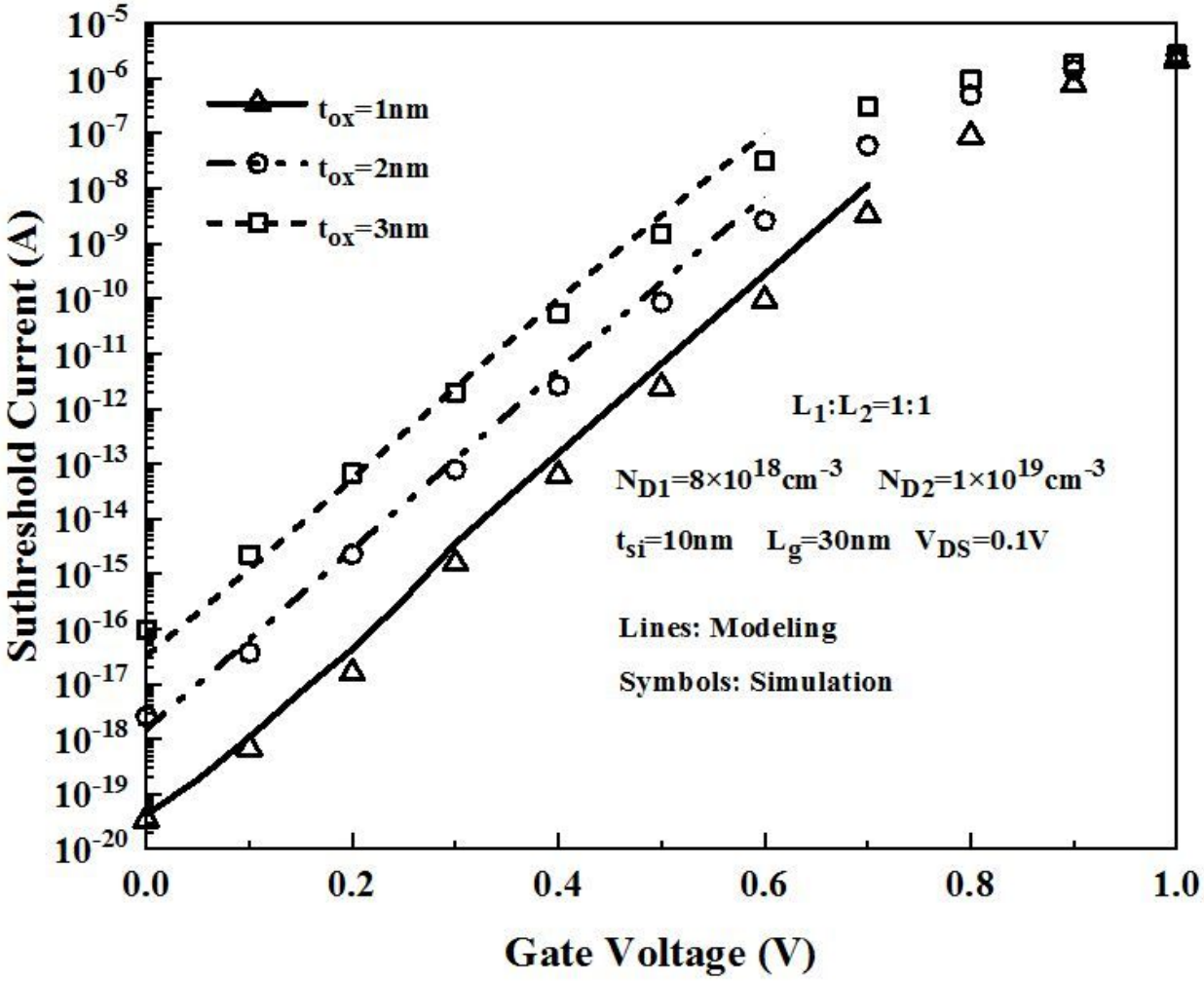


Figure 13

Variation of Subthreshold current (IDS) with gate voltage (VGS) for different oxide thickness