An efficient FIR filter based on hardware sharing architecture using CSD coefficient grouping for wireless application

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Research Article

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Abstract

FIR filter is an essential part of digital signal processing that is extensively used in many areas such as wireless application and digital processing system. An efficient recursive filter is always required for real-time applications such as 5G network, smart robots and Internet of Things etc. The design of FIR filter is inherently stable and has a linear phase characteristic but its implementation often involves complexity and a large filter length to achieve specific design requirements. In this paper, the complexity of FIR filter is reduced by eliminating the repeated subexpression in a canonic sign digit(CSD)number system based filter operation. A new grouping method has been proposed for the CSD number system-based filter coefficient to minimize the number of unpaired nonzero bits in the filter coefficient. The statistical analysis of the proposed grouping method is performed and compared with other existing schemes. The number of unpaired nonzero bits in the proposed grouping scheme is reduced by an average of 24.11% as compared to other existing schemes. Further, an efficient FIR filter with hardware sharing architecture is designed and implemented to achieve a 14.65% reduction in average power consumption and the average operation speed is increased by 10.1% in comparison to the other existing filter structures.

Full Text

Due to technical limitations, full-text HTML conversion of this manuscript could not be completed. However, the latest manuscript can be downloaded and accessed as a PDF.

Figures

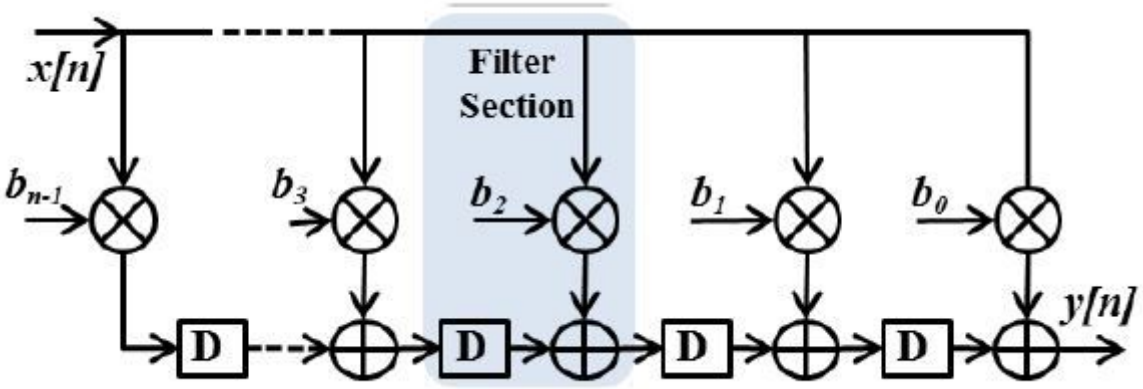

Figure 1

Block diagram of n-tap data broadcast FIR lter

$$b_i = [\underbrace{1\ 0\ -1}_{G_1}\ 0\ 0\ \underbrace{1\ 0\ 0\ -1}_{G_2}\ 0\ 0\ \underbrace{1\ 0\ 1}_{G_3}]_{CSD}$$

$$G_1 = [1\ \ 0\ \ -1] \quad G_2 = [1\ \ 0\ \ 0\ \ -1] \quad G_3 = [1\ \ 0\ \ 1]$$

Figure 2

Proposed grouping pattern for CSD based Iter coefficient

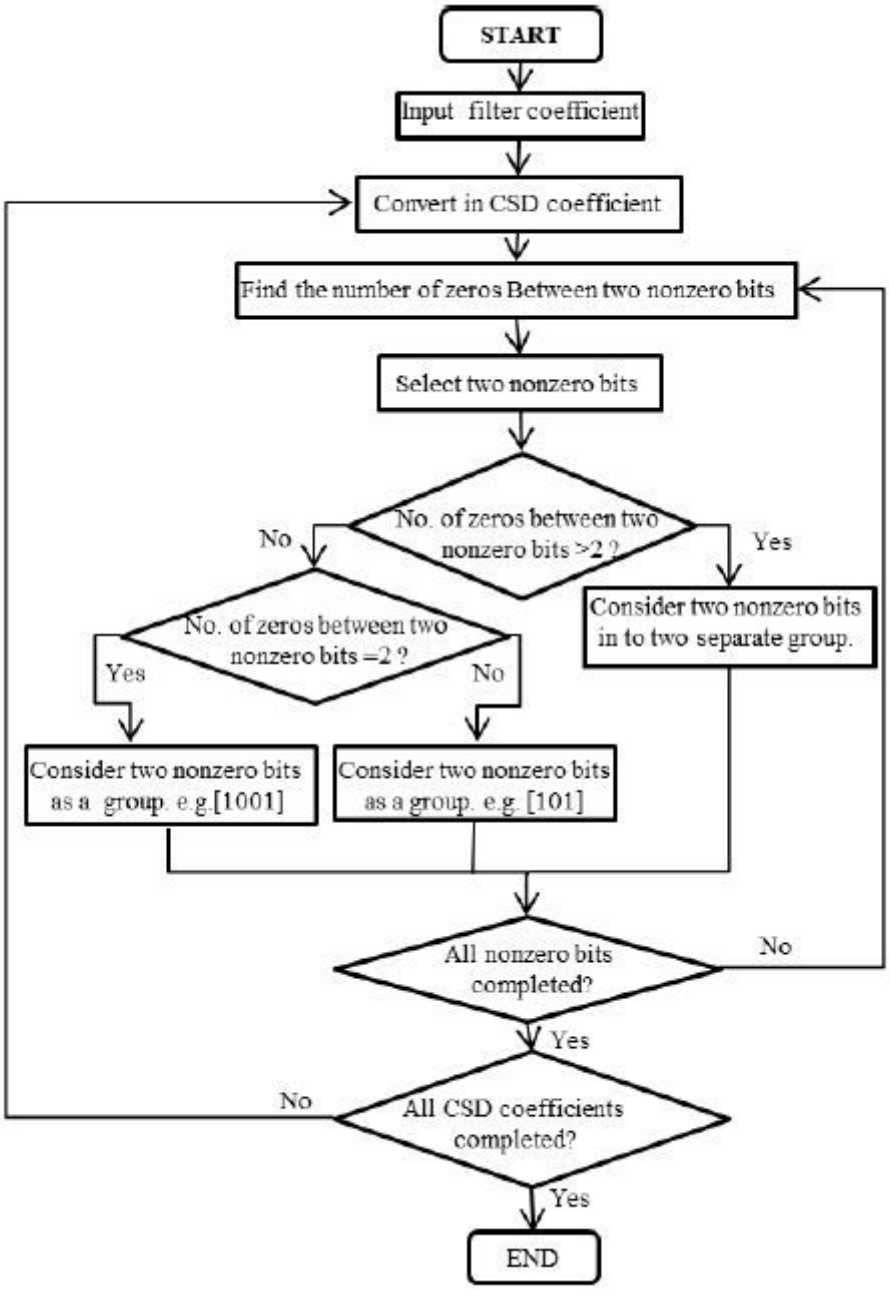

Figure 3

The flowchart of Proposed grouping method for CSD coefficient

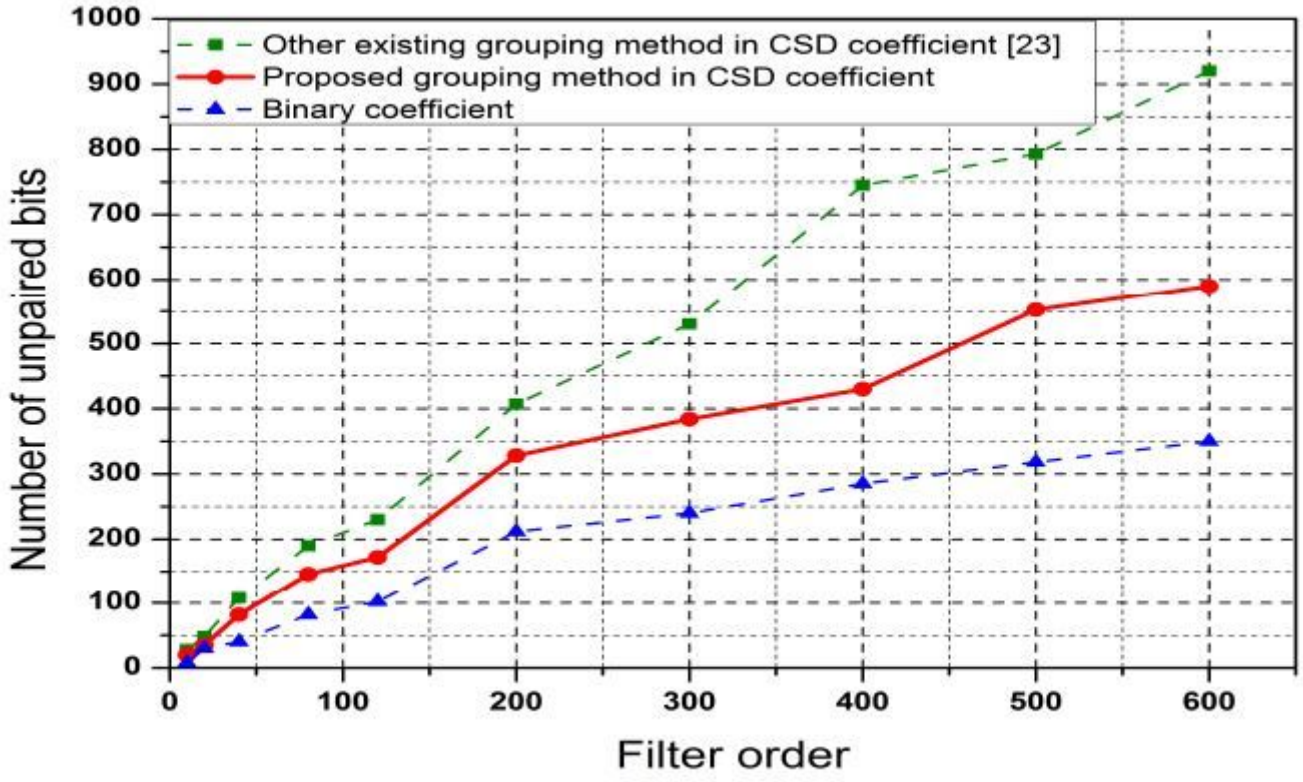

Figure 4

Average number of unpaired nonzero bits for binary representation, proposed group- ing method in CSD based lter coefficient

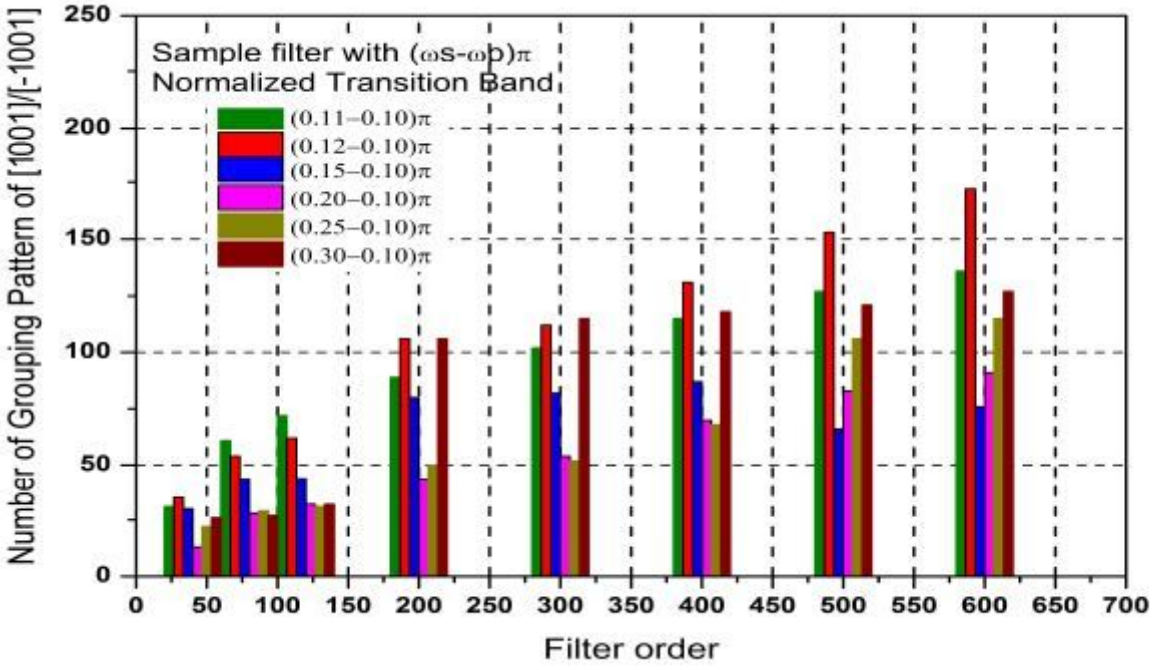

Figure 5

No. of Proposed grouping pattern in narrow transition band CSD based lter coef- cient with lter order

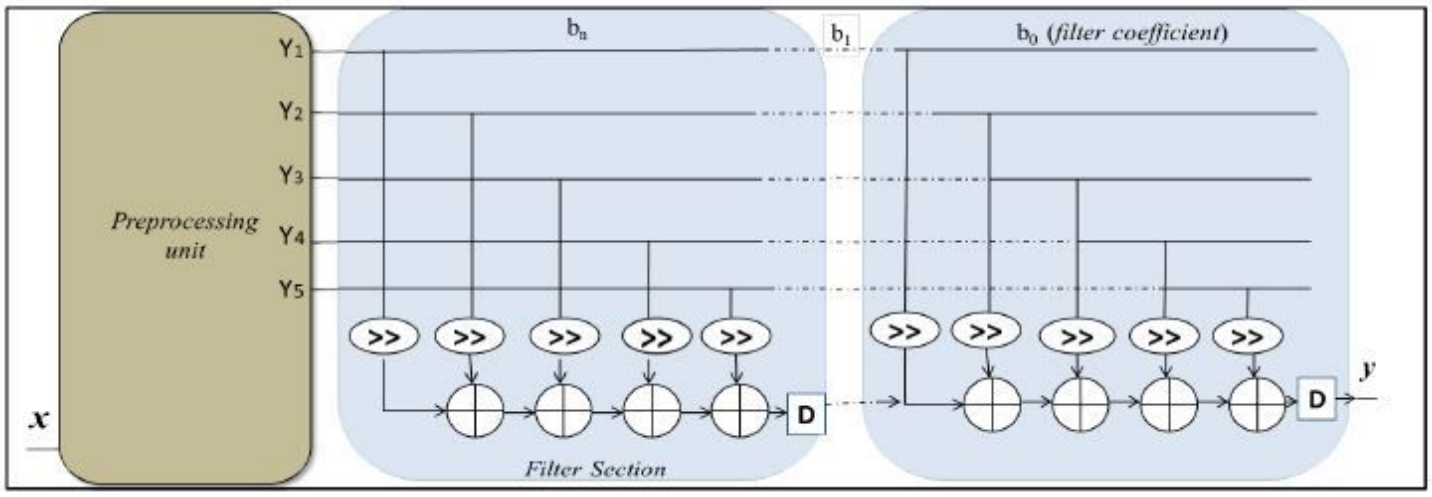

Figure 6

n-tap FIR lter architecture with hardware sharing

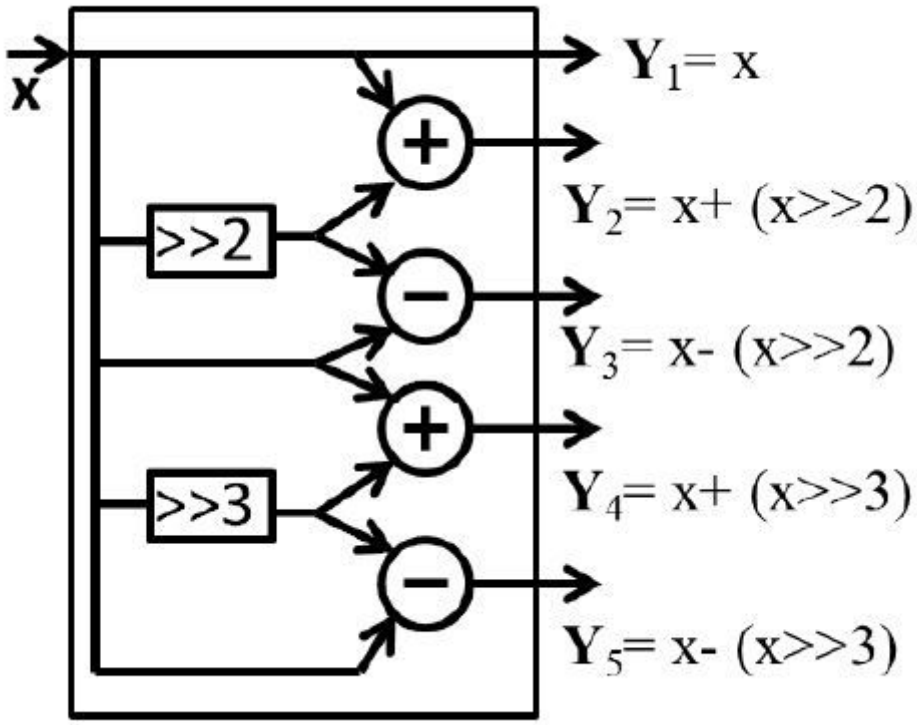

Figure 7

Layout of preprocessing unit

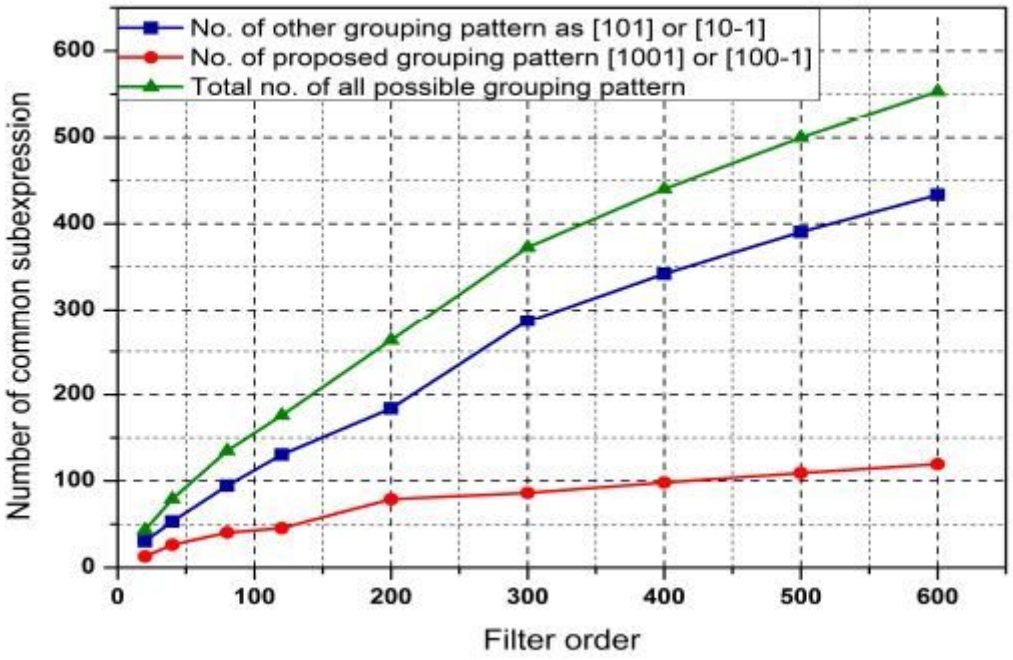

Figure 8

Number of Common Subexpression for proposed grouping method, other existing grouping pattern in CSD based lter coefficient and total number of all possible grouping pattern.

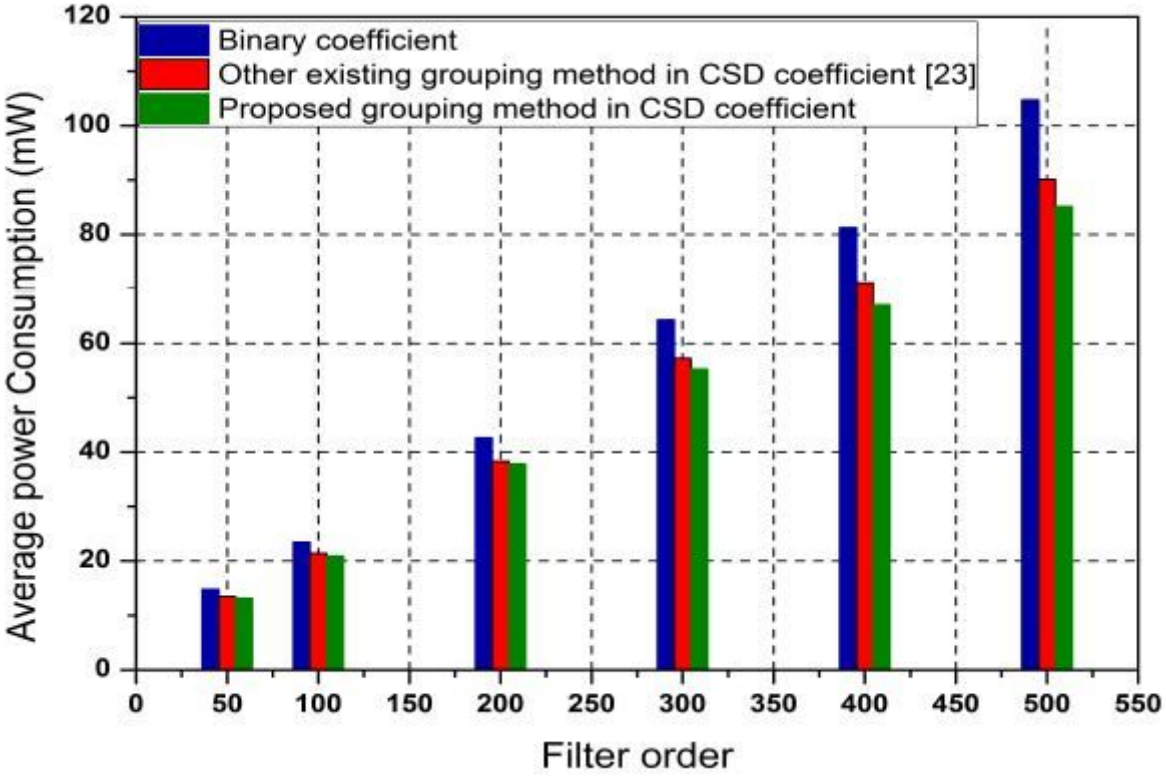

Figure 9

Average of power consumption of binary and CSD coefficient

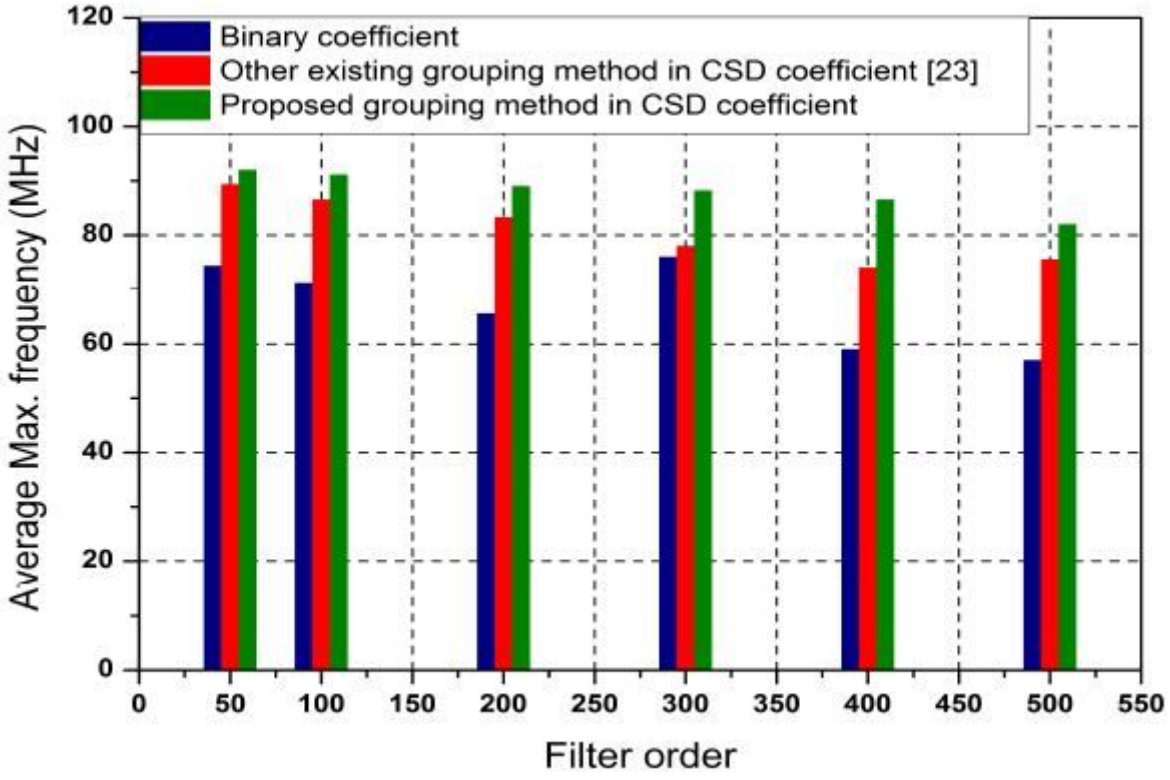

Figure 10

Comparison of average max. frequency with varying lter order