Spike-time dependent plasticity rule in memristor models for circuits design

Mouna Elhamdaoui
Universite de Monastir Faculte des Sciences de Monastir
Faten Ouaja Rziga (fatenrzigaouaja@gmail.com)
Universite de Monastir Faculté Des Sciences de Monastir Tunisie https://orcid.org/0000-0002-7270-4985
Khaoula Mbarek
Universite de Monastir Faculte des Sciences de Monastir
Kamel Besbes
Universite de Monastir Faculte des Sciences de Monastir

Research Article

Keywords: LTP, LTD, Memristor models, Neuromorphic systems, Plasticity, Synapse, STDP

Posted Date: April 30th, 2021

DOI: https://doi.org/10.21203/rs.3.rs-164635/v1

Spike-time dependent plasticity rule in memristor models for circuits design

Mouna Elhamdaoui[1], Faten Ouaja Rziga[1,*], Khaoula Mbarek[1], Kamel Besbes[1,2]

Abstract

Spike Time-Dependent Plasticity (STDP) represents an essential learning rule found in biological synapses which is recommended for replication in neuromorphic electronic systems. This rule is defined as a process of updating synaptic weight that depends on the time difference between the pre- and post-synaptic spikes. It is well known that pre-synaptic activity preceding post-synaptic activity may induce long term potentiation (LTP) whereas the reverse case induces long term depression (LTD). Memristors, which are two-terminal memory devices, are excellent candidates to implement such a mechanism due to their distinctive characteristics. In this article, we analyze the fundamental characteristics of three of the most known memristor models, and then we simulate it in order to mimic the plasticity rule of biological synapses. The tested models are the linear ion drift model (HP), the Voltage ThrEshold Adaptive Memristor (VTEAM) model and the Enhanced Generalized Memristor (EGM) model. We compare the *I-V* characteristics of these models with an experimental memristive device based on Ta_2O_5. We simulate and validate the STDP Hebbian learning algorithm proving the capability of each model to reproduce the conductance change for the LTP and LTD functions. Thus, our simulation results explore the most suitable model to operate as a synapse component for neuromorphic circuits.

Keywords: LTP, LTD, Memristor models, Neuromorphic systems, Plasticity, Synapse, STDP.

1. Introduction

Recently, neuromorphic technology has revealed that brain-based computer systems are capable of processing large amounts of data by using low-power operations [1]. However, they consist basically of similar structures as the human brain, composed of neurons linked by multiple synapses. These systems able to follow a basic weight update rule across synapses, just like humans remember information. This rule was called spike-timing dependent plasticity (STDP) [2]. It demonstrates how the strength of synaptic connections is modulated [2,3]. Thus, the synaptic connection is strengthened when the presynaptic neuron fires before the postsynaptic neuron, which is known as long-term potentiation (LTP), and the connection is weakened when the firing order is reversed, which is called long-term depression (LTD).

Since the discovery of STDP rule in biological synapses, researchers have been attracted with the concept of modifying synaptic weight using this rule in bio-inspired electronic synapses. However, the circuit-oriented approach is complex in that the variable "synaptic weight" generally must be stored as an electric charge in a capacitor or even numerically in a neuromorphic integrated circuit. This adds complexity to the circuit and increases energy and power consumption. Consequently, non-volatile resistive memories, namely memristors are currently employed in neuromorphic computation systems in order to reproduce the synaptic weight update by suitably changing their internal state [4-9].

In particular, memristors have been widely studied and developed to mimic synaptic functions such as, LTP, LTD and STDP [4,10-12]. Several complex tasks were performed efficiently using the STDP learning rule based on memristors such as unsupervised learning [12], data classification [13] and pattern recognition [14].

Memristor component was first introduced by L. Chua in 1971 as the fourth circuit component, alongside the three fundamental passive components, which are the resistor, the capacitor, and the inductor [15]. Memristors are widely used as synaptic devices due to their adjustable resistance [16,17], low-power operation, nano-scale physical structure, and high-density integration [18,19].

In the literature, several research teams have fabricated memristive devices to emulate synaptic functions using a variety of materials [21-24]. The large variety of the memristor devices structure and materials composition has led to the

* Corresponding author.
E-mail address: faten_ouaja@yahoo.fr

[1] Microelectronics and Instrumentation Lab, University of Monastir, Monastir, Tunisia
[2] Centre for Research on Microelectronics & Nanotechnology Sousse Technology Park, Sousse, Tunisia

development of various memristor modeling techniques [18,20,25-29]. This variety of models allows to choose an acceptable compromise between accuracy and simplicity.

Among these models, we will focus on three different models: the linear ion drift model (HP) model [20], the Voltage ThrEshold Adaptive Memristor (VTEAM) model [29], and the Enhanced Generalized Memristor (EGM) model [18]. We simulated the *I-V* curve of these models in order to fit the experimental data of the Ta_2O_5-RRAM device [23]. Next, we implement each model to determine both LTP and LTD functions, and then we validate the STDP learning algorithm. We present a detailed comparison of these models, in order to explore the most promising memristor model to be used as a synapse component.

This article consists of the following sections: Section 2 provides a brief discussion of the memristor switching characteristics. Section 3 introduce the memristor fundamentals including mathematical definition and working principle of HP model, VTEAM model, and the EGM model. Then, we present the *I-V* curves of these models compared to the experimental data. Section 4 discusses our simulation results obtained from the conductance change in order to validate LTP, LTD and the STDP learning algorithm. Section 5 contain discussion of our results. Finally, section 6 concludes this paper.

2. An overview of the memristor switching device

A solid-state memistor device is a thin-film nanoscale TiO_2 device consisting of a doped region with TiO_{2-x} oxygen gaps and an undoped region of TiO_2. These two regions are sandwiched together across two platinum electrodes, as depicted in Fig.1 (a). The resistance change is induced by migration of the oxygen holes in the TiO_{2-x} region, produced by the application of a voltage across the memristor. Therefore, the oxygen holes migration depends on the sign of the applied voltage.

Applying a positive voltage to the top electrode of the device switches the resistance states from high resistance state (HRS) to low resistance state (LRS), and this switching is referred as SET state. Alternatively, when a negative voltage is applied, it switches from the LRS state to the HRS state, and this is referred as RESET state. Because of the poor oxygen mobility of the vacancies, they may be able to stand for a long time after switching off the power supply to the device. This means that if no power is provided to the device, then the memristors' dynamic resistance will remain constant. This shows that the memristor device has the ability to operate as a non-volatile memory. Moreover, there is a major property that sets memristor devices apart from all other electronic devices, namely the I-V characteristic known as the pinched hysteresis loop, which is illustrated in Fig.1 (b). This distinctive shape arises from the non-linear relationship between the voltage and the current passing across the memristor device. Besides, both negative and positive voltage pulses can affect the conductance of the device. This is similar to a biological synapse whose synaptic plasticity increases or decreases according to the applied action potential.

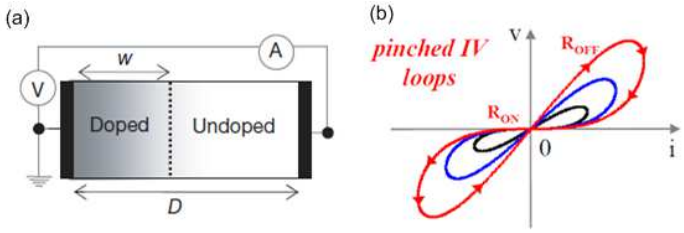

Fig. 1 (a) Structure of the HP TiO_2 memristor [2] (b) The memristor pinched *I-V* loop.

3. Memristor Models

We provide in Table 1 a comparative study of the memristor models, including their mathematical characteristics and their implemented parameters, which we will be implementing and testing in the next section.

Table 1 Comparative analysis of the memristor models

Memristor Models	**Linear Ion Drift model (HP)** [19]	**Voltage Threshold Adative Memristor model (VTEAM)** [28]	**Enhanced Generalized Memristor model (EGM)** [17]
Threshold Voltage	No	Yes	Yes
State variable	$0 \le w \le D$ Doped region width	$x_{on} \le x \le x_{off}$ Undoped region width	$0 \le w \le 1$ Not explained physically
Generic	No	Yes	Yes
Current-voltage relationship	$v(t) = \left(R_{on}\frac{w(t)}{D} + R_{off}\left(1 - \frac{w(t)}{D}\right)\right) i(t)$	$i(t) = \left[R_{on} + \frac{R_{off} - R_{on}}{w_{off} - w_{on}}.(w - w_{on})\right]^{-1}.v(t)$	$i(t) = \begin{cases} a_1\, x(t)\sinh(b\, v(t)); & v(t) \ge 0 \\ a_2\, x(t)\sinh(b\, v(t)); & v(t) < 0 \end{cases}$
State variable derivative	$\frac{dw}{dt} = \frac{\mu v R_{on}}{D} i(t)$	$\frac{dw(t)}{dt} = \begin{cases} k_{off}.\left(\frac{v(t)}{v_{off}} - 1\right)^{\alpha_{off}}.f_{off}(w), & 0 < v_{off} < v \\ 0, & v < v_{on} < v_{off} \\ k_{on}.\left(\frac{v(t)}{v_{on}} - 1\right)^{\alpha_{on}}.f_{on}(w), & v < v_{on} < 0 \end{cases}$	$\frac{dx}{dt} = \eta\, g(v(t))\, f(x(t))$
Simulation parameters	R_{off}=140kΩ; R_{on}=1kΩ; R_{init}=36kΩ; D=1nm; μv=1$e^{-14}m^2s^{-1}v^{-1}$.	a_1=a_2=6.10^{-5}; b=2.1; V_p=V_n=1; A_p=A_n=2050; α_n=0.3; αp=0.1; x_p=0.9; x_n=0.1; x_0=0.1; η=1	R_{on}=13kΩ; R_{off}=110kΩ; V_{on}=-1V; V_{off}=0.02V; k_{on}=-100ms^{-1}; k_{off}=5e-4ms^{-1}; α_{on}=2.5; α_{off}=1.5; w_{on}=0; w_{off}=4nm.

We simulate the studied models with the Spectre simulator in Virtuoso® Custom IC Design in order to fit the *I-V* results of an experimental Ta_2O_5-RRAM memristor device and then to validate their capabilities to emulate synaptic functions.

- *Simulation of the Linear Ion Drift model*

The linear ion drift model has been developed based on the first fabricated HP's structure of the memristor device [19]. The above memristor behavior is mathematically described using equations in Table 1. The voltage *V* and current *I* curves of the HP model are shown in Fig. 2(a) in which we performed a sinusoidal excitation of 2 V magnitude and 1 *kHz* frequency. Fig.2 (b) gives a comparative analysis between the experimental data of the Ta_2O_5-RRAM device [23] and the simulated results of the linear ion drift model.

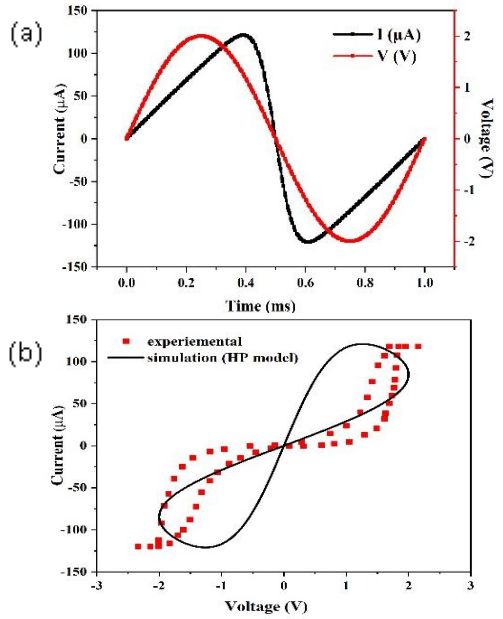

Fig. 2 (a) Current and voltage curves of the simulated HP model versus time, (b) The experimental *I-V* curve of Ta_2O_5-RRAM memristor device compared with the simulated results of the HP model.

- *Simulation of the Voltage Threshold Adaptive Memristor model*

The VTEAM model has been proposed by Kvatinsky et al. [29]. It is an extension of the TEAM model which is based on current threshold [28]. VTEAM is a voltage threshold-type model developed to fit different experimental results. Fig.3 (a) gives the current *I* and voltage *V* curves of the simulated VTEAM model. Fig.3 (b) shows the *I–V* characteristics of the VTEAM model compared with the Ta_2O_5-RRAM memristor device [23].

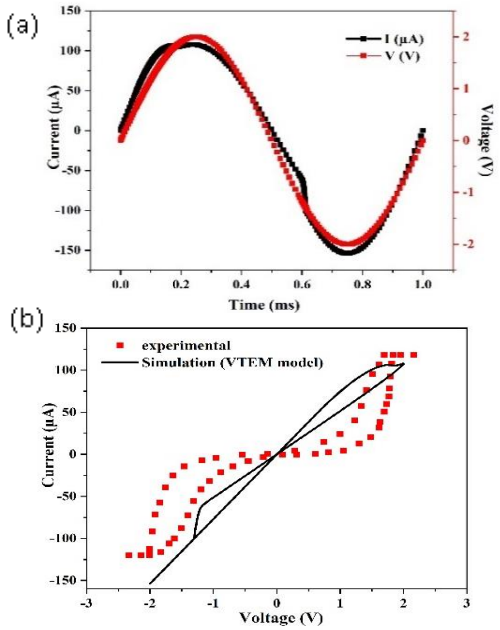

Fig. 3 (a) Current and voltage curves of the simulated VTEAM model versus time, (b) The experimental *I-V* curve of Ta_2O_5-RRAM memristor device compared with the simulated results of the VTEAM model

- *Simulation of the Enhanced Generalized Memristor model*

The Enhanced Generalized Memristor model has been proposed in [27] and then explored in [18]. A sub-circuit of the memristor model is implemented as a simple netlist, which consists of multiple elements in SPICE [27]. Then, The EGM model undergoes some modifications in order to be implemented in Verilog-A [18]. The model was correlated to several memristor devices. Fig.4 (a) shows the current *I* and voltage *V* curves of the EGM model. Fig.4 (b) shows both the experimental *I-V* curve of the Ta_2O_5-RRAM device [23] and the simulated results of the EGM model.

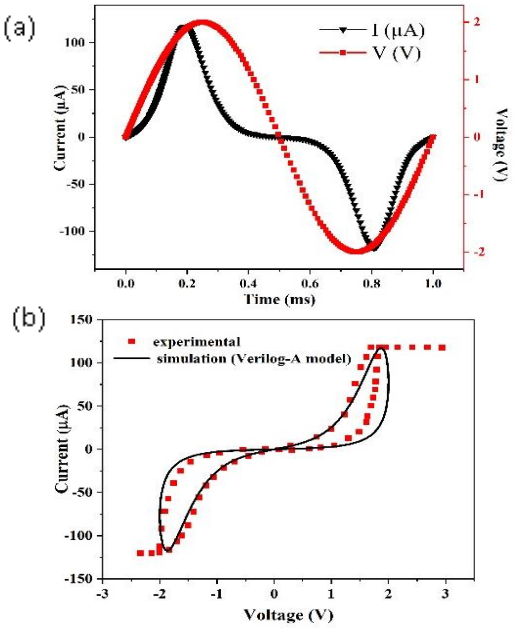

Fig. 4 (a) Current and voltage curves of the EGM model versus time, (b) The experimental *I-V* curve of Ta_2O_5-RRAM memristor device compared with the simulated results of the EGM model.

We can notice that the *I-V* curves of the HP model and the VTEAM model indicate almost linear characteristics everywhere except the boundary, with a symmetric switching behavior for the HP model and an asymmetric behavior for the VTEAM model. Thus, the HP and VTEAM models cannot correlate well the behavior of the physical device. While the obtained *I–V* characteristics of the EGM model with a symmetric curve agree well with the experimental data of the Ta2O5-RRAM memristor model [23].

4. Synapse functions mimicking

4.1 Long term potentiation/ depression

In neural networks, the synaptic connection weight can be modulated through learning protocols, LTP, LTD and STDP. LTP indicates that certain patterns of synaptic activity can cause a lasting increase in synaptic strength, while other patterns of synaptic activity can cause a continuous decrease in synaptic strength, LTD.

To test LTP and LTD mechanisms, we applied a hundred consecutive pulses for different amplitudes values and a fixed pulses duration is the order of 1 µs. Fig.5 explores the conductance change curves for the three memristor models showing the LTP and LTD cases when a sweeping voltage was applied.

We specified two amplitude ranges for each model, the first one is used to maintain LTP and the second one is used to maintain LTD case.

- The pulse amplitude for the HP model is variated between {-1 V, -4 V} for LTD and {1 V, 4 V} for LTP. Fig. 5 (a) and (b) show a gradual conductance decrease and increase for the HP model according to the input voltage bias.
- For the VTEAM model the pulse amplitude is variated between {-1.5 V, -3.5 V} for the LTP case and {1.5 V, 3.5 V} for the LTD case. Fig. 5 (c) and (d) show a gradual conductance decrease when applying positive voltage and no conductance increase for negative input voltage for the VTEAM model.
- For the EGM model, we choose a pulse amplitude variated between {-1.5 V, -2.2 V} for LTD and {1.8 V, 3 V} for LTP. Fig. 5 (e) and (f) show a gradual conductance decrease and increase according to the input voltage bias for the EGM model.

These previous results of the *I-V* characteristic and the conductance gradual change can prove that the EGM is the most effective and suitable model to be used as a synapse component. To further demonstrate this, we will test the capacity of each model to validate the STDP mechanism.

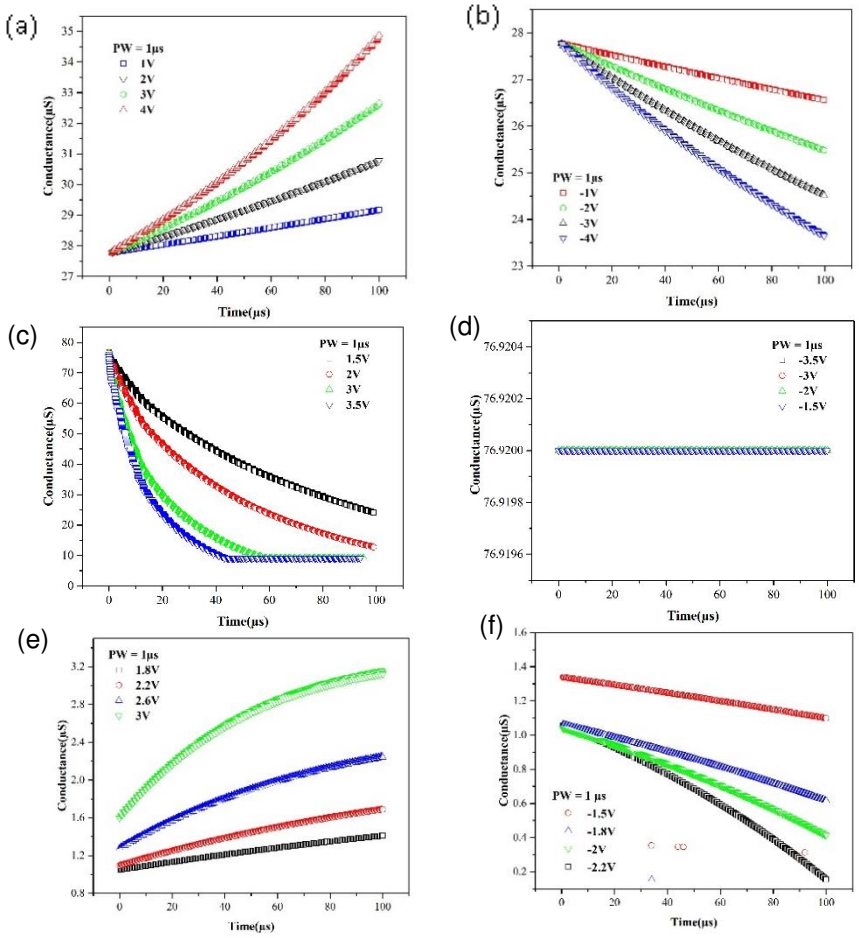

Fig. 5 Curves of the conductance change for a voltage sweeping. Potentiations and depressions: (a), (b) for HP model, (c), (d) for the VTEAM model and (e), (f) for the EGM model.

4.2 Validation of the spike-time-dependent plasticity

The STDP is a learning mechanism based on mammalian brain synapses [30]. Several experimental investigations of this mechanism have been studied in synapses based memristors architectures [10,21-24]. The STDP modify the synaptic weight depending on the activities of the pre-synaptic and post-synaptic neurons [4]. The pre-neuron and post-neuron spikes reach the synapse in opposite directions. In this case, the change in synaptic weight is a function of the relative timing between the two neuron spikes, labeled Δt ($\Delta t = t_{post} - t_{pre}$), where t_{pre} and t_{post} are the arrival timing of pre- and post-spikes, respectively.

- When Δt > 0, the synapse exhibits long-term potentiation (LTP).
- When Δt < 0, the synapse exhibits a long-term depression (LTD).

The combination of the synaptic functions, LTP and LTD, subsequently confirm the STDP learning method.

In order to test and validate the STDP function using the memristor models detailed in our work, we employ a spike pair protocol [31,32] in which the lower and upper memristor electrodes are assigned to the presynaptic and postsynaptic inputs respectively, as shown in Fig. 6.

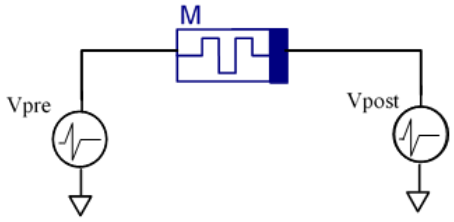

Fig. 6 Design circuit of the memristor synapse.

We considered the same voltage pulses for the three simulated memristor models. The maximum voltage applied to the memristor could be high enough to change the resistance state of the memristor which is fixed as 2 V. In the STDP demonstration, we consider the device conductance as the synaptic weight.

Then its variability is corresponding to a change in the synaptic weight. The evolution of memristance for each memristor model during the application of positive and negative Δt was given in Fig.7.

- For the HP model, as shown in Fig.7(a) if Δt > 0 the memristance decrease from 18,2 *k*Ω to 17,6 *k*Ω, so the conductance presents LTP. And if Δt < 0 the memristance increase from 17.6 *k*Ω to 18,2 *k*Ω to show the conductance LTD.
- For the VTEAM model, the memristance change was given in Fig. 7(b). If Δt > 0, the memristance remains unchanged to 6.5 *k*Ω. And if Δt < 0, the memristance increases from 6.5 *k*Ω to 9.9 *k*Ω, thus the conductance shows LTD.
- For the EGM model, the memristance change was given in Fig. 7(c). If Δt > 0, the memristance decrease from 36,6 *k*Ω to 17,3 *k*Ω, so the conductance presents LTP. Then, if Δt < 0, the memristance increases from 17,3 *k*Ω to 36,6 *k*Ω, so the conductance indicate an LTD.

In addition, in order to implement the STDP learning rule, we use the function Δw (Δt) described by Eq. 1, which is defined as a modification of the synaptic weight for an isolated pair of spikes [33,34]. As given in Fig. 7, the amount of potentiation and depression will be determined as a function of the time difference between pre-synaptic and post-synaptic spikes.

$$\Delta w(\Delta t) = \begin{cases} w^{+} e^{\frac{-\Delta t}{\tau^{+}}} & for \quad \Delta t > 0 \\ -w^{-} e^{\frac{\Delta t}{\tau^{-}}} & for \quad \Delta t < 0 \end{cases} \qquad (1)$$

Where w^- and w^+ indicate the minimum and maximum modifications of the synaptic weight with respect to the initial state during potentiation and depression functions, respectively. τ^- and τ^+ are the time windows that define the synaptic weight update rate for LTD and LTP cases, respectively.

Moreover, we use the previous results illustrated in Fig.7 to determine the value of the Δw function for each model.

Fig. 8 shows the simulation results of the STDP characteristics based on the three memristor models.

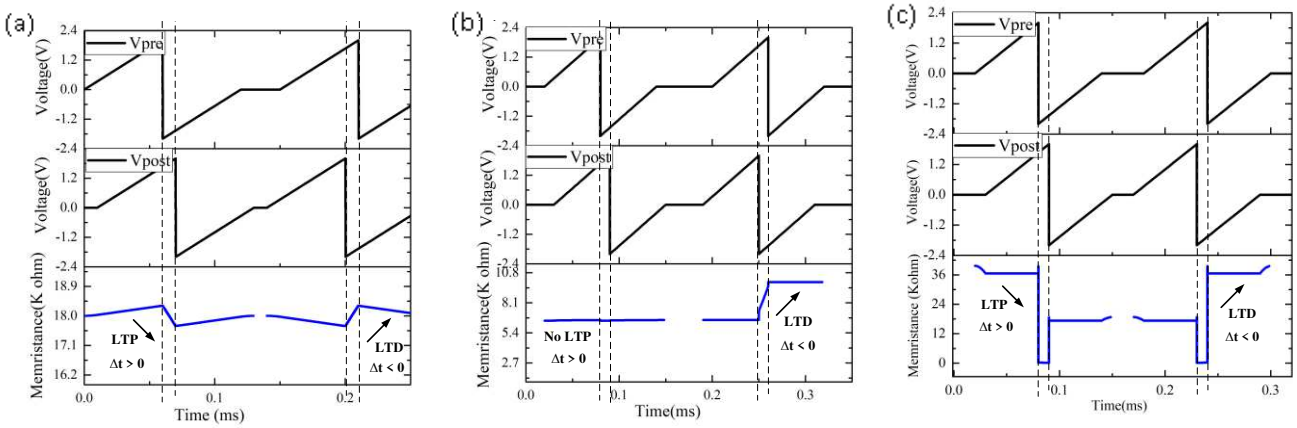

Fig. 7 Simulation results of STDP test circuit given pre voltage spikes, post voltage spikes and the memristance evolution: (a) HP model, (b) VTEAM model (c) EGM model.

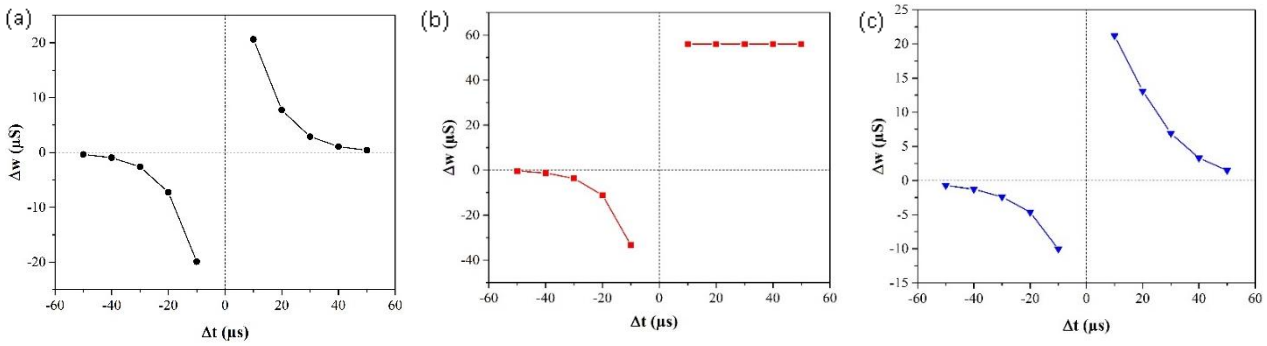

Fig. 8 Represent the STDP simulation results: (a) HP model, (b) VTEAM model, (c) EGM model.

Using our previous results when testing the ability of the three simulated models to mimic the LTP and LTD, we can conclude that, the conductance programmability of the HP model and the EGM model can demonstrate both LTP and LTD functions, which leads to the validation of the STDP learning rule, as shown in Fig.8 (a) and (c). Hence, these results are similar to biological synaptic systems [2]. While the VTEAM model can only support LTD. Then, its STDP curve can show conformity with biological systems only when $\Delta < 0$, as shown in Fig. 8 (b). So, we can conclude that we cannot apply the VTEAM model to implement neuromorphic circuit using the STDP learning method.

5. Discussion

To design neuromorphic circuits based on memristors, the implemented models must be sufficiently effective as compared to the behavior of physical devices, they should support LTP and LTD functions to validate STDP learning mechanism. Also, it is desirable for the memristor model to be simple, flexible and general so it can be adjusted to fit different physical memristive devices.

In this work, we have studied the most popular memristor models, HP model [20], VTEAM model [29] and EGM model [18], in order to explore the most appropriate model to operate as a synapse component for neuromorphic systems. Table 1 gives a comparison of these models, we note that the first model [20] has very limited parameters and does not include threshold voltage, it contains only five parameters which make it less flexible to be tuned and to fit multiple memristor device.

It's *I-V* curve show that the HP model does not correctly account for nonlinear behaviour of the experimental memristor device.

However, our simulation results prove that this model can support both LTP and LTD functions and we successfully validate the STDP mechanism.

The VTEAM model [29] is a voltage-controlled model, it is a general model, which can fit different memristor devices, but the application of a positive voltage allows it to decrease its conductance while the application of a negative voltage allows it to remains unchanged to its initial state. So, this model can only support LTD function. This affect the capability of the VTEAM model to validate the biological STDP rule, which is illustrated in our results in Fig.8b.

The EGM model [18] is flexible, it is a voltage-controlled model, and general, it can fit various memristive devices. The simulated *I–V* characteristics of this model with a symmetric curve corresponds well with the experimental data of the Ta_2O_5-RRAM memristor device. Furthermore, the gradual conductance decrease and increase of the EGM model show that this model can exhibit the two synaptic functions LTP and LTD. This prove that we can implement and validate the STDP learning rule.

Fig. 9 shows the relative variation curves of the STDP of the three implemented memristor models.

We prove from our previous results that the first model can validate the biological STDP mechanism but it has various convergence problems and it is less flexible. The second model is general and flexible but it cannot support LTP function, so in our opinion, the VTEAM model cannot implement the STDP rule in a good way such as biological synapses. The EGM model can show several characteristics which make it a good candidate to act as synapse component. As shown in Fig. 9, we prove that this model can implement the STDP function in a similar way to biological synaptic systems [2]. These characteristics make the EGM model the most effective and acceptable model that can be used to validate the synaptic functions and then to successfully perform neuromorphic circuits.

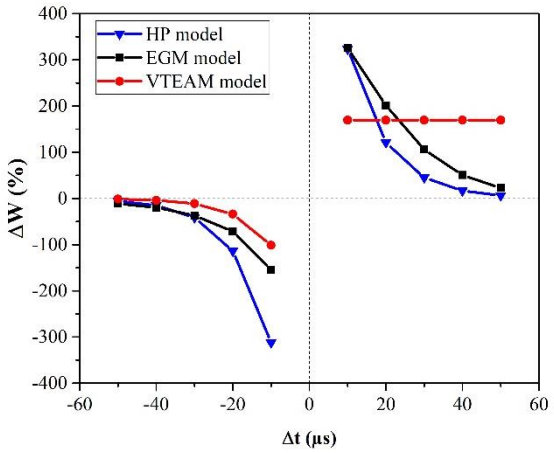

Fig. 9. The relative STDP curves for HP model, VTEAM model and the EGM model.

6. Conclusion

The memristive synapses play a key role in performing neuromorphic circuits, their plasticity is obtained by a variation in memristance values based on the temporal coincidences of the pre- and post-synaptic points. In order to implement such systems, an effective memristor model is needed, in this article, we analyze the fundamental characteristics of three of the most known memristor models, the linear ion drift model (HP), the Voltage ThrEshold Adaptive Memristor (VTEAM) model and the Enhanced Generalized Memristor (EGM) model. We tested their capability to imitate synaptic functions. We compared their I-V characteristics to an experimental result. Then we examined their gradual conductance modulation to prove the LTP and LTD functions which was achieved by modulating the polarity and amplitude of the applied pulses. Based on the conductance modulation of each model, we validate the STDP learning rule. From our simulation results, we note that the obtained *I–V* characteristics of the EGM model corresponds well with the experimental data of the Ta_2O_5-RRAM memristor device. It can demonstrate both LTP and LTD functions, which leads to the validation of the STDP learning rule. Hence, the EGM model is the most suitable model to mimic synaptic functions and then to be used in neuromorphic circuits.

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Figures

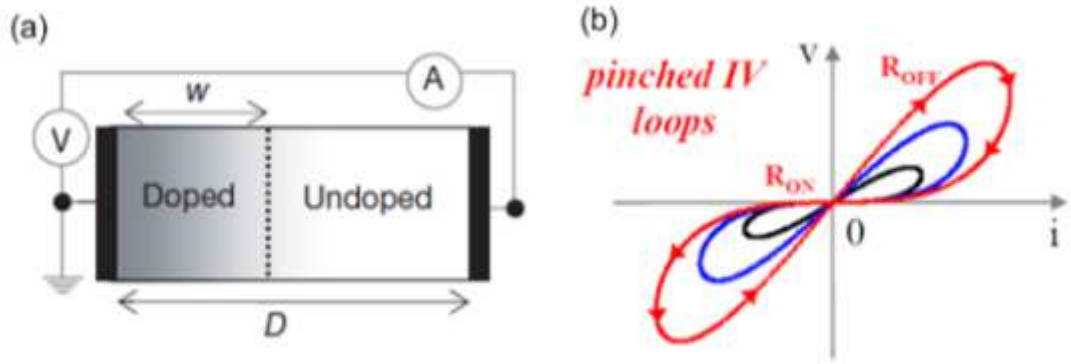

Figure 1

(a) Structure of the HP TiO2 memristor [2] (b) The memristor pinched I-V loop.

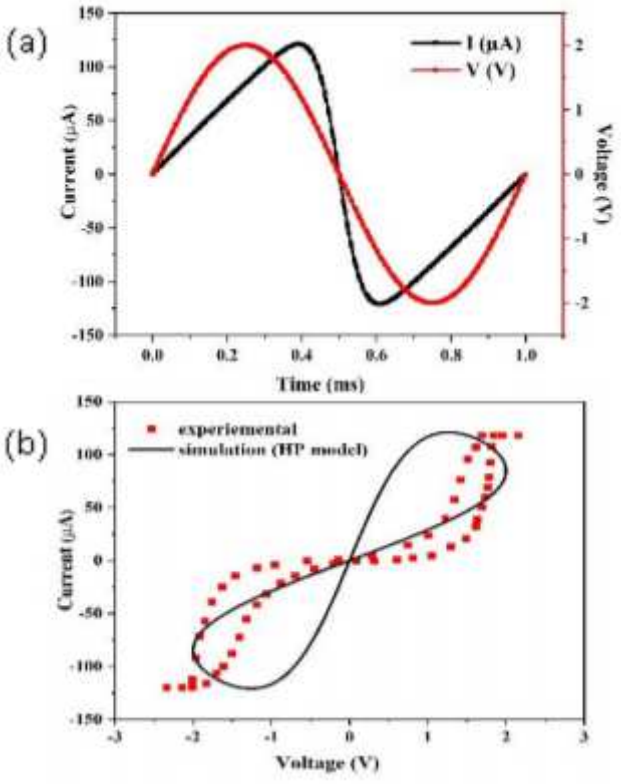

Figure 2

(a) Current and voltage curves of the simulated HP model versus time, (b) The experimental I-V curve of Ta2O5-RRAM memristor device compared with the simulated results of the HP model.

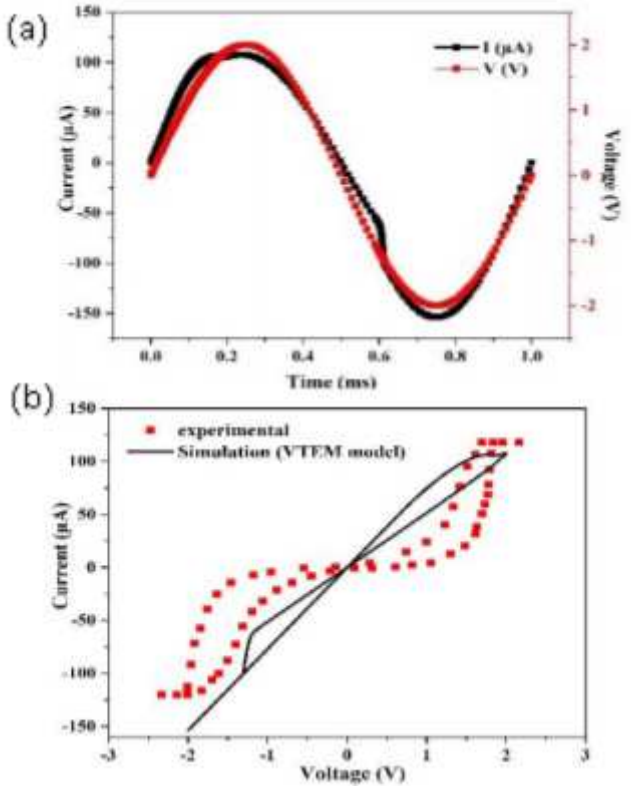

Figure 3

(a) Current and voltage curves of the simulated VTEAM model versus time, (b) The experimental I-V curve of Ta2O5-RRAM memristor device compared with the simulated results of the VTEAM model

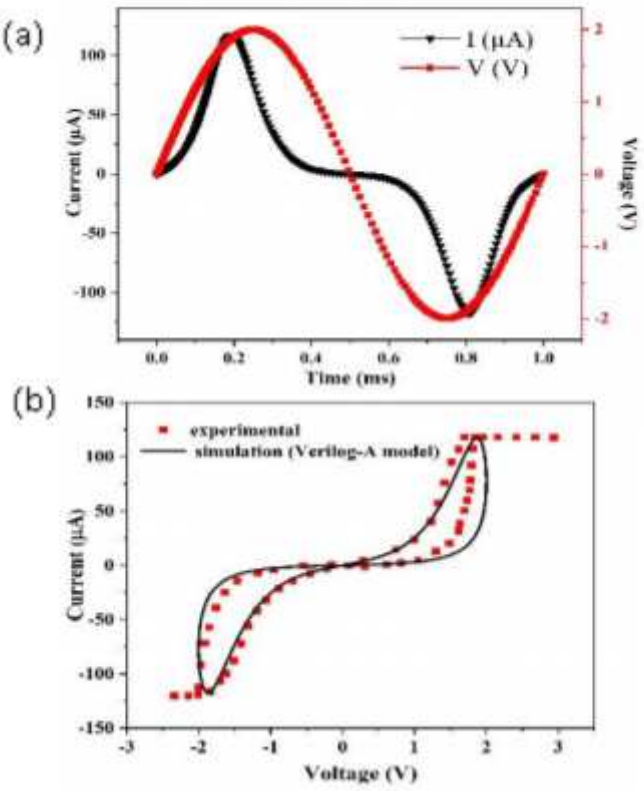

Figure 4

(a) Current and voltage curves of the EGM model versus time, (b) The experimental I-V curve of Ta2O5-RRAM memristor device compared with the simulated results of the EGM model.

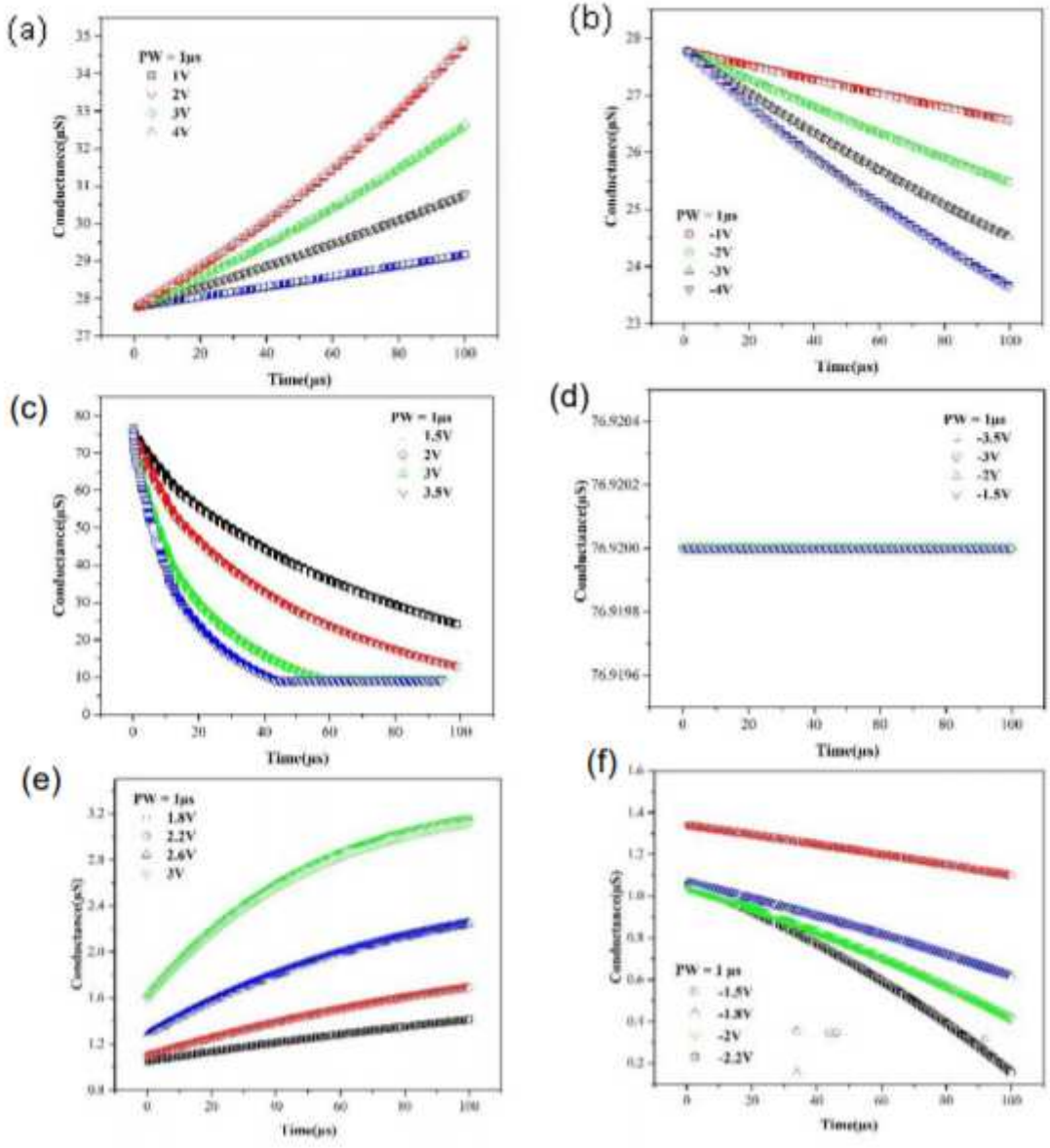

Figure 5

Curves of the conductance change for a voltage sweeping. Potentiations and depressions: (a), (b) for HP model, (c), (d) for the VTEAM model and (e), (f) for the EGM model.

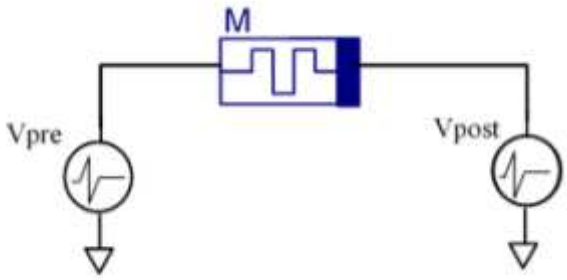

Figure 6

Design circuit of the memristor synapse.

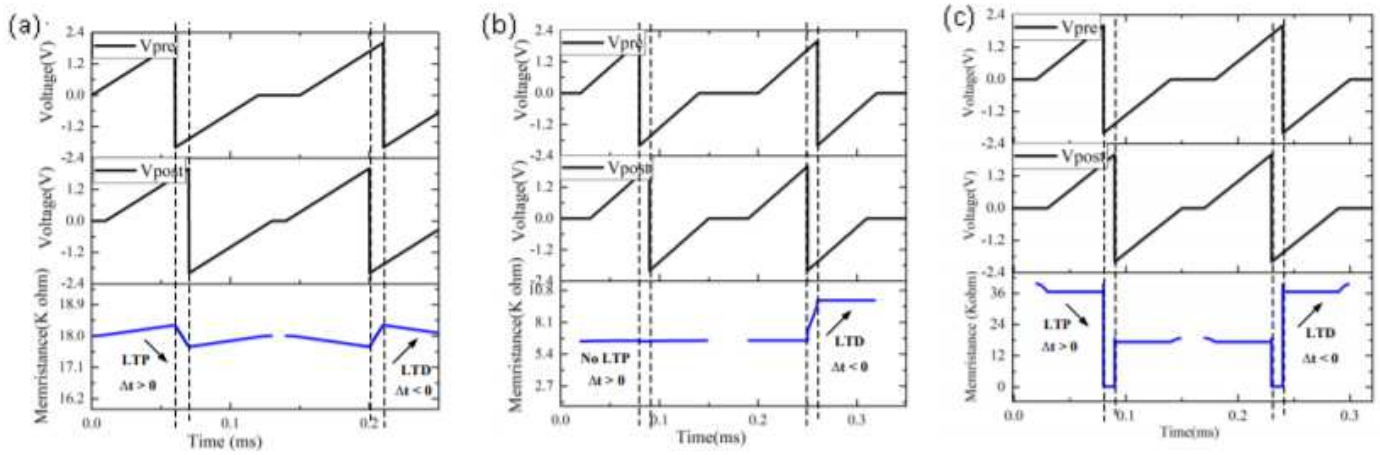

Figure 7

Simulation results of STDP test circuit given pre voltage spikes, post voltage spikes and the memristance evolution: (a) HP model, (b) VTEAM model (c) EGM model

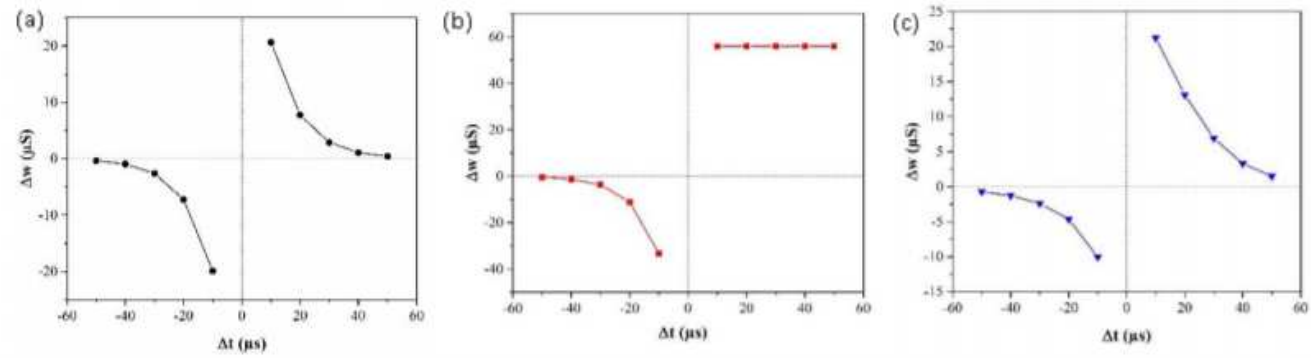

Figure 8

Represent the STDP simulation results: (a) HP model, (b) VTEAM model, (c) EGM model

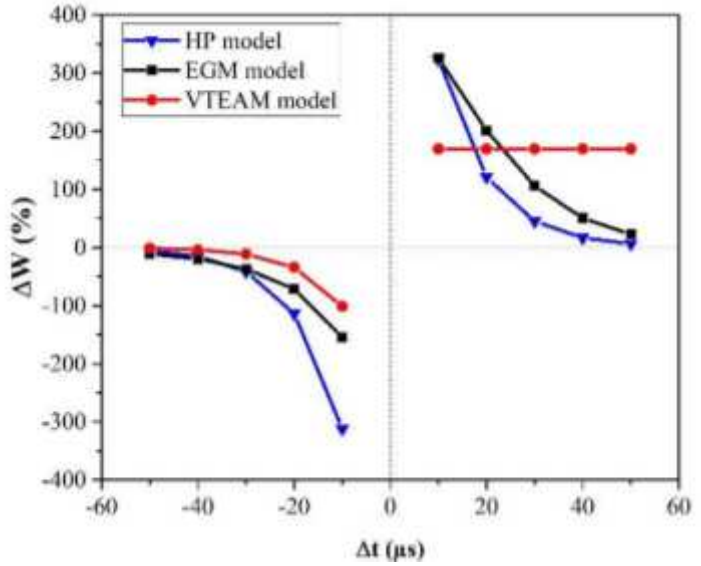

Figure 9

The relative STDP curves for HP model, VTEAM model and the EGM model.