Design of CNTFET Based Domino Wide OR Gates Using Dual Chirality for Reducing Subthreshold Leakage Current

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Abstract

The leakage current is prime concern in the modern portable battery operated device. However, various techniques are presented and performance is evaluated using MOSFET and FinFET devices. To further reduce leakage current for improved battery backup in portable devices, new devicesnamely Carbon Nano Tube Field Effect transistors (CNTFETs) can be used for design of different digital circuits. In this paper, subthreshold leakage power of dual chiral CNTFET based domino circuit is investigated and also the results are compared with single chiral CNTFET domino circuits. For better performance, threshold voltage of CNTFET in critical path is varied by changing the diameter or chirality of carbon nanotube. Subthreshold leakage power saving in dual chiral standard and LECTOR based domino circuits for OR2, OR4, OR8 & OR16 for low temperature (25°C) & low input ranges from 90.36- 95.96% and from 91.97-97.3%; for low temperature & high input ranges from 90.66-95.23% and from 92.85-96.39%; for high temperature (110°C) & low input ranges from 89.24- 99.73% and from 27.5-99.83%; for high temperature & high input ranges from 89.65-97.86% and from 91.85-99.76% when compared with single chiral standard and LECTOR based domino circuits respectively.

Highlights

The major contributions of the paper are as follows:

1. A comprehensive analysis on the state-of-the-art leakage reduction techniques.
2. An analysis of the leakage reduction using CNTFET devices.
3. An improved leakage reduction technique using dual chiral CNTFET in standard footerless and LECTOR based domino circuits.
4. The simulation results show subthreshold leakage current reduction upto 97.3% at 25°C and 99.76% at 110°C.

1. Introduction

Due to the scaling limit, conventional CMOS (Complementary Metal Oxide Semiconductor) and FinFET (Fin- Field Effect transistors) technology needs to be replaced with highly efficient Carbon Nano Tubes FETs(CNTFETs). The CNTFET based domino logic circuits can show drastic improvement in power consumption due to ballistic transport phenomenon of charge carriers in CNTFET.This section first presents various characteristics of CNTs followed by the discussion on subthreshold leakage on CNTFETs.

1.1 CNTs and its Characteristics

According to structure, CNTsare oftwo types: Single Walled CNT (SWCNT) and Multi Walled CNT(MWCNT). The SWCNT is constructed from one atom thick graphene sheet rolled in cylindrical tube. When graphene sheet is rolled across three different axes SWCNT can be classified as zigzag (n,0), armchair (n,n) and chiral (n,m) as shown in Fig.1. Equation of three different axes known as chiral vector ($\vec{C}$)[1,2,3] is defined by Eq. (1)

$$\vec{C} = n\vec{a}_1 + m\vec{a}_2$$

where n and m are integers, $\vec{a}_1$ and $\vec{a}_2$ are unit vectors.

For dual chirality, different threshold voltage is achieved by varying CNT diameters. When diameter of CNT is reduces, threshold voltage of CNTFET is increases. The diameter [1,2,3] of a carbon nanotube is given by Eq. (2).

$$d = \frac{a}{\pi}\sqrt{(n^2 + nm + m^2)}$$

where a=0.246 nm and n & m are chiral vector integers.

1.2 Subthreshold Leakage Current Characteristics

Fig. 2 (a) and 2 (b) shows subthreshold current flow in n-type CNTFET and p-type CNTFET transistor. In n-type CNTFET, when gate terminal is set to '0' or low, thetransistor is in OFF state and ideally no current flows from source to drain but practically very small current flows between them due to short channel effects (SCEs). This current is known as subthreshold leakage current. In p-type CNTFET, gate terminal is set to high to move transistor in OFF state where subthreshold leakage current flow from source to drain.

The V-I characteristics of n-CNTFET and p-CNTFET is shown in Fig. 3(a) and Fig. 3(b), respectively. As shown in Fig. 3(a), in n-CNTFET for high values of n (chiral vector integer) when source voltage increases subthreshold current increases rapidly but after one point slope of subthreshold current reduces rapidly with the change in source voltage. When chiral vector integer n reduces or in other words diameter of CNT reduces, subthreshold current also decreases. Further, reduction in chiral vector integer does not make remarkable in subthreshold current. As shown in Fig. 3(a), for n=13 to n=7 the magnitude of subthreshold current is almost same and fall in the same line.

As shown in Fig. 3(b), subthreshold current increases gradually with source voltage in p-CNTFET. But in case of chiral vector integer n=19 when source voltage increases beyond 0.8V sudden breakdown occurs and large amount of subthreshold current flows. When CNT diameter reduces subthreshold current decreases by very small amount and cannot be distinguished, hence subthreshold current lines overlapped. From here, it is concluded that n=13 or 11 are best suited values for subthreshold leakage reduction.

The paper is organized as follows. Section 2 provides literature review wherase Section 3 describes the proposed techniques. Results and discussion are given in section 4. Finally, Section 5 concludes the paper.

2. Literature Review

The leakage current is prime concern fordesign engineers and therefore signification attention is captured by the researchers across the globe. However, various reduction techniques are presented in the literature; it is still high and motivates us for further work which is summarized in this section. A lector stacking technique for gate oxide and subthreshold leakage current reduction is presented in [4] where p- and n-type leakage control transistors (LCTs) are introduced between pull-up and pull-down network of domino circuit. In this circuit, each LCT gate is controlled by source terminal signal of other transistor. In this technique, either n-type or p-type transistor operates near its cut-off region for any combination of inputs which leads to higher resistance between supply and ground thus reducing leakage current. Moreover, in inverter circuit a footed-diode transistor is inserted between n-type transistor and ground which offer more resistive path between supply and ground to suppress leakage current at the inverter. According to Kao *et al.*[5] several dual threshold voltage techniques exist which reduces total leakage power included high performance maintaining in static and dynamic combinational logic circuits. In [5], a domino

circuit simulated on three circuit variants: first all transistors with low threshold voltage, second all the transistors with high threshold voltage and third dual threshold voltage with three different modes evaluation, precharge and standby. The results found that low threshold voltage design is faster than high threshold voltage.

Gupta *et al.* [6] enhance their previous work with dual threshold voltage technique and removed footed-diode transistor from inverter and analyzed in four different states CHIL (Clock high and inputs are low), CHIH (clock high and inputs are high), CLIL (clock low and inputs are low) and CLIH (clock low and inputs are high). It is shown that CHIH state is effective to suppress the leakage at low temperature and CHIL is ineffective. At high temperature CHIH is preferred for high fan-in and CLIL is preferred for low fan-in. According to Zhou *et al.* [7] for CMOS circuit multi-threshold CMOS technology is an effective method to reduce subthreshold leakage power which satisfies design of low power and high performance requirements. Garg *et al.*[8] proposes Foot Driven Stack Transistor Domino Logic (FDSTDL) for designing CMOS domino logic gates which reduces leakage power with better noise performance. Asyaei [9] presented a new leakage tolerant domino circuit that provides higher noise immunity with lower power consumption and without significant delay increment for wide fan-in gates. Further in [10], a new charging scheme is presented that reduces power consumption of dynamic circuit where dynamic node discharges frequently and suitable for large fan-in gates. All these works are contributed for CMOS technology, further many circuits proposed in FinFET technology node. Moradi *et al.* [11] designed high performance domino circuits including leakage and proposed several logic circuits using FinFET device which is useful for reducing total leakage power. Magraiya *et al.* [12,13] also worked for reduction of subthreshold leakage power in FinFET domino circuits with the help of ONOFIC & ONOFIC pull-up approach and achieved subthreshold leakage reduction.

Further, some works are going on CNTFET devices are related to device level modification. According to Avshish Kumar *et al.*[14] single wall carbon nanotube field effect transistors (CNTFETs) have clear advantage over MOSFETs particularly performance is improved related to on currentwith respect to dielectric constant and gate insulator thickness.Hence, thinner gate oxide and larger CNT improves the performance of CNTFETs. Further, Junctionless ballistic carbon nanotube field-effect transistors (JL-CNTFET) [15] is proposed by Khalil Tamersit which mitigates ultrascaling effects and enhances performance subject to leakage current, subthreshold swing, switching speed and drain induced barrier lowering etc. and Electrostatic doped Schottky barrier carbon nanotube field effect transistor (EDSBCNTFET) [16] is proposed by Amandeep Singh *et al.* for low power memory design by leakage power reduction and better stability.

It is observed from the above research work that the existing leakage reduction techniques with CMOS & FinFET devices are still not minimizing the leakage current efficiently. Further there is very less analysis on the leakage current of circuits with CNTFETs. Therefore, this paper presents new dual chiral CNTFET based domino circuits and provides a critical analysis to minimize leakage current.

3. Proposed Cntfet Domino Circuits

To address the aforementioned leakage current problem in the recent devices, new dual chiral CNTFET based two different standard and LECTOR domino OR circuitsare proposed. To differentiate high threshold transistors from low threshold transistors thickness of tube is reduced as shown in Fig. 4(b) and Fig. 6(b).

3.1 Standard Domino CNTFET OR Gate

A generalized circuit diagram for 2 inputs standard footerless domino OR gate is shown in Fig.4(a) having same threshold voltage or single chiral tubes are used whereas Fig.4(b) shows proposed dual chiral footerless domino CNTFET circuit. In dual chiral, carbon nanotube diameters of clock transistor CN1, keeper transistor CN2 and inverter transistor CN4 are varied by changing the chiral vector. Due to this, carbon nanotube diameter reduces and flow of drain current in the transistor also reduces.

The working of a dual chiral CNTFET domino circuit is same as standard domino circuit: when clock is low (clk=L), the high threshold precharge transistor CN1 is ON which charges the dynamic node; this is called precharge phase. During this precharge phase, output node goes low and high threshold CN2 transistor turns ON, maintaining the dynamic node in high state. Output of domino logic is independent of the inputs applied in the evaluation transistors, whereas only the leakage current is dependent on the input vectors applied. On the other hand, when the clk=H, transistor CN1 is OFF and CN2 is dependent on the output of the domino circuit; this is called evaluation phase. Charging of dynamic node will depend on the input vectors applied and according to output node condition which will be low or high. Flow of subthreshold current is shown in Fig.5 using dashed arrow for low and high inputs.

The next subsection presents the LECTOR based dual chiral CNTFET domino circuits to minimize the leakage.

3.2 LECTOR Domino CNTFET OR Gate

In this section LECTOR based 2-input domino OR CNTFET both for single and dual chiral vector is shown in Fig. 6(a) and (b) respectively. Earlier Gupta *et al.* [6] had presented the same logic for domino logic in CMOS technology for reduction of subthreshold and gate oxide leakage currents. But in case of CNTFET subthreshold leakage is the dominant parameter of the total leakage current, hence the focus of this work is to investigate and reproduce the same logic in case of CNTFET. In Fig. 6(b) dual chiral carbon tubes are used with clock transistor CN1, keeper transistor CN2, inverter transistor CN5 and evaluation transistors CN7 & CN8.

The proposed dual chiral LECTOR domino CNTFET circuit effectively reduces subthreshold leakage power. In this technique, low threshold transistor CN4 and CN6 are leakage control transistors (LCTs) [4]. The proposed dual chiral LECTOR domino gate operates similarly to proposed dual chiral standard footerless CNTFET domino gate. In the proposed circuit, when clock is low (clk=L), the dynamic node is charged through the high threshold transistor CN1 and low threshold transistor CN4. This charging is independent of the input state of previous clock. Suppose the inputs are low before the clk=L, node N2 will be at low potential and low threshold transistor CN4 offers a very low resistance path for charging of the dynamic node. If inputs are high before clk=L, then node N2 potential is not sufficient to turn completely OFF the low potential transistor CN4 (operating near cut-off region). The resistance of CN4 will be less than its OFF resistance which allows charging of the dynamic node. This case is known as precharging phase and output is independent of inputs of the evaluation network, whereas only the leakage current is dependent.

Now, when clk=H or circuit is in standby mode known as evaluation phase.In this phase, output is depending on the inputs. If all the inputs are low, the dynamic node will not be discharged by the evaluation network and the output of the inverter will be low and it turns ON the high threshold transistor CN2, the voltage at node N1 will turn ON the high threshold transistor CN5, but the voltage induced at node N2 will not enough to cut-off the transistor CN4, which will operate near the cut-off region, offering a high resistance path between Vdd and ground, thus reducing subthreshold leakage current.

When all or any one the input is high, the dynamic node will be discharged through the evaluation network. The transistor CN2 will turn OFF the voltage at node N1 and will operate the transistor CN6 near its cut-off region (offering high resistance). The potential at node N2 will turn ON the transistor CN4. Therefore, the introduction of low threshold LCTs increases the resistance between Vdd and ground in addition with propagation delay of the domino circuit. Flow of subthreshold current in dual chiral LECTOR based OR CNTFET for low and high inputs are shown in Fig. 7(a) and (b) respectively. These circuits reduce the leakage current significantly and can be effectively employed for low power designs. The next section presents the efficacy of the proposed work with simulation results.

4. Results And Discussion

To evaluate the performance of the proposed technique, zigzag (n,0) CNTFET based domino OR gates are designed for 2, 4, 8 and 16 inputs using single threshold voltage (single chiral) and dual threshold voltage (dual chiral) CNTFETs. Stanford CNTFET Model for 32 nm [17] is used for simulating the standard and LECTOR circuits for accurate estimation of active power, delay and subthreshold currents. All the existing and proposed circuits are simulated at Vdd = 0.9V, 4nm gate width for 2, 4, 8 and 16-input domino OR gates. For reasonable comparison, the sizing of the n-CNTFETs and p-CNTFETs are kept same in the existing and proposed dual chirality circuits. Active power consumption and delay is measured by applying a clock period of 5ns with 50% duty cycle and simulation runs for 100ns. The active power consumption and delay are compared withstandard, LECTOR and proposed dual chiraldomino OR gates (2, 4, 8 and 16 inputs) for low and high inputs. Subthreshold current is measured at 0.9V using dc analysis by varying supply from 0 to 0.9 dc voltage and setup the inputs either low or high. For single chiral circuits all the CNTFETs have equal diameters of chiral vector integer is (19,0). For dual chiral some of the transistor CNT diameters are changed in the circuit by changing the chiral integer n = 19 value to 15, 13,11, 9 and 7.

4.1 Power Consumption and Delay Analysis

At 25°C active power consumption and delay of the CNTFET domino circuits is shown in Table 1 and Table 2 respectively. The result shows that the active power consumption in the CNTFET domino circuit is increased with number of input. For chiral vector integer n = 7 minimum active power consumption is achieved, when compared to other combinations of different chiral vectors. This is due to the fact that low chiral indices offer higher threshold voltages. The delay is increased when chiral vector integer is varied from n = 19 to n = 7. This is also due to the same reason mentioned in regards to active power consumption and hence we can see a trade-off between power and delay with the variation of chiral indices vector in CNTFET.

Table 1
Active power consumption of Standard and LECTOR domino OR gates with proposed chirality variation

Active Power (nW)	No. of inputs	Single V_t (n = 19)	Dual V_t (n = 19 & 15)	Dual V_t (n = 19 & 13)	Dual V_t (n = 19 & 11)	Dual V_t (n = 19 & 9)	Dual V_t (n = 19 & 7)
Standard	**OR2**	2.60	11.72	8.31	7.04	12.21	5.40
	OR4	13.45	10.76	10.10	12.03	10.31	5.40
	OR8	17.32	11.73	12.08	10.75	10.06	6.60
	OR16	23.84	25.15	17.03	34.96	10.95	8.89
LECTOR	**OR2**	24.95	12.30	11.82	10.46	6.81	6.99
	OR4	21.81	14.18	11.54	1.37	5.41	5.81
	OR8	22.09	17.82	12.46	11.25	24.16	6.01
	OR16	23.10	7.17	3.82	9.98	20.19	12.05

Table 2
Delay of standard and LECTOR domino OR gates with proposed chirality variation

Delay (ps)	No. of inputs	Single V_t (n = 19)	Dual V_t (n = 19 & 15)	Dual V_t (n = 19 & 13)	Dual V_t (n = 19 & 11)	Dual V_t (n = 19 & 9)	Dual V_t (n = 19 & 7)
Standard	**OR2**	1.23	1.35	1.46	1.69	3.22	9.35
	OR4	1.11	1.27	1.39	1.68	3.38	10.25
	OR8	1.25	1.28	1.48	1.76	3.91	12.02
	OR16	1.08	1.36	1.56	8.71	4.61	15.05
LECTOR	**OR2**	4.37	4.11	4.15	4.79	8.86	28.38
	OR4	3.43	3.65	3.79	4.54	8.82	28.61
	OR8	3.16	3.50	3.76	4.67	9.26	30.84
	OR16	3.05	3.62	4.02	4.99	10.19	35.64

Power delay product (PDP) of the standard and LECTOR based domino logic for single and dual V_t is shown in Table 3. Here it is calculated that the PDP is increased with the number of inputs and with the decrease of chiral index vector both for standard and LECTOR based domino logic.

Table 3
Power delay product (PDP) of standard and LECTOR domino OR gates with proposed chirality variation

PDP (zJ)	No. of inputs	Single V_t (n = 19)	Dual V_t (n = 19 & 15)	Dual V_t (n = 19 & 13)	Dual V_t (n = 19 & 11)	Dual V_t (n = 19 & 9)	Dual V_t (n = 19 & 7)
Standard	**OR2**	3.20	15.82	12.11	11.91	39.28	50.50
	OR4	14.93	13.71	14.07	20.26	34.88	55.34
	OR8	21.63	15.00	17.84	18.91	39.37	79.30
	OR16	25.70	34.18	26.60	304.61	50.49	133.80
LECTOR	**OR2**	109.01	50.49	49.07	50.10	60.32	198.36
	OR4	74.72	51.69	43.75	6.23	47.70	166.21
	OR8	69.78	62.32	46.80	52.55	223.65	185.33
	OR16	70.48	25.96	15.36	49.79	205.80	429.51

4.2 Subthreshold Leakage Power Consumption at Low Temperature (25°C)

Subthreshold leakage power saving in proposed dual chiral standard footerless and LECTOR domino OR gates in comparison to single chiral domino gates for both low and high inputs are shown in Table 4. The graphical representations of the same for low and high inputs are shown in Figs. 8 and 9 respectively.

Table 4
Percentage Subthreshold leakage power saving in proposed dual chiral standard footerless and LECTOR based domino OR gates with respect to single chiral domino for low and high inputs at 25°C

Sub-threshold leakage	No. of inputs	Compared with standard single chiral domino					Compared with LECTOR based single chiral domino				
		Dual V_t (n = 19 & 15)	**Dual V_t (n = 19 & 13)**	**Dual V_t (n = 19 & 11)**	**Dual V_t (n = 19 & 9)**	**Dual V_t (n = 19 & 7)**	**Dual V_t (n = 19 & 15)**	**Dual V_t (n = 19 & 13)**	**Dual V_t (n = 19 & 11)**	**Dual V_t (n = 19 & 9)**	**Dual V_t (n = 19 & 7)**
Low inputs	**OR2**	90.36	94.80	94.68	94.67	94.67	91.97	96.34	96.42	96.43	96.43
	OR4	92.54	95.96	95.86	95.86	95.86	94.59	97.26	97.29	97.30	97.30
	OR8	91.04	95.14	95.02	95.01	95.01	93.32	96.48	96.49	96.50	96.50
	OR16	90.50	94.84	94.71	94.71	94.71	92.82	96.17	96.14	96.14	96.15
High inputs	**OR2**	90.66	95.23	95.10	95.09	95.09	92.85	96.39	96.30	96.29	96.29
	OR4	90.66	95.23	95.10	95.09	95.09	92.85	96.39	96.30	96.29	96.29
	OR8	90.66	95.23	95.10	95.09	95.09	92.85	96.39	96.30	96.29	96.29
	OR16	90.66	95.23	95.10	95.09	95.09	92.85	96.39	96.30	96.29	96.29

From Table 4 it is found that at low temperature for low inputs, dual chiral standard footerless CNTFET domino OR gates for chiral vector integer n = 19&15 subthreshold leakage power saving is from 90.36–92.54%; for n =

19&13 subthreshold leakage power saving is from 94.8–95.96%; for n = 19&11, 19&9, and 19&7 subthreshold leakage power saving is in all three cases is almost same from 94.67–95.86%. From the results it is found that for chiral integer vector n = 19&13 maximum subthreshold leakage power saving is achieved, as shown in Fig. 8(a).

Also from Table 4 it is found that at low temperature for low inputs, dual chiral LECTOR based CNTFET domino OR gates for chiral vector integer n = 19&15 subthreshold leakage power saving is from 91.97–94.59%; for n = 19&13 subthreshold leakage power saving is from 96.17–97.26%; for n = 19&11, 19&9, and 19&7 subthreshold leakage power saving is in all three cases is almost same from 96.14–97.30%. From the results it is found that maximum subthreshold leakage power saving for chiral integer vector n = 19&9and 19&7, as shown in Fig. 8(b).

Similarly, for high input at low temperature, dual chiral standard footerless CNTFET domino OR gates for chiral vector integer n = 19&15 subthreshold leakage power saving is 90.66%; for n = 19&13 subthreshold leakage power saving is 95.23%; for n = 19&11 subthreshold leakage power saving is 95.10%; for 19&9 and 19&7 subthreshold leakage power saving is in both two cases is same 95.09%. From the results it is found that for chiral integer vector n = 19&13 maximum subthreshold leakage power saving is achieved, as shown in Fig. 9(a).

Also from Table 4 it is observed that at low temperature for high inputs, dual chiral LECTOR based CNTFET domino OR gates for chiral vector integer n = 19&15 subthreshold leakage power saving is 92.85%; for n = 19&13 subthreshold leakage power saving is 96.39%; for n = 19&11 subthreshold leakage power saving is 96.30%; for 19&9 and 19&7 subthreshold leakage power saving is in both two cases is same 96.29%. From the results it is found that for chiral integer vector n = 19&11 maximum subthreshold leakage power saving is achieved, as shown in Fig. 9(b).

4.3 Subthreshold Leakage Power Consumption at High Temperature (110°C)

Subthreshold leakage power saving in proposed dual chiral standard footerless and LECTOR domino OR gates in comparison with single chiral domino gates for both low and high inputs are shown in Table 5. The graphical representations of the same for low and high inputs are shown in Figs. 10 and 11 respectively.

Table 5

Percentage Savings of subthreshold leakage power in proposed dual chiral standard footerless and LECTOR based domino OR gates with respect to single chiral domino for low and high inputs at 110°C

Sub-threshold leakage	No. of inputs	Compared with standard single chiral domino					Compared with LECTOR based single chiral domino				
		Dual V_t (n = 19 & 15)	**Dual V_t (n = 19 & 13)**	**Dual V_t (n = 19 & 11)**	**Dual V_t (n = 19 & 9)**	**Dual V_t (n = 19 & 7)**	**Dual V_t (n = 19 & 15)**	**Dual V_t (n = 19 & 13)**	**Dual V_t (n = 19 & 11)**	**Dual V_t (n = 19 & 9)**	**Dual V_t (n = 19 & 7)**
Low inputs	OR2	89.24	97.81	99.49	99.63	99.63	27.50	95.91	99.62	99.74	99.74
	OR4	92.27	98.40	99.63	99.73	99.73	92.77	98.69	99.76	99.83	99.83
	OR8	90.65	98.05	99.54	99.67	99.66	92.22	98.49	99.68	99.77	99.77
	OR16	90.07	97.92	99.51	99.64	99.64	92.01	98.42	99.65	99.75	99.75
High inputs	OR2	89.65	97.86	99.53	99.67	99.67	91.85	98.39	99.65	99.76	99.75
	OR4	89.65	97.86	99.53	99.67	99.67	91.85	98.39	99.65	99.76	99.75
	OR8	89.65	97.86	99.53	99.67	99.67	91.85	98.39	99.65	99.76	99.75
	OR16	89.65	97.86	99.53	99.67	99.67	91.85	98.39	99.65	99.76	99.75

From Table 5 it is observed that at high temperature for low inputs, dual chiral standard footerless CNTFET domino OR gates for chiral vector integer n = 19&15 subthreshold leakage power saving is from 89.24–92.27%; for n = 19&13 subthreshold leakage power saving is from 97.81–98.4%; for n = 19&11 subthreshold leakage power saving is from 99.49–99.63%; for n = 19&9 and 19&7 subthreshold leakage power saving is in both cases is same from 99.63–99.73%. From the results maximum subthreshold leakage power saving is found that for chiral integer vectors n = 19&9 and 19&7, as shown in Fig. 10(a).

Also from Table 5 it is found that at high temperature for low inputs, dual chiral LECTOR based CNTFET domino OR gates for chiral vector integer n = 19&15 subthreshold leakage power saving is from 27.5–92.77%; for n = 19&13 subthreshold leakage power saving is from 95.91–98.69%; for n = 19&11 subthreshold leakage power saving is from 99.62–99.76%; for n = 19&9 and 19&7 subthreshold leakage power saving is in both cases is same from 99.74–99.83%. From the results maximum subthreshold leakage power saving is found that for chiral integer vectors n = 19&9 and 19&7, as shown in Fig. 10(b).

Similarly, for high input at high temperature, dual chiral standard footerless domino OR gates for chiral vector integer n = 19&15 subthreshold leakage power saving is 89.65%; for n = 19&13 subthreshold leakage power saving is 97.86%; for n = 19&11 subthreshold leakage power saving is 99.53%; for n = 19&9 and 19&7 subthreshold leakage power saving is in both cases is same 99.67%. From the results, the maximum subthreshold leakage power saving is found for chiral integer vectors n = 19&9 and 19&7 as shown in Fig. 11(a).

Also from Table 5 it is found that at high temperature for high inputs, dual chiral standard footerless CNTFET domino OR gates for chiral vector integer n = 19&15 subthreshold leakage power saving is 91.85%; for n = 19&13 subthreshold leakage power saving is 98.39%; for n = 19&11 subthreshold leakage power saving is 99.65%; for n = 19&9 subthreshold leakage power saving is 99.76%; and for n = 19&7 subthreshold leakage power saving is

99.75%. From the results it is found that for chiral integer vector n = 19&9 provides maximum subthreshold leakage power savings, as shown in Fig. 11(b).

5. Conclusion

Dual chiral technique is a reliable technique to reduce subthreshold leakage power in CNTFET domino circuits. From result section it is verified that the dual chiral CNTFET domino OR gates reduces subthreshold leakage power at both low and high temperatures. At 25°C when inputs are low dual chiral standard footerless CNTFET domino subthreshold current is minimum for chiral vector integers n = 19 & 13 and achieve subthreshold leakage power reduction upto 95.96%; for dual chiral LECTOR based CNTFET domino subthreshold current is minimum for chiral vector integers n = 19 & 7 with subthreshold leakage power reduction upto 97.3%. At 25°C when inputs are high dual chiral standard footerless CNTFET domino subthreshold current is minimum for chiral vector integers n = 19 & 13 and achieve subthreshold leakage power reduction upto 95.23%; for dual chiral LECTOR based CNTFET domino subthreshold current is minimum for chiral vector integers n = 19 & 7 with subthreshold leakage power reduction upto 96.39%. At 110°C when inputs are low dual chiral standard footerless CNTFET domino subthreshold current is minimum for chiral vector integers n = 19 & 9 and achieve subthreshold leakage power reduction upto 99.73%; for dual chiral LECTOR based CNTFET domino subthreshold current is minimum for chiral vector integers n = 19 & 9 with subthreshold leakage power reduction upto 99.83%. At 110°C when inputs are high dual chiral standard footerless CNTFET domino subthreshold current is minimum for chiral vector integers n = 19 &9 and achieve subthreshold leakage power reduction upto 99.67%; for dual chiral LECTOR based CNTFET domino subthreshold current is minimum for chiral vector integers n = 19 &9 with subthreshold leakage power reduction upto 99.76%. Hence it is investigated that dual chiral CNTFET based circuits are worth like in CMOS technology and can be effectively utilized in designing of low power CNTFET circuits.

Declarations

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Consent to participation and publication

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Declaration of interests

- The authors have no relevant financial or non-financial interests to disclose.
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We the undersigned declare that the manuscript entitled “Design of CNTFET based Domino Wide OR Gates using Dual Chirality for Reducing Subthreshold Leakage Current” is original, has not been fully or partly published before and is not currently being considered for publication elsewhere.

We confirm that the manuscript has been read and approved by all named authors and that there are no other persons who satisfied the criteria for authorship but are not listed. We further confirm that the order of authors listed in the manuscript has been approved by all of us.

We understand that the Corresponding Author is the sole contact for the editorial process. The corresponding author "Vijay Kumar Magraiya" is responsible for communicating with the other authors about process, submissions of revisions and final approval of proofs.

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Figures

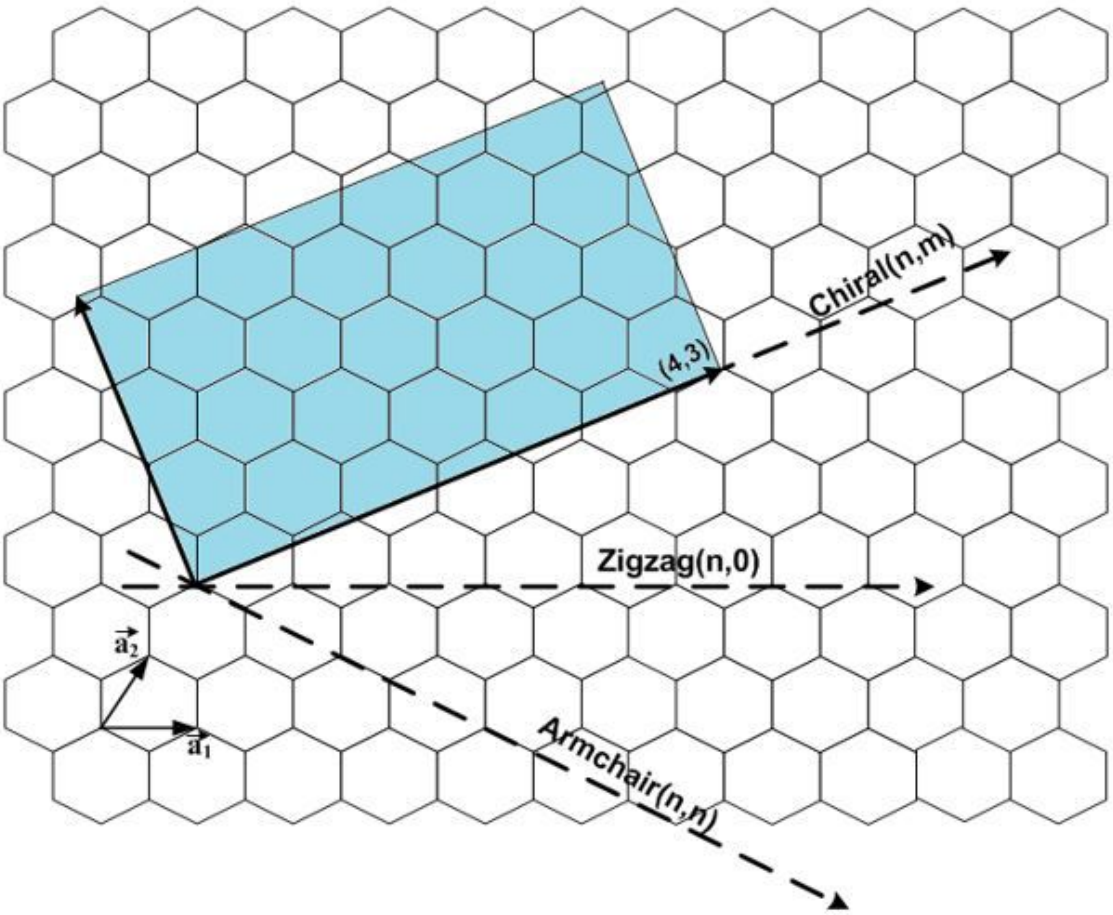


Figure 1

One atom thick graphane sheet for SWCNT construction

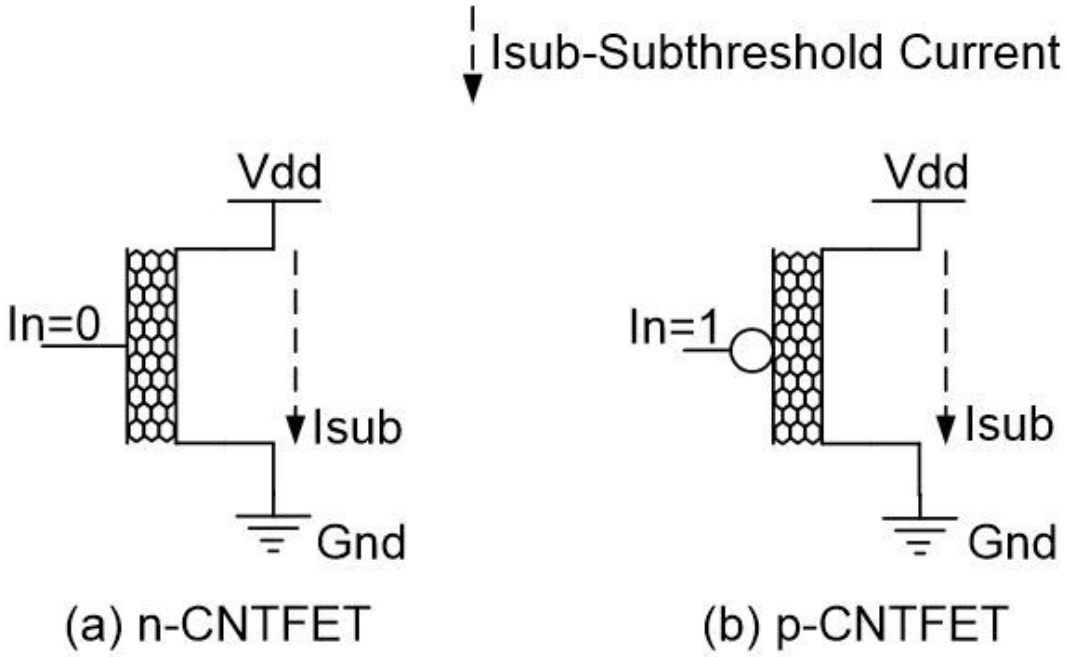


Figure 2

Condition of subthreshold current flow in n-CNTFET and p-CNTFET

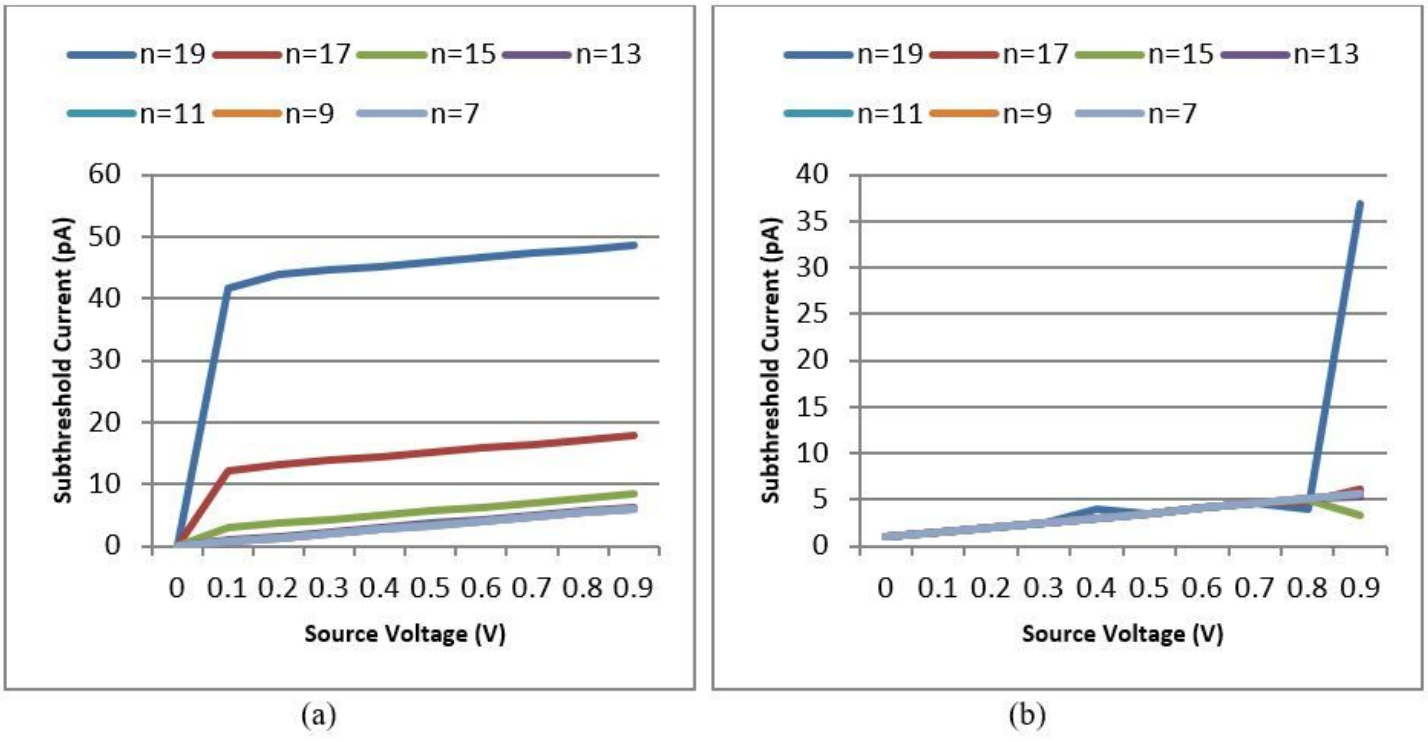


Figure 3

Plot of V-I characteristics (source voltage v/s subthreshold current) varying chiral vector integer (n): (a) n-CNTFET, (b) p-CNTFET.

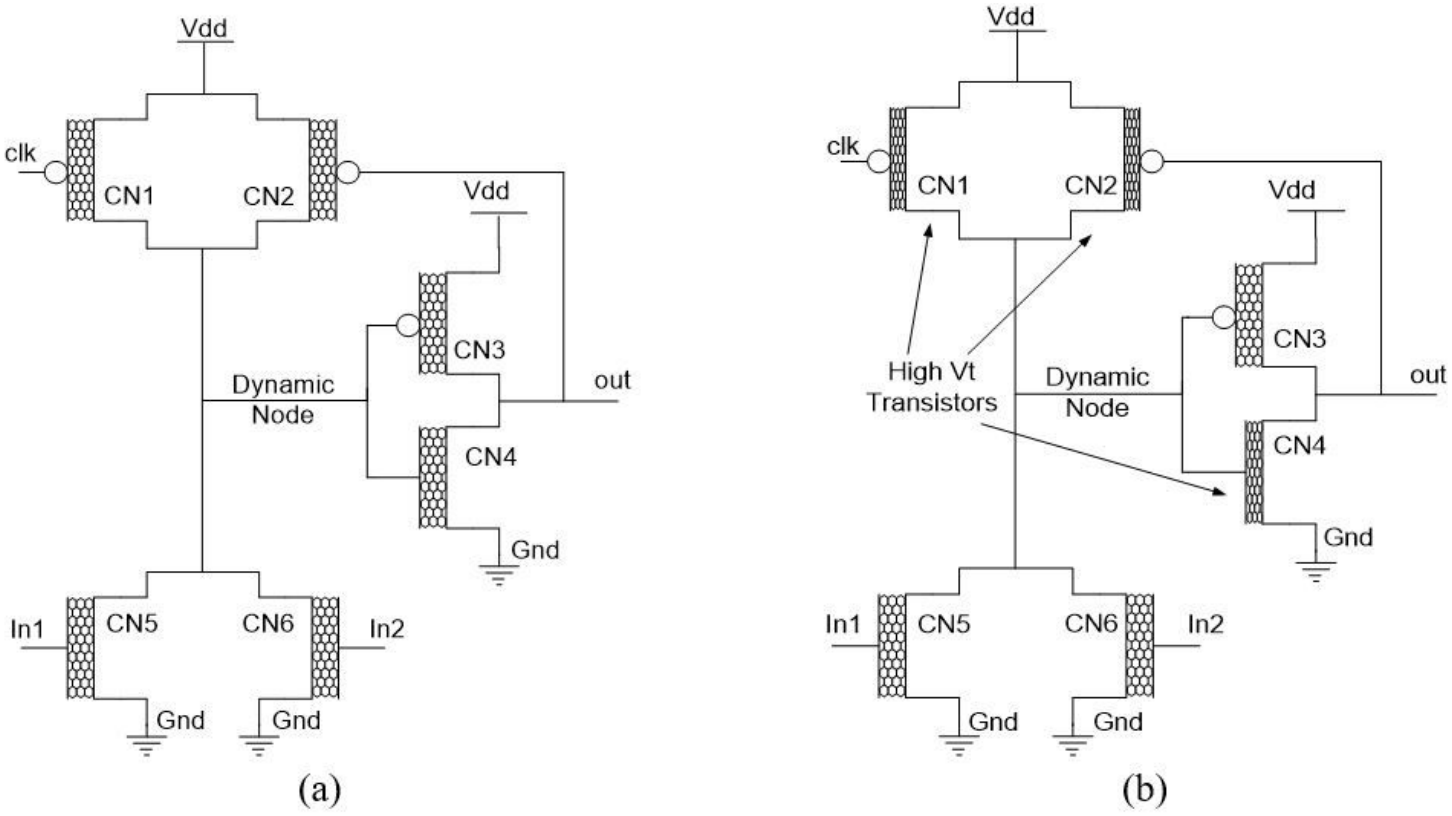


Figure 4

2-input domino OR CNTFET(a) Standard gate (b) Proposed dual chiralgate

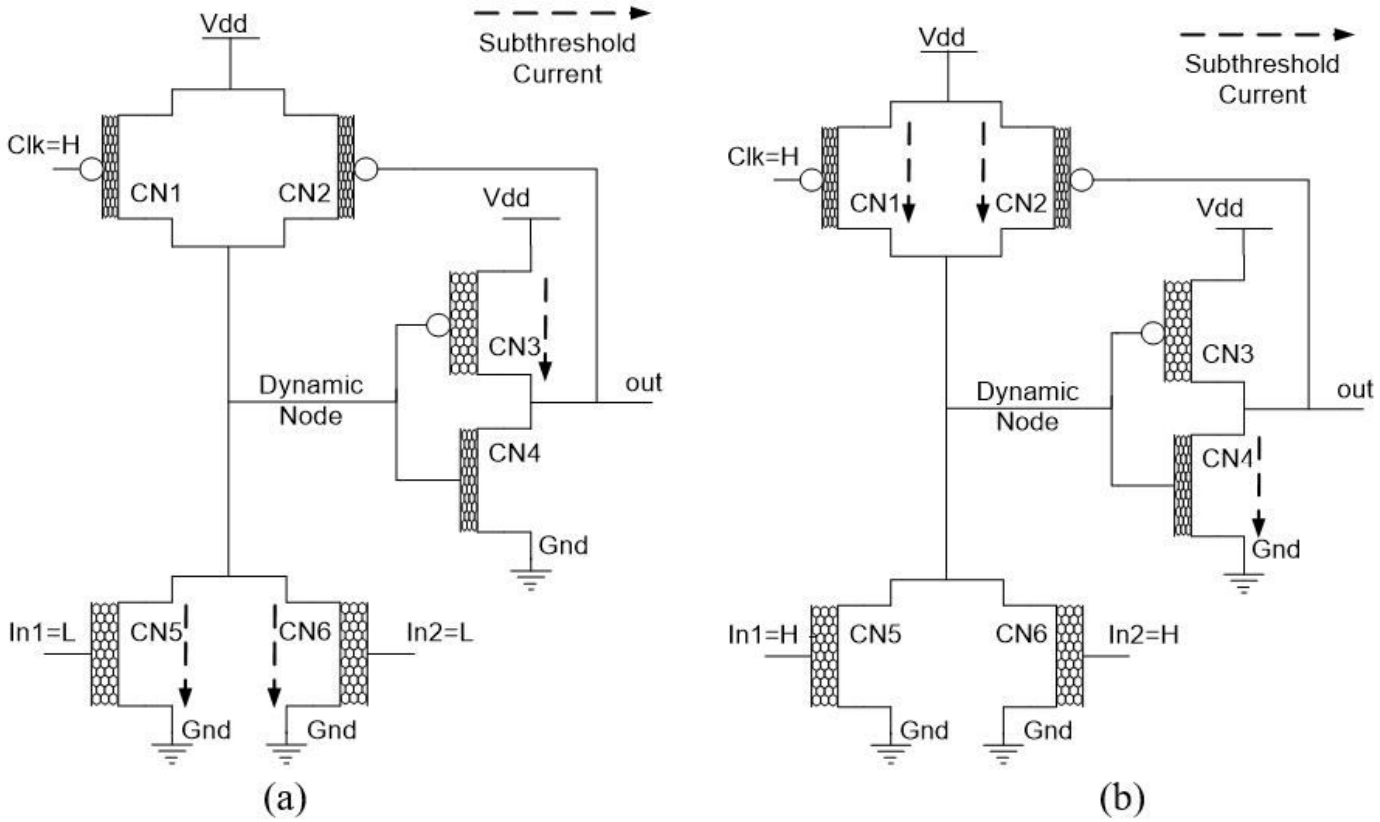


Figure 5

Flow of subthreshold current in proposed dual chiral domino OR CNTFET gate (a) low inputs (b) high inputs.

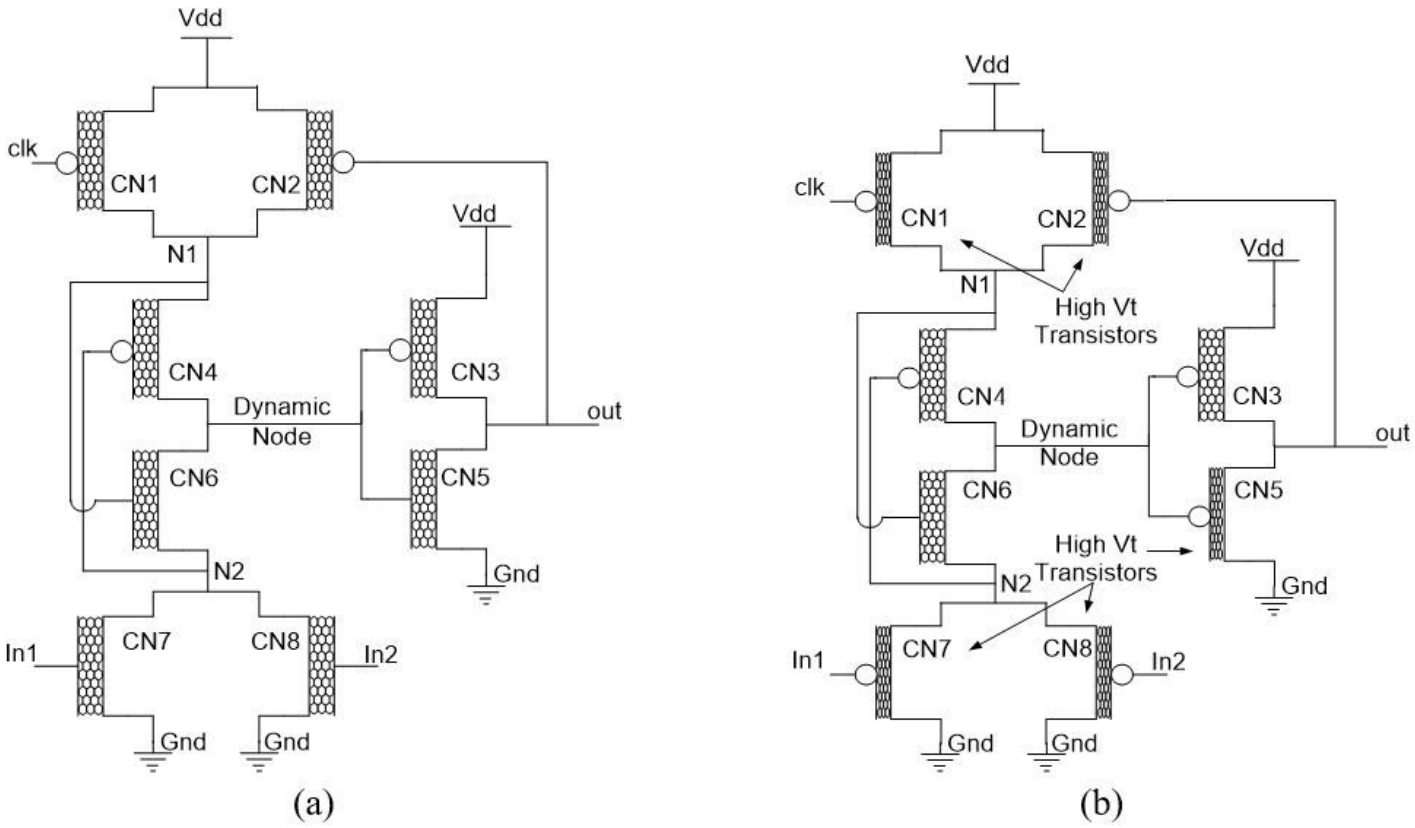


Figure 6

(a) LECTOR based 2- input domino OR CNTFET gate (b) Proposed 2-input dual chiral LECTOR based OR CNTFET gate

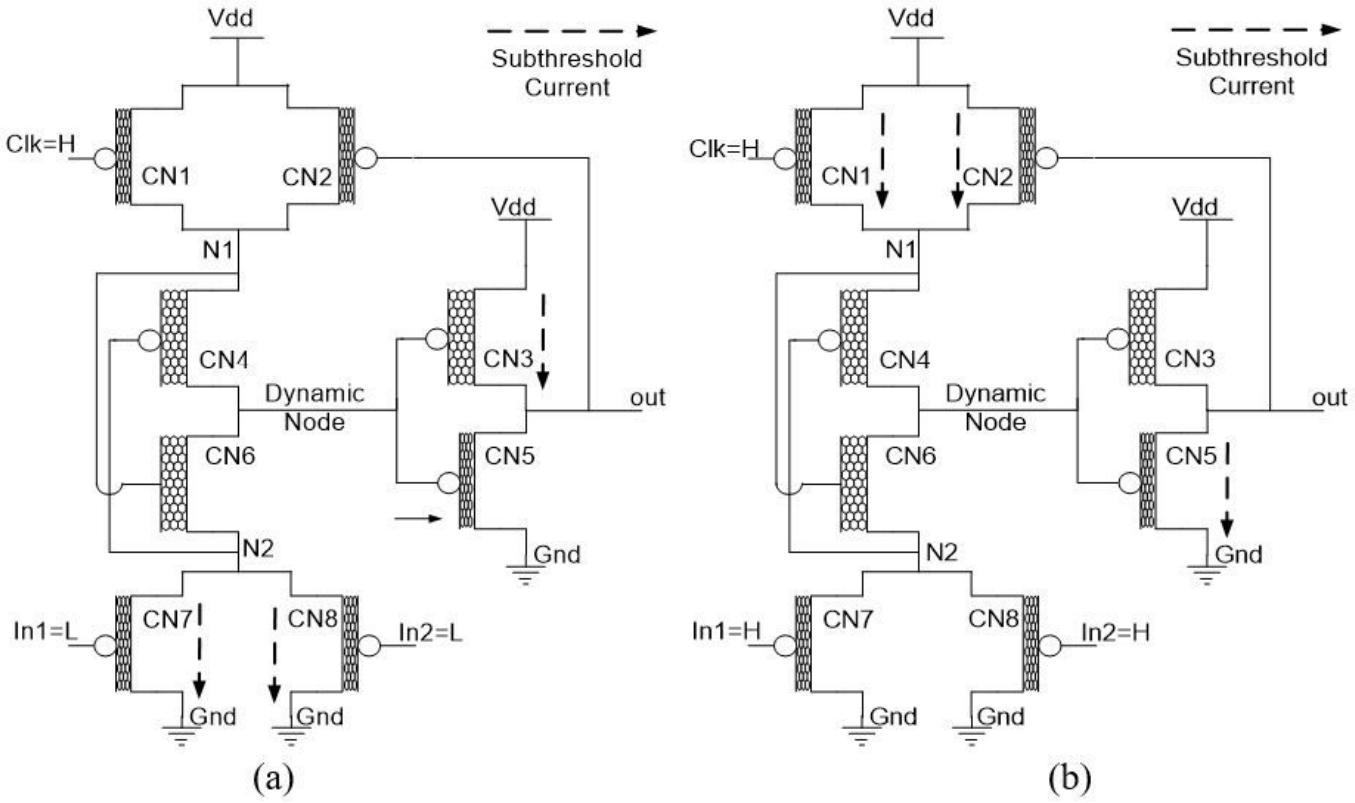


Figure 7

Flow of subthreshold current in proposed dual chiral LECTOR based CNTFET domino OR gate (a) low inputs (b) high inputs

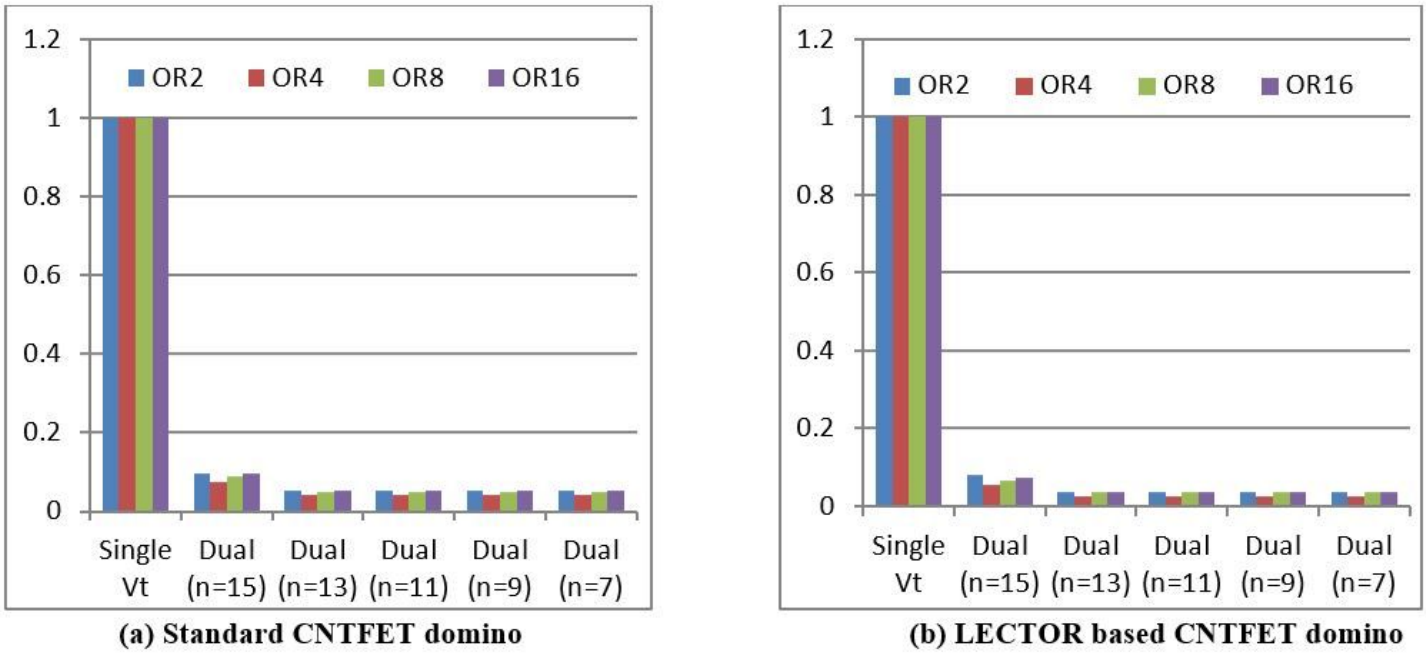
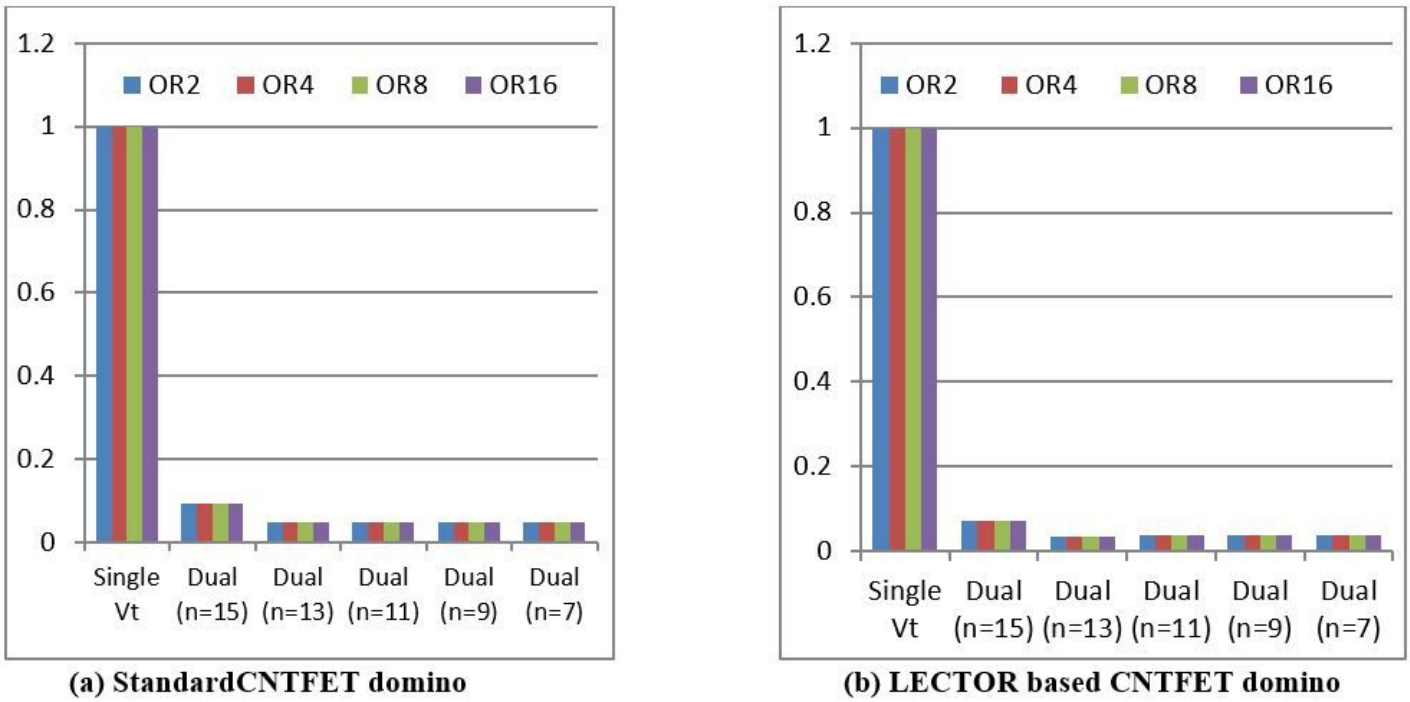


Figure 8

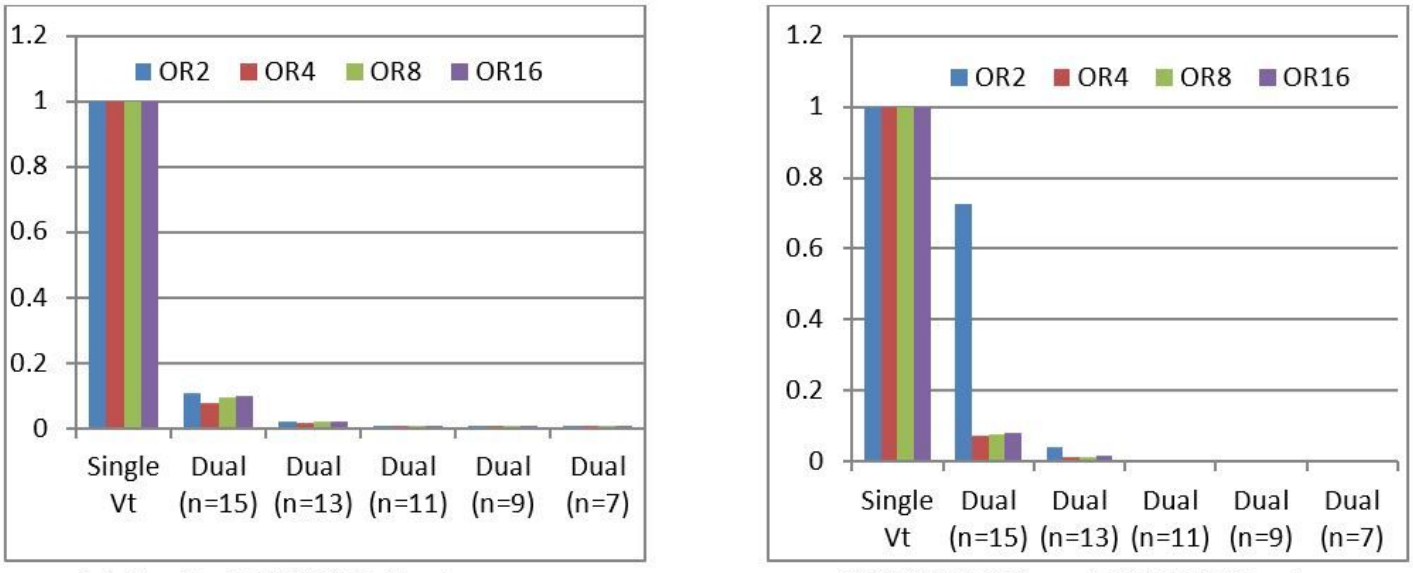
At low temperature, subthreshold leakage power saving in proposed dual chiral domino OR gates for 2, 4, 8 & 16-input. Subthreshold leakage power is normalized to the leakage power of single Vt standard and LECTOR footerless domino OR gates for low inputs (a) Standard CNTFET domino (b) LECTOR based CNTFET domino



(a) StandardCNTFET domino (b) LECTOR based CNTFET domino

Figure 9

At low temperature, subthreshold leakage power saving in proposed dual chiral domino OR gates for 2, 4, 8 & 16-input. Subthreshold leakage power is normalized to the leakage power of single Vt standard and LECTOR footerless domino OR gates for high inputs (a) Standard CNTFET domino (b) LECTOR based CNTFET domino



(a) Standard CNTFET domino (b) LECTOR based CNTFET domino

Figure 10

At high temperature, subthreshold leakage power saving in proposed dual chiral domino OR gates for 2, 4, 8 & 16-input. Subthreshold leakage power is normalized to the leakage power of single Vt standard and LECTOR footerless domino OR gates for low inputs (a) Standard CNTFET domino (b) LECTOR based CNTFET domino

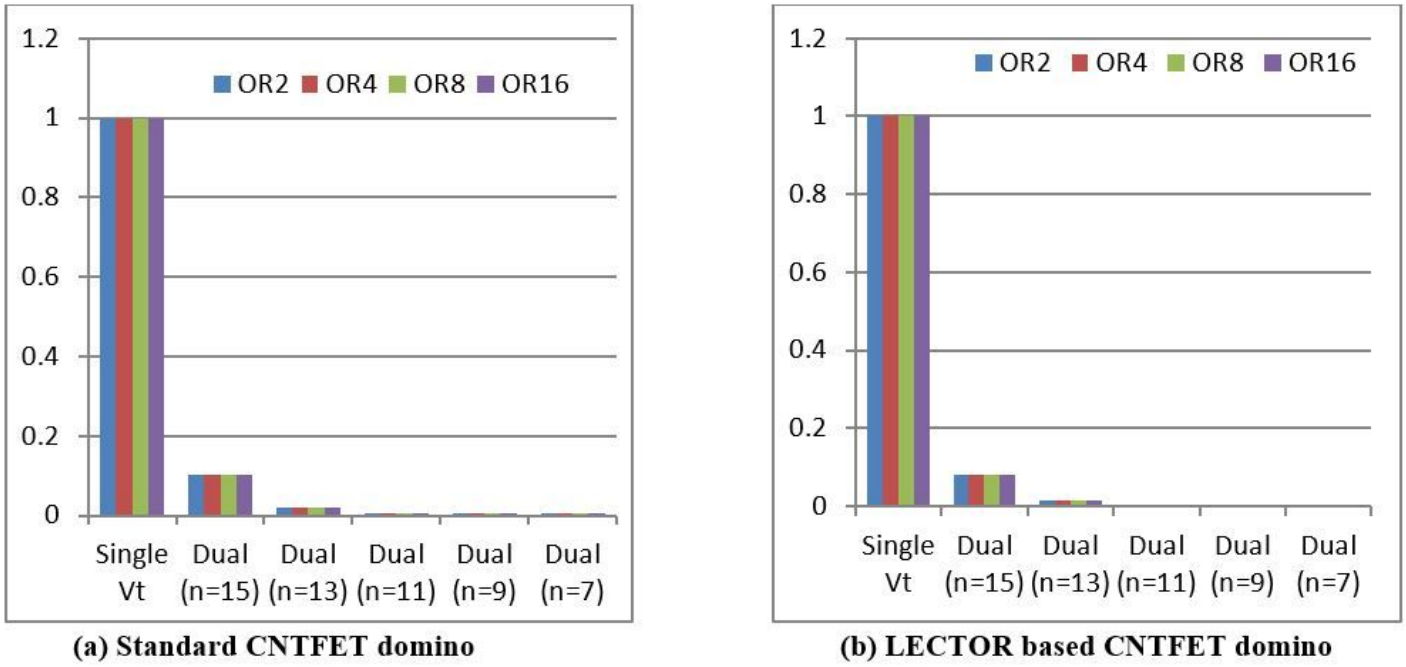


Figure 11

At high temperature, subthreshold leakage power saving in proposed dual chiral domino OR gates for 2, 4, 8 & 16-input. Subthreshold leakage power is normalized to the leakage power of single Vt standard and LECTOR footerless domino OR gates for high inputs (a) Standard CNTFET domino (b) LECTOR based CNTFET domino