Investigation of Common Source Amplifier Circuit Application Using Gate Stack Based Gate-all-around Charge Plasma Nanowire FET

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Research Article

Keywords: Gate-All-Around, Nanowire, Charge plasma, Gate stack, Common source amplifier, FET

Posted Date: March 15th, 2022

DOI: https://doi.org/10.21203/rs.3.rs-1448544/v1

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Investigation of common source amplifier circuit application using gate stack based gate-all-around charge plasma nanowire FET

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Abstract

The reported work demonstrates the application of common source amplifier circuit using gate-all-around gate stacked charge plasma nanowire field effect transistor (GAA GS CP NW FET). Primarily, the impact of the gate stacking (GS) technique upon the Gate-All-Around Charge Plasma Nanowire Field Effect Transistor (GAA CP NW FET) structure is explored. In which GAA GS CP NW FET structure resulted in excellent electrostatic control over the channel by incorporating the advantages of GAA structures. The transfer characteristics have been enhanced with the gate stacking (SiO₂ + high k) technique when employed at the dielectric region of the structure. The charge plasma concept which is applied in the proposed device helped in reducing the threshold voltage fluctuations. A contrast is drawn between GAA CP NW FET and GAA GS CP NW FET structures in terms of analog and RF analysis. Linearity parametric analysis were made to examine the distortion less digital communication and a comparison is made between the structures. The proposed structure is then utilized for designing a common source amplifier circuit and contrasted with the GAA CP NW FET structure. With the applied gate stacking technique, the proposed structure resulted in improved ON-current, reduced OFF-current, enhanced current ratio. The CS amplifier circuit application resulted in improved V_{out} and gain attributes with the proposed GAA GS CP NW FET structure when compared with Metal Oxide Semiconductor FET (MOSFET), Tunnel FET (TFET) and GAA CP NW FET structure proving its capability for forthcoming nanoscale circuit applications.

Index terms: Gate-All-Around, Nanowire, Charge plasma, Gate stack, Common source amplifier, FET.

I. Introduction

In recent times, microelectronics has seen an incredible growth in which the transistor’s involvement is considered crucial [1]. Semiconductor technology with silicon-based devices produced exquisite progresses over the past decade [2], the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) paved a way for research in terms of device miniaturization which in turn gave decent improvements with performance and less cost in fabrication [3]. Moore’s law holds true for only some specific scaling but next-generation devices, for the best performance and less power consumption, research is on process for further downscaling [4-5]. Though, Short channel effects (SCEs) and process limitations were created in the device with the downscaling of the transistor size [6-7]. Hence, a necessity for novel methods on devices and structures to meet the objectives in stability and performance have been increased. To overcome such disadvantages with device miniaturization and SCEs the use of new materials [8-9], innovative novel operated designs [10-11] were explored by researchers and scientists. Though new materials which were introduced hold good improvements, silicon has persisted as an appropriate material with its further advantages in terms of the production process, cost, and fabrication’s perspective [12].
To surpass the SCEs, devices like Tunnel-FET (TFETs) [13-14], Impact Ionization MOS (IMOS) [15] and novel structured designs such as three-dimensional (3D) structures [16], multi-gate designs such as tri-gate structures [17-18] for improved controllability over gate and gate-all-around (GAA) structure designs with high packaging density and excellent gate controllability over the channel were considered as the best replacements [19]. With the applications include clinical purpose biosensors [20], industrial based pressure sensors [21] etc. Among the mentioned alternatives with advantages like transport properties, electrostatic control, and reduced SCEs, the GAA structures turn out to be a promising design alternative [22]. At sub-10nm technology nodes, Gate-All-Around Nanowire Field Effect Transistors (GAA NW FETs) exhibited exceptional electrostatic properties when compared with the FinFETs [23]. For RF and digital process applications, Nanowire FETs (NWFETs) emerged as highly desirable structures [24]. The promising performance of the device with improved ON-current ($I_{ON}$), large current ratios ($I_{ON}/I_{OFF}$), and subthreshold swings were reported and thus proved itself to be the most excellent structure design for the downscaling of semiconductor nanoscale devices [25]. With the broad research on GAA NW FET device structures, a disadvantage like high series resistance which occurred due to the abrupt formation of the junction has been addressed by the Junction-Less NW FETs (JL NW FETs) [26]. But JL NW FETs suffered from lower drive current due to reduced carrier mobility and heavy doping concentration at the channel area because of uniform doping over the channel, source and drain regions [27]. To overcome the heavy channel doping concentration issue, charge plasma technique has been introduced to the GAA NW FET structures [28]. The need for doping is excluded as the n-type and p-type of the device will be brought to the intrinsic region of the device. With the help of appropriate work functions, source and drain regions can be developed making it a GAA Charge Plasma NW FETs (GAA CP NW FETs) device structure. Due to the problem with limit in scaling at gate, the dielectric region which is less than 2nm the difference between static power consumption and gate leakage current has been raised. A layer of high-k dielectric over the SiO$_2$ oxide region is introduced to overcome the scaling issue which gave less leakage current, advanced drive current and increased gate capacitances [29]. This concept of adding a thin layer of high k over the oxide region is described as gate stacking. Thus, making it a GAA Gate Stacking CP NW FETs (GAA GS CP NW FETs).

In this treatise, a fair comparison is drawn out of the proposed GAA GS CP NW FETs device structure with GAA CP NW FET [30] device structure for Analog and RF analysis to observe the switching operation of the devices, linearity analysis to study the distortion less digital communication from the transmitter to receiver and to explore both structures in designing a common source amplifier circuit application. The rest of the paper is arranged as follows: Section II explains the structure of GAA CP NW FET [30], and proposed structure of the GAA GS CP NW FET device and the parameters used. Analog and RF performance analysis, Linearity analysis and implementation of the common source amplifier circuit of GAA GS CP NW FET device structure have been examined and compared with GAA CP NW FET device structure in section III results and discussion. Finally, conclusions are drawn in section IV.

## II. The proposed device schematic and design specifications

The proposed device incorporates the gate stacking technique. Fig. 1 shows the 3-Dimensional structure view of (a) GAA CP NW FET [30], (b) shows the internal structure view of GAA CP NW FET and (c) shows the internal view of proposed structure of GAA GS CP NW FET. The structure’s cross-sectional view is shown in Fig 2 in which (a) represents the structure of GAA CP NW FET and (b) represents the proposed structure of GAA GS CP NW FET. The parameters that are used for designing GAA CP NW FET [30] and proposed GAA GS CP NW FET structures are as follows: p-n-p configuration structure with source and drain on p-side and n-type channel region. Length of the source and length of the drain as 10nm each and gate length as 20nm for both the structures. The oxide thickness is taken as 1nm with SiO$_2$ as gate oxide for GAA CP NW FET and the oxide thickness for GAA GS CP NW FET structure is taken as 0.5nm for SiO$_2$ and 0.5nm for HfO$_2$ (high k material) for implementing gate stacking technique upon the GAA CP NW FET structure. The spacer length ($L_{SP}$) for both the structures is taken as 10nm. Uniform doping for the n-type channel is given as $1 \times 10^{15}$ cm$^{-3}$ for both the structures with a radius of 5nm. The remaining parameters used in simulating the structures are mentioned in Table 1. Since both the structures i.e., GAA CP NW FET and GAA GS CP NW FET are of charge plasma structures hence, a common work function is used to form source and drain regions which is 3.9eV – Hafnium (Hf). Having the advantage of charge plasma, doping has been eliminated from the simulation of both structures. Silvaco ATLAS [31] simulator is utilized for simulations of both the structures and to attain the data that is required. The models used for
simulation are Auger recombination model, Bohm quantum model, High-field reduction model, Fermi-Dirac model, and Concentration-dependent mobility model.

III. Results and discussion

This section contains the simulated results of GAA CP NW FET and GAA GS CP NW FET structures. A detailed analysis is discussed on comparing both the structures. The characteristics of drain current with respect to gate voltage in both linear and log scale of GAA CP NW FET and GAA GS CP NW FET structures with \( V_{DS} = 1V \) and \( V_{GS} \) from 0V to 1V is shown in Fig. 3. The resistance in between the source and drain is usually determined by the drain current. At high voltages, the resistance of the channel is determined by the resistance of source and drain terminals. From Fig. 3 the drain current of the GAA GS CP NW FET structure is higher when compared with the GAA CP NW FET structure due to the addition of high-k material which is the gate stacking technique applied to the proposed structure. When compared for the ON-state current (I\(_{ON}\)), GAA GS CP NW FET structure gave 30.6 (µA/µm) whereas GAA CP NW FET gave 28.8 (µA/µm). Concerning the OFF-state current (I\(_{OFF}\)) GAA GS CP NW FET gave 4.55×10\(^{-7}\) (µA/µm) and GAA CP NW FET gave 5.66×10\(^{-7}\) (µA/µm) proves that the proposed structure i.e., GAA GS CP NW FET gave the better outcomes. The electric property which determines

<table>
<thead>
<tr>
<th>Parameters</th>
<th>GAA CP NW FET [30]</th>
<th>GAA GS CP NW FET</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Gate work function</strong></td>
<td>4.63 eV Niobium</td>
<td>4.63 eV Niobium</td>
</tr>
<tr>
<td><strong>Source work function</strong></td>
<td>3.9 eV Hafnium</td>
<td>3.9 eV Hafnium</td>
</tr>
<tr>
<td><strong>Drain work function</strong></td>
<td>3.9 eV Hafnium</td>
<td>3.9 eV Hafnium</td>
</tr>
<tr>
<td><strong>Gate Length</strong></td>
<td>20nm</td>
<td>20nm</td>
</tr>
<tr>
<td><strong>Length of Source/Drain</strong></td>
<td>10nm</td>
<td>10nm</td>
</tr>
<tr>
<td><strong>Radius</strong></td>
<td>5nm</td>
<td>5nm</td>
</tr>
<tr>
<td><strong>Gate oxide material</strong></td>
<td>SiO(_2)</td>
<td>SiO(_2)</td>
</tr>
<tr>
<td><strong>Effective oxide thickness (EOT)</strong></td>
<td>1nm</td>
<td>0.5nm</td>
</tr>
</tbody>
</table>

![Fig. 1. 3-D structures view of (a) GAA CP NW FET [30] (b) Internal structure of GAA CP NW FET (c) Internal structure of GAA GS CP NW FET.](image1)

![Fig. 2. 2-D cross-sectional structures view of (a) GAA CP NW FET [30] (b) GAA GS CP NW FET.](image2)
the efficiency of the device which is associated with the change in the differential output current to the input voltage at the constant $V_{DS}$ (voltage from drain to source) is termed as transconductance. Fig. 4(a) shows the transconductance ($g_m$) with respect to gate voltage for GAA CP NW FET and GAA GS CP NW FET structures. With the improved drive current and the high carrier mobility the proposed structure GAA GS CP NW FET shows an increased transconductance when compared with the GAA CP NW FET structure. With provided high transconductance, the proposed structure plays a prominent in analog applications. The power dissipation and the switching behaviour is determined by the parasitic capacitances which are stored inside the channel region and for that determining the total gate capacitance is an important factor. Fig. 4(b) shows the total gate capacitance ($C_{GG}$) characteristics with respect to the gate voltage of GAA CP NW FET and GAA GS CP NW FET structures. It is evident from Fig. 4(b) is that the proposed structure GAA GS CP NW FET due to the addition to dielectric (high-k material HfO$_2$) shows a better result with respect to total gate capacitance when compared with the GAA CP NW FET structure.

Fig. 3. $I_D$-$V_{GS}$ in log and linear scale of GAA CP NW FET and GAA GS CP NW FET.

Fig. 4. Analog parametric results of GAA CP NW FET and GAA GS CP NW FET structures with (a) Transconductiontance ($g_m$), (b) Total gate capacitance ($C_{GG}$), (c) Unity gain frequency and (d) Gain product bandwidth (GPB).
For determining RF performance analysis, unity gain frequency or cut-off frequency \(F_T\) plays an important role. Fig. 4(c) shows the characteristics of unity gain frequency with respect to the gate voltage of GAA CP NW FET and GAA GS CP NW FET structures. For any device or structure, to obtain higher \(F_T\) there should be a higher \(g_m\). As from Fig. 4(a), the proposed device has higher transconductance and the factors the influence \(F_T\) are also high. Hence the proposed GAA GS CP NW FET structure shows higher cut-off or unity gain frequency when compared with the GAA CP NW FET structure proving that the proposed structure is best concerning RF or analog analysis. Gain product bandwidth (GPB) is one of the prominent results evaluated for RF analysis. The gain product bandwidth can be obtained by Eq. 1. Which is the product of gain with the frequency that is measured for a particular point. The gain product bandwidth of GAA CP NW FET and GAA GS CP NW FET with respect to gate voltage is shown in Fig 4(d).

\[
\text{Gain Product Bandwidth (GPB)} = \frac{g_m}{20\pi C_{GD}} \quad (1)
\]

From Fig. 4(d) it is evident that the proposed GAA GS CP NW FET structure shows higher GPB than the GAA CP NW FET structure. GPB mainly depends upon the transconductance and the capacitance from the gate to the drain area. If the transconductance gives a higher result so does the GPB. The drive current as well as the high carrier mobility in the proposed structure is the reason behind its higher GPB when compared with the GAA CP NW FET structure. The comparison with respect to the on-state, off-state, current ratio, threshold voltage, subthreshold and average SS of GAA CP NW FET and GAA GS CP NW FET are shown in Table 2. The on-state current is higher with the proposed GAA GS CP NW FET, and a lower off-state current has been recorded when compared with the GAA CP NW FET structure. With the remaining aspects like current ratio, \(V_T\), Sub \(V_T\) and Avg. SS, the proposed device GAA GS CP NW FET structure proved to be the best when compared with the GAA CP NW FET structure.

Table 2. Comparison of current (off state, on state & their ratio), threshold voltage, sub \(V_T\) & AvSS with both the structures

<table>
<thead>
<tr>
<th></th>
<th>GAA CP NW FET</th>
<th>GAA GS CP NW FET</th>
</tr>
</thead>
<tbody>
<tr>
<td>ON – State (I_{ON}) (µA/µm)</td>
<td>28.897</td>
<td>30.6583</td>
</tr>
<tr>
<td>OFF – State (I_{OFF}) (A/µm)</td>
<td>5.6631×10^-7</td>
<td>4.55283×10^-7</td>
</tr>
<tr>
<td>Current Ratio (I_{ON}/I_{OFF})</td>
<td>5.1026×10^7</td>
<td>6.739×10^7</td>
</tr>
<tr>
<td>Threshold Voltage (V_T) (V)</td>
<td>0.197185</td>
<td>0.201346</td>
</tr>
<tr>
<td>Sub-threshold (Sub V_T) (V/dec)</td>
<td>0.0606031</td>
<td>0.0601596</td>
</tr>
<tr>
<td>Avg. SS (V/dec)</td>
<td>0.0299312</td>
<td>0.0303275</td>
</tr>
</tbody>
</table>

In this present era of digital communication, distortion-free communication when connected to a system should be as linear as possible. For the linearity analysis of the proposed structure GAA GS CP NW FET when compared with GAA CP NW FET structure is determined by observing some important parameters which include \(g_{m2}\), \(g_{m3}\), VIP3, IIP3, IMD3 and 1-dB compression point.

\(g_{m2}\) is the second-order derivative of the drain current. The second-order derivative of drain current i.e., \(g_{m2}\) with respect to gate voltage for GAA CP NW FET and GAA GS CP NW FET structures is shown in Fig. 5(a) and for the proposed structure GAA GS CP NW FET the second-order derivative can be seen higher when compared with the GAA CP NW FET structure. The third-order derivative of drain current is \(g_{m3}\). The variation in \(g_{m3}\) with respect to the gate voltage of GAA CP NW FET and GAA GS CP NW FET structures is shown in Fig. 5(b). It is evident from Fig. 5(b) that the proposed GAA GS CP NW FET structure is found to have a higher value of \(g_{m3}\) when compared with the GAA CP NW FET structure. The third order voltage intercept point (VIP3) with respect to the gate voltage of GAA CP NW FET and GAA GS CP NW FET is shown in Fig. 5(c). The first voltage harmonics are the same for both the structures and the peak of GAA GS CP NW FET is higher in terms of VIP3 when compared with the GAA CP NW FET structure. The mathematical expression for VIP3 is given in Eq. 2.

\[
VIP3 = \sqrt{\frac{24}{g_{m3}}} \left(\frac{g_{m2}}{g_{m3}}\right) \quad (2)
\]

A linear parameter that can present the suitability of the structure for distortion less applications is IIP3. The variation in IIP3 with respect to gate voltage for GAA CP NW FET and GAA GS CP NW FET structures is shown in Fig. 5(d). The mathematical expression for IIP3 is given in Eq. 3.
\[ IIP3 = \frac{2}{3} \left( \frac{g_{m2}}{g_{m3}(R_s)} \right) \]  

(3)

Where \( R_s = 50 \Omega \)

The equity between the first and third modulation harmonic power is defined by IMD3. Fig. 5(e) shows the IMD3 variation with respect to the gate voltage of GAA CP NW FET and GAA GS CP NW FET structures. It is observed that the peak of GAA GS CP NW FET is higher when compared with the GAA CP NW FET structure proving its capability for wireless communication systems. The mathematical expression for IMD3 is given in Eq. 4.

\[ IMD3 = \left[ \frac{9}{3} (VIP^3) g_{m3} \right] R_s \]  

(4)

Where \( R_s = 50 \Omega \)

Fig. 5(f) shows the 1-dB compression point of GAA CP NW FET and GAA GS CP NW FET structures. The proposed structure GAA GS CP NW FET has the maximum value of 0.2dB at VGS = 0.65V when compared to the GAA CP NW FET structure. The expression of 1-dB compression point is given at Eq. 5.

\[ 1 - dB \text{ compression point} = 0.22 \sqrt{\frac{g_{m2}}{g_{m3}}} \]  

(5)

Fig. 5. Linearity analysis of GAA CP NW FET and GAA GS CP NW FET structures with (a) variation in \( g_{m2} \), (b) variation in \( g_{m3} \), (c) variation in VIP3, (d) variation in IIP3, (e) variation in IMD3 and (f) 1-dB compression point.
The potential of the proposed device GAA GS CP NW FET is verified by the analog integrated circuit design with common source amplifier (CS amplifier). Fig. 7 demonstrates the n-type CS amplifier circuit designed using GAA CP NW FET and GAA GS CP NW FET structures. Look up table (LUT) based Verilog-A model is assisting various research groups in carrying out the SPICE simulations [32]. The LUT approach for designing a circuit model for SPICE implementation is fairly practiced by the researchers as its accurate in implementing for almost all the devices, though the valid compact models are yet to be designed. The transfer of capacitance characteristics of NW-FET structures is utilized by the LUT based Verilog-A model. The information that is essential for designing the LUT based Verilog-A is given in Fig. 6.

<table>
<thead>
<tr>
<th>$I_{DS}$ Look Up Table</th>
<th>$C_{GS}$ Look Up Table</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>$V_{GS}$</td>
</tr>
<tr>
<td>...</td>
<td>...</td>
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<td>...</td>
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</tbody>
</table>

Fig. 6. LUT format for designing Verilog-A model

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC supply voltage</td>
<td>1v</td>
</tr>
<tr>
<td>Drain capacitor ($C_D$)</td>
<td>1p</td>
</tr>
<tr>
<td>Gate capacitor ($C_G$)</td>
<td>2u</td>
</tr>
<tr>
<td>Source capacitor ($C_S$)</td>
<td>2u</td>
</tr>
<tr>
<td>$R_1$</td>
<td>5k</td>
</tr>
<tr>
<td>$R_2$</td>
<td>5k</td>
</tr>
<tr>
<td>$R_S$</td>
<td>10k</td>
</tr>
<tr>
<td>$R_L$</td>
<td>1900k</td>
</tr>
<tr>
<td>$R_D$</td>
<td>140k</td>
</tr>
</tbody>
</table>

Table 3. Parameters used in netlist for n-type common source amplifier circuit implementation.

Fig. 7. N-type common source amplifier circuit design utilized and implemented with GAA CP NW FET and GAA GS CP NW FET structures.
The total number of tables that are extracted from the simulation of structures are three for each structure and they are IdVg.tbl, Cgs.tbl and Cgd.tbl. .tbl is the extension that should be saved so that the same format will be called into the Verilog code. Later the Verilog code with extension .va is then called into a netlist.sp. netlist is written with .sp extension for calling out into SMARTSPICE simulator. SMARTSPICE is used for the analysis on implementing n-type common source amplifier circuit. The circuit diagram of the n-type common source amplifier circuit designed using GAA CP NW FET and GAA GS CP NW FET is shown in Fig. 7. \( V_{in} \) and \( R_{in} \) are the input voltage and input resistance respectively with small magnitude are given for device amplification. \( C_G, C_D, C_S \) are capacitors at the gate, drain and source respectively are connected to the circuit to the dc components from the amplified output signal. \( R_1 \) and \( R_2 \) are the resistances. \( R_D \) and \( R_S \) are the resistors at drain and source respectively. \( R_L \) is the load resistor. The product of bandwidth and gain are constant at all times. Which means if the gain is to be improved, a sacrifice must be made with bandwidth vice versa in the case of an amplifier. The gain of any amplifier circuit depends upon the transconductance and the equivalent output resistance of the structure which is expressed in Eq. 6.

\[
A_V = g_m R_{eq}
\]  

(6)

The parameters that are used in creating a netlist for an n-type common source amplifier is shown in Table 3. The netlist which is to be called into SMARTSPICE is saved with the .sp extension.

Fig. 8. Transient analysis response of n-type common source amplifier for GAA CP NW FET and GAA GS CP NW FET structures.

Fig. 9. Variation in \( R_L \) (a) output voltage characteristics, (b) gain in dB at constant \( R_D = 140k \) and variation in \( R_D \) (c) output voltage characteristics (d) gain in dB at constant \( R_L = 1900k \) of n-type common source amplifier for GAA CP NW FET and GAA GS CP NW FET structures.
The transient analysis is made with suitable bias voltages, resistor and capacitor values given in Table 3. The netlist values are kept constant as mentioned in Table 3 for both the structures GAA CP NW FET and GAA GS CP NW FET. Transient analysis of n-type common source amplifier for GAA CP NW FET and GAA GS CP NW FET is shown in Fig. 8. The good amplification is achieved at $R_D = 140k$ and $R_L = 1900k$. At $R_D = 140k$ and $R_L = 1900k$, GAA GS CP NW FET structure gave a good amplification with 180-degree phase shift from input and is higher when compared with the GAA CP NW FET structure. Thus, proving its ability in designing amplifiers as in integrated circuits this is one of the prominent building blocks. As an extensive analysis the variation in $R_L$ by keeping $R_D$ at constant 140k and variation in $R_D$ by keeping $R_L$ at constant 1900k in n-type common source amplifier with respect to GAA CP NW FET and proposed GAA GS CP NW FET structures are shown in Fig. 9. The obtained $V_{out}$ and gain in dB for both the variation in $R_L$ and $R_D$ are plotted in Fig. 9(a), (b), (c) and (d) respectively for both the structures. With all the analysis carried out considering in variation of $R_L$ and $R_D$ values the proposed structure GAA GS CP NW FET gave better outcomes when compared with the GAA CP NW FET structure.

Table 4. CS amplifier performance comparison with references.

<table>
<thead>
<tr>
<th>CS Amplifier application</th>
<th>$R_L$ (kΩ)</th>
<th>$V_{IN}$ (V)</th>
<th>$V_{OUT}$ (V)</th>
<th>Gain (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOSFET [33]</td>
<td>1000</td>
<td>0.05</td>
<td>0.079</td>
<td>3.9</td>
</tr>
<tr>
<td>HD TMG TFET [33]</td>
<td>1000</td>
<td>0.05</td>
<td>0.15</td>
<td>9.5</td>
</tr>
<tr>
<td>GAA CP NW FET</td>
<td>1000</td>
<td>0.05</td>
<td>0.25</td>
<td>13.9</td>
</tr>
<tr>
<td>GAA GS CP NW FET</td>
<td>1000</td>
<td>0.05</td>
<td>0.29</td>
<td>15.2</td>
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</table>

The simulation results carried out on GAA CP NW FET and GAA GS CP NW FET showed better results in terms of gain when compared with MOSFET [33] and Hetero Dielectric Tri Material Gate Tunnel FET (HD TMG TFET) based CS amplifier [33] is shown in Fig. 10. The performance parameters comparison with MOSFET and HD TMG TFET based CS amplifier are shown in Table 4. Here for comparison purpose the mentioned value of $R_L$ is taken and simulated for GAA CP NW FET and GAA GS CP NW FET structures. GAA CP NW FET based CS amplifier results in gain 13.9dB and GAA GS CP NW FET based CS amplifier results in gain 15.2dB proving GAA GS CP NW FET good compatibility in designing CS amplifier circuits.

IV. Conclusion

A detailed investigation is carried out for the proposed GAA GS CP NW FET structure from analog and RF analysis to linearity analysis to the implementation of the n-type common source amplifier circuit. The proposed structure demonstrates profoundly good results when the comparison is drawn with the GAA CP NW FET structure in all the analysis carried out. GAA GS CP NW FET structure has shown exceptional outcomes in terms
of high on-state current, low off-state current, steep sub-threshold which are all chosen features for usage in low power and high performances VLSI circuits. The proposed structure GAA GS CP NW FET showed good results not only in analog and RF but also in linearity analysis proving its capability for distortion less communication systems. The circuit implementation that is carried out for the implementation of n-type common source amplifier has also shown better results with good amplification when compared with GAA CP NW FET providing valuable contribution with the usage in low power circuits.

**DECLARATIONS SECTION**

**Ethics approval and consent to participate:** Not Applicable.

**Consent for publication:** Not Applicable.

**Availability of data and materials:** Not Applicable.

**Competing interests:** The authors have no relevant financial or non-financial interests to disclose.

**Funding:** The authors declare that no funds, grants, or other support received during the preparation of this manuscript.

**Author’s contributions**

**Leo Raj Solay:** Simulation, Computation, TCAD software and Writing – Original draft preparation

**Pradeep Kumar:** Conceptualization, Supervision, and Validation.

**S. Intekhab Amin:** Computation, TCAD software, Revision, Supervision, and Validation.

**Sunny Anand:** Conceptualization, computation, revision, Supervision, and Validation.

**Acknowledgements:** Not Applicable.

**COMPLIANCE WITH ETHICAL STANDARDS SECTION**

**Disclosure of potential conflicts of interest:** No conflicts of interest to report.

**Research involving human participants and/or animals:** Not Applicable.

**Informed consent:** Not Applicable.

**References**


