RESEARCH

A robust 4-channel micro-power low-noise neural recording amplifier for hippocampal cognitive prosthesis

Ming Ni, Yan Han*, Jian Lei and Hakbong Kim

*Correspondence: hany@zju.edu.cn
the School of Micro-nano Electronics, Zhejiang University, Hangzhou, China
Full list of author information is available at the end of the article

Abstract

Background: Recording of electrical activity of neurons is indispensable for decoding the information in the brain. The amplitude of signals recorded by electrodes is small, and it must be amplified to the level that can be digitalized by the analog-to-digital convert (ADC). A micro-power low-noise neural recording amplifier is indispensable for implant hippocampal cognitive prosthesis. When the process turns into deep submicron, the gate leakage current of the metal oxide semiconductor (MOS) transistor becomes larger and mismatch between devices becomes worsen. It is necessary to keep the neural amplifier robust in all process corners.

Methods: The proposed circuit is a two-stage amplifier which can achieve a good trade-off between power consumption and noise. Four second-stage amplifiers share a common reference amplifier to reduce area and power consumption. A pseudo-resistor with high resistance is utilized to realize a very-low frequency high-pass corner without external components. In order to minimize process variation, a bulk-compensated (BC) technique is adopted to maintain adequate tolerance in all corner case.

Results: The 4-channel neural amplifier is designed and fabricated in a 40 nm standard complementary metal oxide semiconductor (CMOS) process. It achieves a mid-band gain of 54 dB, a bandwidth of 70 Hz to 7.7 kHz, a total input-referred noise of 3.2 μV_{rms}, and a Noise Efficiency Factor (NEF) of 3.3 while consuming 4.68 μW from the 1.1 V supply. The core area of one channel is only 0.032 mm^2.

Conclusion: A 4-channel integrated neural recording amplifier chip with bias-compensated circuits is presented in this paper. Extensive simulations insure that the design is "centere". The chip layout is verified using design rules check (DRC) and layout versus schematic (LVS) design check with the help of verification tools. Test results shows that it is less sensitive to process variation and consumes less power compared with amplifier without bulk-compensated circuit. This makes the design robust and uniquely appropriate for low-power implant application.

Keywords: Implant prosthesis; Neural amplifier; Low power; Low noise; Bulk-compensated circuit

Background

With the development of information science and technology, there are more diverse research and treatment methods for modern medicine. Although we can now cure many diseases, and even edit genes, there still is a long way to understand the brain.

As the most important and complex part of the human body, the brain contains more than 100 billion neurons and more glial cells. Each neuron may form up to 10,000 synaptic connections with other neurons, which constitutes more than 1,000 trillion synaptic connections [1]. Such a sophisticated structure has brought great challenges to the interpretation of the pathogenesis of brain diseases.

The hippocampus is a part of the limbic system of the brain, located below the cerebral cortex, and is mainly responsible for spatial positioning and the formation of new long-term memories [2]. Damage to the hippocampus can lead to the loss of the ability to convert short-term memory into long-term memory, causing cognitive dysfunction and disorientation. Hippocampal system damage can result from cerebral hypoxia, encephalitis or epilepsy. There is no known treatment for these debilitating cognitive deficits. According to the World Alzheimer Report 2020, there are currently estimated to be over 50 million people worldwide living with dementia. The number of people affected is set to rise to 152 million by 2050. A new case of dementia arises somewhere in the world every 3 seconds [3]. Since 1998, researchers have developed hundreds of drugs, but only 4 drugs have undergone clinical trials so far, and all ended in failure [4].

The dilemma of drug therapy motivates researchers to explore new treatments. With the development of technology, prosthesis and brain machine interface (BMI) have been applied in the treatment of various diseases [5]. Berger et al. outlined a plan for addressing this issue through the replacement of damaged tissue with microelectronics that mimics the functions of the original biological circuitry [6]. The microelectronic systems do not just electrically stimulate cells to generally heighten or lower their average firing rates. Instead, the prosthesis incorporates mathematical models and replicates the fine-tuned, spatio-temporal coding of information by the hippocampal memory system.

Figure 1 shows the processing path and the major elements of the prosthetic device. The analog front-end, consisting of 16 micro-power low-noise amplifiers (LNA), 16 high-pass filters and 16 ADC. The digitized signals then are classified by 16 spike sorters [7] into spike-event channels, where events are represented by a single bit. Outputs are computed by a single multi-input multi-output (MIMO) model processor [8], which delivers up to 8 channels of output to a neural stimulator (NS) [9, 10]. LNA, as the first module in the whole system, plays an extremely important role.

Results

The proposed 4-channel neural amplifier is fabricated in a 40 nm standard CMOS process. The layout of the neural amplifier is shown in Figure 2(a), and the dies photograph is shown in the left of Figure 2(b). A neural amplifier without BC circuit is presented for comparison, and its die photograph is shown in the right of Figure 2(b). The only difference between the dies of the two neural amplifiers is whether a BC circuit exists. Both two die area occupies 0.5 mm^2, in which the core occupies 0.032 mm^2. That means each channel only occupies 0.008 mm^2. Performance summary and comparison are shown in Table 1. Here, “With BC” means the neural amplifier with bulk-compensated circuit, and “Without BC” means the neural amplifier without bulk-compensated circuit. The measurement results show that the high-pass cutoff frequency of the proposed neural amplifier is 70 Hz, and

the low-pass cutoff frequency is 7.7 kHz. The right amplifier without BC circuit consumes 10.5 μA at 1.1 V power supply, and the input-referred noise is 3.6 μV_{rms} when integrated in interested bandwidth, which leads to an NEF of 5.9. While the left amplifier with BC circuit consumes 4.25 μA at 1.1 V power supply, and the input-referred noise is 3.2 μV_{rms} when integrated in interested bandwidth, leading to a NEF of 3.3. The neural amplifier with BC has lower power and better NEF than the amplifier without BC. With a BC circuit, the neural amplifier achieves lower power, lower noise, and robust in a deep submicron process.

The features discussed above are the best results in the measurements. We measured power consumption in 15 dies and compared the neural amplifier with and without BC. The total current of the dies is distributed among a certain range, as shown in Figure 3. The curve above shows current consumptions of amplifiers without BC circuit in 15 dies; while the curve below shows current consumptions of amplifiers with BC circuit in 15 dies. Power consumption reduced by approximately 60% using the BC circuit. Meanwhile, the current difference among 15 dies becomes small using BC circuit. Therefore, we can obtain a highly stable total current and low power consumption using a BC circuit, which is important for an analog design in deep submicron process.

Discussion

Different researchers have focused on different features in their design. For example, some studies have focused on the low power of the amplifier [11, 12], some have pursued low noise [13, 14, 15], while others have paid more attention to the NEF [16, 17, 18, 19], high input impedance [20, 21], little distortion [22, 23, 24] and small area [25, 26]. A tradeoff exists between power, noise and area and balancing these performances in design is important. When the process turns into deep submicron, the performance of the MOS transistor become worse. For example, the gate leakage current of the MOS transistor becomes larger, but the threshold voltage becomes slightly lesser, and the mismatch between devices could possibly worsen. Designing the front-end neural amplifier in deep submicron process becomes difficult due to the worse performances of the device and the harmful effects by process variation. This paper adopted a method to overcome process variation and presented a robust circuit in deep submicron process.

Conclusions

A 4-channel integrated neural recording amplifier chip with BC circuits is presented in this paper. Extensive simulations insure that the design is centered". The chip layout is verified using DRC and LVS design check with the help of verification tools. Test results shows that it is less sensitive to process variation and consumes less power compared with amplifier without BC circuit. This makes the design robust in a deep submicron process and uniquely appropriate for low-power implant application.

Methods

This section discusses important specifications of the neural recording amplifier and the detailed circuits implementation of it.

Specifications

Typical neural action potentials, or spikes, have amplitudes up to 500 μV when recorded extracellularly, with energy in the 100-Hz–7-kHz band, while low-frequency local field potentials (LFPs) have amplitudes as high as 5 mV and may contain signal energy below 1 Hz [27]. In the hippocampal prosthesis, spike signals are mainly concerned, and thus the bandwidth of the LNA is designed as 100-Hz–7-kHz and the gain of the neural amplifier is designed as 54 dB. Considering the neural amplifier will be implanted in the brain, it must dissipate little power and occupy little area; thus a maximum power dissipation less than 15 μW and core area less than 0.1 mm^2 per channel is required.

Circuits implementation

System architecture

As shown in Figure 4, each channel is composed of two amplifiers in cascade. The first stage is an open-loop pseudo differential amplifier which consists of two identical single-input-single-output amplifier. Its gain is 34 dB. The second stage is a closed-loop fully differential amplifier. Its gain is 20 dB. The noise figure (NF) of the whole circuit is shown in Eq. 1.

$$NF = 10log\Big(10^{\frac{NF_1}{10}} + \frac{10^{\frac{NF_2}{10}} - 1}{10^{\frac{G_1}{10}}}\Big) \tag{1}$$

Here, NF_1 is the noise figure of the first stage amplifier, NF_2 is the noise figure of the second stage amplifier, and G_1 is the gain of first stage amplifier. It can be seen that the greater the gain of the first stage, the smaller the system noise for the case of noise of the two stages is constant. Therefore, the gain of the first stage is designed to be large enough to achieve low noise in this design. In the architecture of the proposed 4-channel neural amplifier, first stage of each channel shares a reference amplifier as common input. Compared with simple combination of four single channel neural amplifiers, three single-input-single-output amplifiers are reduced; thus, 35% power consumption is reduced because the first stage amplifier consumes most of power.

Pseudo-resistor

A MOS-bipolar pseudo-resistor (PR) with high resistance and on-chip capacitors are employed to reject the large dc offsets generated at the electrode-tissue interface. The resistance of the pseudo-resistor is extremely high (>100 GΩ). More and more studies have adopted the pseudo-resistor in their designs since Harrizon proposed this concept in [28]. Figure 5 shows the structure of diode-connected positive channel Metal Oxide Semiconductor (PMOS) device. The PMOS works as a parasitic PNP transistor with the collector and the base connected. Thus, the current and conductance across PR can be described as follows.

$$I = I_S \exp \frac{V_{BE}}{nV_t} \tag{2}$$

$$\frac{dI}{dV_{BE}} = \frac{I_S}{nV_t} \exp\Big(\frac{V_{BE}}{nV_t}\Big) \tag{3}$$

Here, V_{BE} refers to the base-emitter voltage difference of parasitic PNP transistor, and I_S means the reverse saturation current. V_t is the thermal voltage, n is the subthreshold slope factor, and I is the current across PR. The relationship between the resistance of PR and the current across PR can be written as,

$$R_{PR} = \Big(\frac{dI}{dV_{BE}}\Big)^{-1} \tag{4}$$

When turning into deep submicron technology, the supply voltage decreases while the threshold voltage of an MOS device is almost constant; thus the gate leakage current of the PMOS device increases. Based on the above analysis, when the gate of the PMOS device connects with one end of the pseudo-resistor, a larger leakage current of about a few picoamperes exists in the deep submicron process. Thus, the voltage difference between the two ends of the pseudo-resistor becomes larger in the order of a few decade millivolts.

The first-stage amplifier

In the design of the first stage, transistors M_1–M_4 work as a cascode class C inverter [29], and the gain of the amplifier is decided by the ratio of capacitance C_1 and C_2 as shown in Figure 6. Given that the current of normal class C inverter cannot be controlled easily, transistor M_5 and connected devices (not shown in Figure 6) are added to provide a reference bias for M_1. Transistor M_1 and M_2 work in the sub-threshold region (weak inversion) to maximize the ratio of g_m/I_D while transistor M_3 and M_4 work in the strong inversion [30]. For the transistor working in the sub-threshold region, transconductance is shown in Eq. 5.

$$g_m = \frac{\kappa I_D}{V_t} \tag{5}$$

$$\begin{aligned}\frac{v_{n,in}^2}{\Delta f} &= \Big(\frac{C_1+C_2}{C_1}\Big)^2\Big[\frac{2kT}{\kappa(g_{m1}+g_{m2})}\Big(1+\gamma\frac{g_{m3}+g_{m4}}{g_{m1}+g_{m2}}\Big)\Big] \\ &+ \Big(\frac{C_2}{C_1}\Big)^2\frac{4kT\cdot PR_2}{1+sC_2PR_2-\frac{sC_2PR_2}{g_{m2}R_{out}}} \\ &+ \Big(\frac{C_1+C_2}{C_1}\Big)^2\Big(\frac{g_{m1}}{g_{m1}+g_{m2}}\Big)^2\Big(\frac{1}{1+sC_1PR_1}\Big)^2\Big(4kT\cdot PR_1+\frac{2kT}{\kappa g_{m5}}\Big)\end{aligned} \tag{6}$$

Here κ refers to the reciprocal of the subthreshold slope factor n in Eq. 2. The total input noise is given in Eq. 6, which indicates noise contributions of different devices. The first part is contributed by transistors M_1–M_4, and the second part is the contribution of PR_2, with its noise decreased by a lowpass path composed of C_2 and PR_2. The last part is contributed by PR_1 and transistor M_5, which is decreased by another lowpass path composed of C_2 and PR_1. Eq. 6 does not show the contribution of the flick noise of an MOS transistor. The flick noise of the MOS transistor can be neglected when the size of the transistor is large enough. The resistance of pseudo-resistors PR_1 and PR_2 are both high. Thus, the last two parts of Eq. 6 can be neglected. With the assumption of $C_1 \gg C_2$ and $g_{m3,4} \ll g_{m1,2}$, Eq.

6 can be simplified as,

$$\frac{v_{n,in}^2}{\Delta f} = \frac{2kT}{\kappa(g_{m1} + g_{m2})} \tag{7}$$

This design minimizes the noise of the first amplifier by obtaining a large transconductance g_m of transistors M_1 and M_2. Transistors M_1 and M_2 work in a subthreshold region to maximize g_m in the same current I_D.

The second-stage amplifier

Figure 7 shows a fully differential amplifier, and Figure 8 is the structure of the operational transconductance amplifier (OTA) used in the second stage. Similar to the first stage, the gain of second stage amplifier is decided by the ratio of capacitance C_1 and C_2. The common voltage V_{cm} is decided by the pseudo-resistor that consists of M_{11} and M_{12}, and the resistance of it is far less than PR_1–PR_2 in Figure 6. Given that a simple OTA is used, the second stage has considerable noise. However, it can be neglected because of the large gain of the first stage. The second stage must consume power less than 1 μW to meet the low power design target.

Bulk-compensated circuits

More unfavorable factors appear in the deep submicron process. As mentioned above, a voltage difference between two ends of pseudo-resistor PR_2 is about a few decade microvolts. By adopting a BC circuit proposed by Hao [31], as shown in Figure 9, the bulk voltage of M_5 is decreased; thus, its threshold voltage is decreased. Because the current across M_5 is constant, the gate voltage of M_5 increases to offset the difference voltage between the two ends of PR_2. Meanwhile, the current across M_1–M_4 is designed to be sufficiently low in the deep submicron process. As shown in Figure 9, the BC circuit that consists of M_{10}–M_{13} is designed to help transistor M_5 resisting process variation with negative feedback. The threshold voltage of transistor M_5 can be described as

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\Phi_F + V_{BS}|} - \sqrt{2\Phi_F}\right) \tag{8}$$

Here, V_{TH0} is the threshold voltage when V_{BS}=0, γ is the body-effect coefficient, Φ_F is Fermi potential and the V_{BS} is the bulk-source potential difference. When the threshold voltage of M_5 decreases due to process varieties, transistor M_{11}, as a sensor transistor, also decreases in threshold voltage. Thus, the current I_1 increases, and I_2 also increases because of the current mirror that consists of M_{12} and M_{13}. The bulk voltage of M_5 (V_{bulk}) decreases, and thus the threshold voltage of M_5 increases. When the threshold voltage of M_5 decreases or increases because of the process varieties, the bulk voltage of M_5 will be changed by the negative feedback path that consists of M_{10}–M_{13} to lessen the impact of threshold voltage variation. Thus, transistor M_5 can provide a highly stable bias current for transistors M_1–M_4 in a deep submicron process.

Acknowledgements
We thank the Zhejiang University School of Medicine for their help with this project.

Funding
Not applicable.

Abbreviations
ADC: analog-to-digital convertor; MOS: metal oxide semiconductor; BC: bulk-compensated; CMOS: complementary metal oxide semiconductor; NEF: noise efficiency factor; DRC: design rules check; LVS: layout versus schematic; BMI: Brain Machine Interface; LNA: low-noise amplifiers; MIMO: multi-input multi-output; NS: neural stimulator; LFPs: local field potentials; NF: noise figure; PR: pseudo-resistor; PMOS: positive channel Metal Oxide Semiconductor; OTA: operational transconductance amplifier.

Availability of data and materials
All data generated or analyzed during this study are included in this published article.

Ethics approval and consent to participate
Not applicable.

Competing interests
The authors declare that they have no competing interests.

Consent for publication
Not applicable.

Authors' contributions
MN was responsible for the system design, circuits simulation, data analysis, and took the lead on manuscript writing and figures drawing. JL made significant contribution to the background review and experiment measurement. YH supervised this research and revised the manuscript. All authors read and approved the final manuscript.

Authors' information
The School of Micro-nano Electronics, Zhejiang University

Author details
the School of Micro-nano Electronics, Zhejiang University, Hangzhou, China.

References
1. Zhang, J.: Basic neural units of the brain: Neurons, synapses and action potential. arXiv preprint arXiv:1906.01703 (2019)
2. Ferrier, D.: The Functions of the Brain. Smith, Elder, New York (1886)
3. Alzheimer's Disease Internationa: World Alzheimer Report 2020 (2020). https://www.alzint.org/about/dementia-facts-figures/ Accessed Accessed 5 Dec 2007
4. Godyń, J., Jończyk, J., Panek, D., Malawska, B.: Therapeutic strategies for alzheimer's disease in clinical trials. Pharmacological Reports **68**(1), 127–138 (2016)
5. Chai, R., Naik, G.R., Ling, S.H., Nguyen, H.T.: Hybrid brain–computer interface for biomedical cyber-physical system application using wireless embedded eeg systems. BioMedical Engineering OnLine **16**(1), 5 (2017)
6. Berger, T.W., Song, D., Chan, R.H., Marmarelis, V.Z., LaCoss, J., Wills, J., Hampson, R.E., Deadwyler, S.A., Granacki, J.J.: A hippocampal cognitive prosthesis: multi-input, multi-output nonlinear modeling and vlsi implementation. IEEE Transactions on Neural Systems and Rehabilitation Engineering **20**(2), 198–211 (2012)
7. Xu, H., Han, Y., Han, X., Xu, J., Lin, S., Cheung, R.C.: Unsupervised and real-time spike sorting chip for neural signal processing in hippocampal prosthesis. Journal of neuroscience methods **311**, 111–121 (2019)
8. Qiao, Z., Han, Y., Han, X., Xu, H., Li, W.X., Song, D., Berger, T.W., Cheung, R.C.: Asic implementation of a nonlinear dynamical model for hippocampal prosthesis. Neural computation **30**(9), 2472–2499 (2018)
9. Li, X., Zhong, S., Morizio, J.: 16-channel biphasic current-mode programmable charge balanced neural stimulation. Biomedical engineering online **16**(1), 104 (2017)
10. Karpul, D., Cohen, G.K., Gargiulo, G.D., van Schaik, A., McIntyre, S., Breen, P.P.: Low-power transcutaneous current stimulator for wearable applications. Biomedical engineering online **16**(1), 1–13 (2017)
11. Lyu, L., Ye, D., Shi, C.-J.R.: A 340 nw/channel 110 db psrr neural recording analog front-end using replica-biasing lna, level-shifter assisted pga, and averaged lfp servo loop in 65nm cmos. IEEE Transactions on Biomedical Circuits and Systems (2020)
12. Kim, S.-J., Han, S.-H., Cha, J.-H., Liu, L., Yao, L., Gao, Y., Je, M.: A sub-μw/ch analog front-end for δ-neural recording with spike-driven data compression. IEEE transactions on biomedical circuits and systems **13**(1), 1–14 (2018)
13. Zheng, J., Ki, W.-H., Tsui, C.-Y.: A fully integrated analog front end for biopotential signal sensing. IEEE Transactions on Circuits and Systems I: Regular Papers **65**(11), 3800–3809 (2018)
14. Liu, Y., Luan, S., Williams, I., Rapeaux, A., Constandinou, T.G.: A 64-channel versatile neural recording soc with activity-dependent data throughput. IEEE transactions on biomedical circuits and systems **11**(6), 1344–1355 (2017)
15. Kumaragamage, C.L., Lithgow, B.J., Moussavi, Z.: Development of an ultra low noise, miniature signal conditioning device for vestibular evoked response recordings. Biomedical engineering online **13**(1), 6 (2014)
16. Wu, C.-Y., Cheng, C.-H., Chen, Z.-X.: A 16-channel cmos chopper-stabilized analog front-end ecog acquisition circuit for a closed-loop epileptic seizure control system. IEEE transactions on biomedical circuits and systems **12**(3), 543–553 (2018)
17. Altaf, M.A.B., Zhang, C., Yoo, J.: A 16-channel patient-specific seizure onset and termination detection soc with impedance-adaptive transcranial electrical stimulator. IEEE Journal of Solid-State Circuits **50**(11), 2728–2740 (2015)

18. Rezaei, M., Maghsoudloo, E., Bories, C., De Koninck, Y., Gosselin, B.: A low-power current-reuse analog front-end for high-density neural recording implants. IEEE transactions on biomedical circuits and systems **12**(2), 271–280 (2018)
19. Han, M., Kim, B., Chen, Y.-A., Lee, H., Park, S.-H., Cheong, E., Hong, J., Han, G., Chae, Y.: Bulk switching instrumentation amplifier for a high-impedance source in neural signal recording. IEEE Transactions on Circuits and Systems II: Express Briefs **62**(2), 194–198 (2014)
20. Chandrakumar, H., Marković, D.: An 80-mvpp linear-input range, 1.6-Gω input impedance, low-power chopper amplifier for closed-loop neural recording that is tolerant to 650-mvpp common-mode interference. IEEE Journal of Solid-State Circuits **52**(11), 2811–2828 (2017)
21. Tohidi, M., Madsen, J.K., Moradi, F.: Low-power high-input-impedance eeg signal acquisition soc with fully integrated ia and signal-specific adc for wearable applications. Ieee Transactions on Biomedical Circuits and Systems **13**(6), 1437–1450 (2019)
22. Chandrakumar, H., Marković, D.: A high dynamic-range neural recording chopper amplifier for simultaneous neural recording and stimulation. IEEE Journal of Solid-State Circuits **52**(3), 645–656 (2017)
23. Li, Q., Wang, X., Liu, Y.: A 60 nv/$\sqrt{}$ hz $<$ 0.01%-thd$\pm$200 mv-dc-rejection bio-sensing chopper amplifier with noise-nonlinearity-cancelling loop. IEEE Transactions on Circuits and Systems II: Express Briefs **67**(2), 215–219 (2019)
24. Guo, J., Yuan, J., Huang, J., Law, J.K.-Y., Yeung, C.-K., Chan, M.: 32.9 nv/rt hz $-$60.6 db thd dual-band micro-electrode array signal acquisition ic. IEEE journal of solid-state circuits **47**(5), 1209–1220 (2012)
25. Uehlin, J.P., Smith, W.A., Pamula, V.R., Perlmutter, S.I., Rudell, J.C., Sathe, V.S.: A 0.0023 mm^2/ch. delta-encoded, time-division multiplexed mixed-signal ecog recording architecture with stimulus artifact suppression. IEEE Transactions on Biomedical Circuits and Systems **14**(2), 319–331 (2019)
26. Gosselin, B., Ayoub, A.E., Roy, J.-F., Sawan, M., Lepore, F., Chaudhuri, A., Guitton, D.: A mixed-signal multichip neural recording interface with bandwidth reduction. IEEE Transactions on Biomedical Circuits and Systems **3**(3), 129–141 (2009)
27. Senzai, Y., Fernandez-Ruiz, A., Buzsáki, G.: Layer-specific physiological features and interlaminar interactions in the primary visual cortex of the mouse. Neuron **101**(3), 500–513 (2019)
28. Harrison, R.R., Charles, C.: A low-power low-noise cmos amplifier for neural recording applications. IEEE Journal of solid-state circuits **38**(6), 958–965 (2003)
29. Chen, Y., Han, Y., Zhang, S., Cao, T., Han, X., Cheung, R.C.: High dc gain and wide output swing class-c inverter. In: 2017 International SoC Design Conference (ISOCC), pp. 53–54 (2017). IEEE
30. Wang, A., Calhoun, B.H., Chandrakasan, A.P.: Sub-threshold Design for Ultra Low-power Systems vol. 95. Springer, New York (2006)
31. Luo, H., Han, Y., Cheung, R., Han, X., Zhu, D.: Bulk-compensated technique and its application to subthreshold ics. Electronics letters **46**(16), 1105–1106 (2010)

Figures

Figure 1 Block diagram of the hippocampal congnitive prosthesis

Figure 2 (a)Screen capture of layout and (b) photograph of dies

Figure 3 Current consumption in 15 dies

Figure 4 Structure of the 4-channel neural amplifier

Figure 5 Structure of the PR

Figure 6 Schematic of the first-stage amplifier

Table

Figure 7 Schematic of the second-stage amplifier

Figure 8 Schematic of the OTA used in the second-stage amplifier

Figure 9 Schematic of the first-stage with bulk-compensated circuit

Table 1 Amplifier Performance Summary and Comparison

	TCASI'18 [13]	JSSC'15 [17]	TBCAS'18 [18]	JSSC'17 [20]	TBCAS'19 [21]	TCASII'19 [23]	This work with BC	This work without BC
Supply Voltage (V)	1.2	1.8	1.8	1.2	1	1.2	1.1	1.1
Power/ch (μW)	9.24	1.62	4.5	2.8	3.2	2.4	4.68	11.55
Gain (dB)	58	40	35.04	25.7	52	40	54	54
BW (Hz)	0.5-500	0.5-100	9.3k	5k	1.2k	0.5-500	100-7k	100-7k
$V_{ni,rms}$ (μV)	1.5	0.9	3.2	5.3	1.5	1.8	3.2	3.6
NEF	6.15	3.29	1.94	4.4	2.96	4.4	3.4	6.4
PEF	45.39	19.48	6.77	23.23	8.76	23.23	12.7	45
PSRR (dB)	-	-	80	76	-	-	>80	>80
CMRR (dB)	>100	97	76	>78	108	>90	>90	>90
Area (mm^2)	1.2	-	0.072	0.071	-	0.46	0.032	0.032
Process (μm)	0.18	0.18	0.18	0.04	0.18	0.18	0.04	0.04