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Research

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RESEARCH

An Analytical Approach of Error Detection and Correction for On-board Nano Satellite

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Abstract

Nanosatellites are persistently progressing and creating global communication and data transmission over the world. It builds up a colossal request for more progressed and dependable frameworks that are able to perform faster and reliable information transmission. An approach has been distinguished as a reasonable plot for the anticipation of single bit and multiple bit errors that are influencing On-board Nanosatellites. In this paper, we have proposed an Analytical Approach of Error Detection and Correction for On-board Nanosatellite. We have planned the framework with three distinctive parts as a encoding, error checking, and decoding portion separately. It has created in such a way that amid information exchange from satellite to ground station to analyze six camera pictures at the same time with the assistance of FPGA and EDAC strategies. To extend the proficiency, we have presented the progressed turbo mechanics EDAC for distinctive transfer speeds of satellite communication and execution examination with the AWGN and Rayleigh channel. EDAC strategies codes are tried in MATLAB and appeared in graphical plots. This method is straightforward and accomplishes unwavering quality and exactness, compared to other comparable strategies.

Keywords: Error detection and correction; Low density parity check; Bose–Chaudhuri–Hocquenghem codes; Turbo codes; Convolutional codes; Shannon’s theorem

1 Introduction

A nanosatellite is a device that moves in a bent way around a planet. Earth observation satellite is one of the fundamental devices for the investigation of the earth’s environment [1]. From Earth’s surface, EO Satellites applies high resolution image sensors to watch and get data on the earth’s surface and utilizes infrared for underneath observation. By watching earth from space EO satellites give fundamental data on climate observing, urban checking, natural disaster, rural development checking, and natural checking etc [2]. Error detection and correction devices nanosatellites aim to perform secured and error-less information transmission between satellite and ground station. They are subject to unsteady and unstable data corruption because of thermal noise, high energy particle impact or any other sort of noise. Single bit error and burst error are two common types of satellite data communication errors. A single-bit error implies one bit changed from 0 to 1 and a burst mistake implies more than one conjugated bit adulterated [3]. The mistake discovery handle is the primary step to error redress, which is subordinate to adding extra bits to the first information. Excess bits are accomplished through two
fundamental coding plans like convolution coding and block coding. Error correction can be classified as a Forward error correction and automatic repeat request, sometimes ARQ and FEC can be combined [3]. This strategy is called a Hybrid automatic-repeat request programmed. There are numerous frameworks outlined to distinguish and redress mistakes such as EDAC utilizing turbo code, BCH code, Convolutional code, Shannon’s theorem increments the proficiency of EDAC we presented a progressed turbo component with two interleaved and five encoding forms and five interpreting forms [4]. Progressed turbo mechanism is tried in MATLAB with AWGN and Rayleigh channel.

The main contributions of this paper are as follows:

- We have proposed an architecture that consists of the EDAC method for the nanosatellites.
- We have studied, analyzed and compared the error detection and correction algorithms that are used by the satellites.
- We have identified the number of erroneous bits. Based on that we have also proposed suitable error correction methods.
- We have implemented the scheme for the LDPC, BCH, Turbo, Convolutional and Shannon’s theorem.
- We have analyzed the performance of five different EDAC algorithms with two different channels in MATLAB.
- Finally, we have identified the limitations of our proposed methods.

The rest of the paper has been depicted within the taking-after way. Segment I examine the EDAC strategies of nanosatellites. The objective behind the investigation has been displayed in segment II and the proposed a method of framework engineering has been talked about in area III. Area IV appears the algorithmic investigation and performance analysis of EDAC Mechanism V-1.1. Area V and VI describe the EDAC Mechanism V-1.2 and EDAC Mechanism V-1.3. Area VII examines the execution of result advancement. Area VIII describe the limitation and future work of EDAC. In conclusion, area IX concludes our paper.

2 Literature Review

Mamun et al. [1] proposed a Hamming Code to prevent parity and parity single bit error onboard satellite in LEO. The main focus is to work on Error Detection and Correction via generating a Hamming Code matrix. After comparison with other Hamming codes, Cycle redundancy check, etc. The schematic limitations from the generated Hamming codes [16, 11, 4] were proven to be the most efficient. MATLAB is used for the implementation process. Both single-bit and double bit errors can be solved via this algorithm.

Pakartipangi et al. [5] proposed a technique to obtain wider coverage area images for low dimensions satellites. Using camera array wider and detailed images found via this system. The system handles all the errors bit using XULA2 LX9 FPGA board. Camera array was designed such way that has overlapping area can’t be found.
Ahmed Hanafi et al. [6] proposed an SRAM-based FPGA technology that implements an onboard computer system and used low earth orbit Nanosatellites. The hardware and software architecture system is based on Xilinx’s Spartan 6 FPGA. The system was designed for developing a payload architecture and an inherent space environment.

Ibrahim et al. [7] proposed a satellite system designed with acceptable accuracy in a low power budget. The latest FPGAs are capable of adopting orbital changes to combat external hazards. This paper presents a concept to establish avionics systems by utilizing crucial features with the available FPGAs. Scrubbing keeps the FPGA data configurations safe with frame calculation and back-tracking method.

Daniel et al. [8] proposed a technique that describes a guideline for simulating the system accuracy providing the necessary statistics to support the decision system regarding the necessary methodology to be implemented[8]. The system design such a way that it can be monitor air pollution in Mexican and Latin American cities. Atmospheric pollutants from cars, volcanoes, industrial areas etc. need to be monitored to keep the spectrometer in the infrared or ultraviolet range[8]. Author designed this system based on COTS devices.

Wilson et al. [9] proposed two major supervise themes hybrid computing and re-configurable computing[9]. The system survey of the impose and convenience for small satellites and also focuses on new technologies, methods and implementation for the next generation[9]. New technologies such as CHREC Space Processor that demonstrates how system designers can feat hybrid and reconfigurable computing on SmallSats to harness these advantages for a variety of purposes[9].

Banu et al. [10] proposed an encryption method to secure terrestrial communication via small satellite. Increased quantity of sending valuable and sensitive data, a satellite can bring risks of providing access to unauthorized data. An advanced encryption standard method is used to protect data from such threats. Satellite operates in a harsh environment surrounded by radiation and magnetic fields which can cause malfunctions in the satellite system and cause fatal faults. The advanced encryption system is strong enough to handle this fault to protect the valuable data and uninterrupted data transmission from potential corruptions.

Banu et al. [11] proposed a commercial algorithm also known as advanced encryption standard. In order to protect valuable and sensitive data and prevent unauthorized access in terrestrial communication, 5 modes of AES in satellite imaging has been used. To prevent fault from noisy channels and effect of SEUs, those 5 modes were analyzed and observed using Hamming error correction code. Measurements of power and throughput overhead were presented with the implementation of FPGA.

Hiler et al. [2] proposed a parity check matrix and a calculated syndrome of error detection and correction on board nano satellites. The scheme can self-detect and self-correct any single event effects error that occurs during transmission[2]. Cryptographic protection is used to secure transmissions from being hacked. MATLAB
and VHDL were used to test out three types of Hamming Code methods. Among them, the most efficient version was Hamming [16, 11, 4].

BENTOUTOU et al.[4] proposed an onboard EDAC method to protect data transmission among AISAT-1 CPU and its memory. The following paper presents the applications of double bit EDAC and implementation with FPGA. The EDAC is calibrated and computed with 3 kinds of techniques.

Wang et al.[12] execution comparison of devotee goof correction codes for correcting colossal burst data botches. Colossal burst goofs as regularly as conceivable happen in flunky communication driving to different chosen bit goofs. Interior parts of the paper, we make a comparison among the CCSDS codes, such as RS codes convolution, turbo, and LDPC codes.

Gao et al.[13] gives a thought of LDPC codes for joint attendant and characteristic broadcasting framework. In this paper, we show earthbound broadcasting framework which is called another Time Broadcasting-Wireless and Specialist and will be gotten a handle on inside the more conspicuous China run and some of the other parts of Asia. This framework requires amazing execution, especially for combined deciphering.

Wang et al.[14] wireless sensor network where encoding algorithm and decoding algorithm both are described with the implementation of rateless and LDPC code. The performance was compared in the WSN environment by a MatLab simulation. Rayleigh channel in MatLab was used to make this simulation. The result and conclusion of this paper are actually based on the simulation performed in MatLab.

Biazaran et al.[15] introduced a numerical method into set audio limits for LDPC codes that use the message conveying the algorithm to an additional white Gaussian audio channel. A process in a flat not related to Rayleigh withers channel has been used. A nonlinear code optimization process has been used and efficient performance has been shown in unusual LDPC codes for such a channel. Headers for unorganized LDPC codes are very close to Shannon the limit of this channel. For example, on a half-scale scale, optimized the standard LDPC code has only a limit of 0.07 dB away from its channel capacity. In addition, simulations performance of well-prepared LDPC and turbo codes in the mobile world, the station has been compared, and the results have shown that in 3072 block size, standard LDPC codes can exceed turbo codes for various types of mobile speeds.

Brandonisio et al.[16] presented Forward error correction based on Reed Solomon inserts a high-level code for the ascent Passive optical networks are analyzed in detail using flexible gate configurations to achieve real burst mode transfer. For FPGAs, certain construction solutions are required. In particular, the burst mode and burst mode the reed - Solomon’s Sodomite is described in detail as well analyzed by testing within state-of-the-art Long reach PON testbed. At the time of this analysis, the river was high FEC performance is disabled by the presentation
is highly consistent and errors made within the explosion of reduction of the first painful period. Visual FEC degradation is fully analyzed using in FPGA the error location analysis tool as well estimates of frame loss. This investigation shows the importance of understanding the error distribution within the blast to accurately measure FEC performance on PON mounting links.

3 Methods
Satellite On-board command data handling structure are shown in figure 1. For a low-cost framework of the nanosatellite, a single chip executed On-board command information dealing with (OBCDH) was proposed for a mixed-mode application specific coordinates circuit (ASIC) [6]. Future Nano Satellites which having information handling and control capacities with information collecting and further detecting capabilities for Soil perception Missions are the result of ASIC detail. Square graph 1 comprises of 4 Subsystems where a 32-bit RISC processor center adjusted for space utilization, a Subsystem of picture dealing with the unit, a communication association for the satellite and a supporting fringe subsystem. OBC is the most component of to scaled-down OBCDH framework. To serve an introductory model of the advanced portion of the OBCDH ASIC, this onboard computer framework on a chip figure 1. Within the OBCDH our fundamental need is to upgrade the EDAC framework so that we are able to have error-free information on disciple communication. In EDAC mechanism V-1.1, V-1.2 and V-1.3 describe the different approach to solve the satellite communication error and analyze the performance of different channel.

4 EDAC Mechanism V-1.1
Nanosatellites that transmitted information to the ground station from their blunders can be checked with the assistance of a few calculations. Within the ground station, CRC checks blunder information. After that step with a sort of blunder, able to get the information indicated by detection methods. Within the location strategies, we figure out whether blunders are shown in our data in case of able to distinguish by means of three steps like information word codeword generator at that point able to recognize the erroneous bit within the input stream appeared in figure 2. Based on our mistakes we ought to alter our calculations agreeing to the measure of mistakes. In this adjustment strategy like Hamming redress, CRC adjustment, and Reed Solomon rectification. With the assistance of these adjustment strategies, we would present at long last get our wanted errorless information.

4.1 Hamming code
Hamming code could be a direct piece code for blunder location and redress. Hamming codes can identify one-bit or two bits mistakes at the same time and it can rectify as they were single-bit mistakes. The fundamental concept of the hamming code is to include an equality bit after the stream of information to confirm that the information was gotten by the ground station and matches the comparing input information stream. Partisan ground stations check the transmitted information in such a way that they distinguish where the mistake has happened. The structure of
the hamming code has square length, message length, and separate. square length characterizes as \( n = 2r - 1 \) where \( r \geq 2 \) message length and remove is \( 2r - r - 1 \). Depending on the hamming code adaptation remove esteem got changed. Due to including more than one equality bit, this conspire can find the position of the blunder and self-correct it by altering the bit. Generally, three sorts of hamming codes are utilized in Nano-satellite communication such as Hamming\([7,4,3]\), Hamming\([8,4,4]\), and Hamming\([16,11,4]\).

4.2 Cyclic Redundancy Check

CRC is the method of accepting emerging alter blunders within the communication channel. Satellite information trade is based on CRC codes and the EDAC process broadly utilized in advanced CRC code is additionally commonly alluded to as polynomial codes -1 on a lean wire, by working on a lean wire is characterized as polynomial checks. The k-bit message is considered a polynomial condition list with the words k, from \( x^{(k-1)} \) to \( x^0 \). The most noteworthy arrange is the coefficient of \( x^{(k-1)} \), the another thing is the proportionate of \( x^{(k-2)} \), and so on. Test digits are created by rehashing the k-bit message \( x^n \) and part the produced by \( rm(n+1) \) bits polynomial code. The excit e n -bit adjust is passed as test digits. The total collection grouping is separated by the same polynomial generator. If the remaining pieces are zero, no mistakes have occurred. If the remaining pieces are not zero, an exchange blunder happened.

4.3 Reed Solomon

Reed Solomon codes are work with a burst sort of information mistake. It moreover utilized as a broadcast framework in adjustment code communication additionally in capacity framework etc [17]. It recognizes the burst blunder of information transmission and amends those blunder information. In the event that the Reed Solomon codes are utilized at that point, the likelihood of an error remaining within the decoded information will be much lower [18]. Reed Solomon codes are too appropriate for different burst blunder adjustment codes as a grouping of \( b + 1 \) sequential mistakes can influence up to 2 signals of measure exciteb [19]. The excitet alternative goes to the coding architect and can be chosen over a wide range. Reed Solomon’s mistake adjustment may be a forward-looking blunder code [20]. It works with polynomial tests of information. Polynomials have been tried in a few places and these numbers are either transmitted or recorded.

4.4 Performance analysis of EDAC Structure

In this figure 3, we have outlined as knead bits to equality check lattice at that point generator lattice and at last adjusted code. To begin with, characterize code word bits per piece, knead bits per piece, equality sub-matrix, generator lattice, and parity-check network. Encode message and discover the position of the blunder in code word (list). At that point, code alters and adjusted code. After all, evacuate blunder information at that point plot this figure 3.

In this figure 4, we have planned input and yield messages with the assistance of CRC. To begin with, we take the input and generator network. At that point
discover checksum. After discovering the checksum we include a checksum to message bits at that point we check yield is in the event that the update is non-zero a transmission mistake has happened and update zero no blunders happened. At that point the plot yield figure 4.

In this 5, we have outlined Reed Solomon code as input and yield messages. Reed Solomon code is utilized to adjust the burst blunders related. This code is characterized by three parameters an letter set estimate $t$, square length excitten, and message length $k$. Decoder characterizes this area utilize Reed Solomon code see of code-word as polynomial esteem is based on message encoded. The decoder recovers encoding polynomial from gotten message information in figure 5.

4.5 EDAC Mechanism V-1.2
4.6 Turbo Encoding Mechanism
The Turbo Encoder block uses a parallel concatenated coding scheme to encode a binary input signal\cite{21}. Three identical convolution encoders and two internal interleavers are used in this coding scheme figure 6. An interleaver is used between systematic encoders of convolution as In Figure 6 seen. Here, we can hit a rate of 1/3, without puncturing and 1/2, with a form of puncturing\cite{22}. Other code rates are also obtained by the process of puncturing.

4.7 Turbo Decoding Mechanism
Turbo decoder is applied when turbo encoded data is applied to transmission over the AWGN channel via Base-Band, The Log-Map decoding structure offers less complex output similar to the limit of Shannon with less complexity. Turbo decoder consists of interleaver and de-interleaver separated SISO decoders as shown figure 7.

4.8 Additive White Gaussian Noise Channel
The Added substance White Gaussian Noise (AWGN) channel is one of the most commonly utilized channels demonstrate by large utilized to show an environment with an exceptionally expansive number of added substance noise sources. Most added substance commotion sources in modern electronics are a coordinate result of zero-mean warm noise, which is caused by random electron movement inside the resistors, wires, and other components. The AWGN channel may be a well-known model to demonstrate the line of locate (LOS) conditions. This channel show is utilized to assess the contrast between a LOS show and a channel demonstrate counting fast-fading impacts. Consequently, the AWGN comes about can be seen as reference estimations.

4.9 Rayleigh Channel
The Rayleigh blurring model is in a perfect world suited to circumstances where there are huge numbers of flag ways and reflections\cite{23}. Ordinary scenarios consolidate cellular broadcast communications where there’s an expansive number of reflections from buildings and the like conjointly HF ionospheric communications where the uneven nature of the ionosphere suggests that the in general hail can arrive having taken various assorted ways. In this proposition, a moderate level autonomous
Rayleigh blurring channel demonstrate is used for the blurring environment[24]. An autonomous Rayleigh blurring handle can be modeled as a steady irregular variable amid each image interim. In arrange to introduce the impact of the autonomous blurring channel, an arbitrary Rayleigh disseminated number is generated, to this number, we include the AWGN to mimic the total impact caused by the channel.

4.10 Performance analysis of Advance turbo mechanism
Turbo codes are better performance codes that result from the interaction of information between recursive codes and decoders of the constitution in figure 8. Turbo code simulated for Rayleigh faded channel for frame size $K = 40$. Frames number in each SNR taken as $500$ to keep the simulation fast.

5 EDAC Mechanism V-1.3
Five Identical EDAC algorithms are used as encoders LDPC, BCH, Turbo, Convolutional, Shannon’s and for all the algorithms random interleaver are used in this coding scheme. Each constituent encoder is terminated by tail bits autonomously. An interleaver is used between five systematic encoders of convolution as in figure 9. Here, we can hit a rate of 1/3, without puncturing and 1/2, with a form of puncturing. Other code rates are also obtained by the process of puncturing. The algorithm for decoding can be designed by either an A Probability posterior (APP) method or a method of maximum likelihood. Decoder consists of Five interleavers and de-interleaver separated SISO decoders, shown in figure 10. Because of noise, encoded output data bit can get corrupted and entered the input of the decoder as $r_0$ for the device bit, $r_1$ for parity-1, and $r_2$ for parity-2, $r_3$ for parity-3, $r_4$ for parity-4, $r_5$ for parity-5. They are fed to the first SISO decoder with these inputs. SISO first the decoder takes the obtained data bits as input, sequence $r_0$ and parity sequence $r_1$ got, which is RSC generated encoder 1, Sequence of output results.

5.1 Low Density Parity Check(LDPC)
Low-density parity codes are linear block codes. LDPC codes have shown a lot of attention errors performances impending the Shannon limit [15]. LDPC transmits a message bit over a noisy transmission channel. LDPC was established using a sparse Tanner graph. LDPC can be decoded block-length in linear time. LDPC codes are two classes: i) regular code ii) irregular code. A regular LDPC matrix is an $N \times M$ binary matrix that has exactly one in each column and $\rho$ one in each row where $\gamma < \rho$ and both are smaller than m. If $H$ is low-density, then the number code of 1 in each row or column is called a random LDPC code if it is not continuous. The constant code is called the irregular LDPC code. It is also possible to see the regularity of these codes when viewing graphical representations. Each V-node and all C-nodes have the same number of incoming edges. The LDPC codes invented by Gallacher were regular codes. Both random codes show the best error work as N increases in the acceleration limit. The A load of code manages the hamming outpace among codewords increases as the number of entries increases. Hamming outpaces among two codewords is a defined number of separate locations in the codeword. LDPC code performance Near Shannon limit, LDPC code clean decoding method data-passing and Low decoding difficulty. LDPC code allows parallel implementation.
LDPC codes have already been adopted as standards for satellite-based digital video broadcasting and long-hole optical communication, possibly acceptable to IEEE wireless local area network standards, and will be considered for the long-term evolution of third-generation mobiles. It is also used for 10GBase-T Ethernet Twist-pair cables that transmit data at 10 gigabytes per second [25]. One of the most popular topics in coding theory is LDPC codes. LDPC encoding difficult thing to implement. In the case of simulations, encode is done by multiplying the matrix, as most personal computer memory allocations can handle these activities by a large operation.

5.1.1 Low density parity check Encoder
LDPC encoding is difficult things to implement. In the case of simulations, encode is done by multiplying the matrix, as most personal computer memory allocations can handle these activities by large operations. Now determine how generated matrix G. We will use the following definition of the syndrome to determine the relationship parity bit with the H matrix. This definition is like a hamming code. Data bits multiplied and encoding applied with the help of a G matrix. G is a generator matrix of Low-Density Parity Check (LDPC) code is not requires an infrequent matrix [13]. A few design methods will be considered lower complexity of LDPC code encoding. The method is to apply the stair code. Introducing the ladder structure can be encoded at linear times as compared to repetitive decoders in H, only a single calculation is required to make the encoder effective by general multiplication. LDPC code design reversible data transmitted is used to LDPC encoder and decoder. Design circuits perform the aspect of the Tanner graph. The same circuits are using the encoding and decoding part. Such functions transfer a lot of promise in a function where the circuit area is limited.

5.1.2 Low density parity check Decoder
Best effective decoders for LDPC codes can realize by applying repeat message-passing decoders[14]. LDPC code represents by parity check matrix H. Tanner’s graph is a graph presentation of LDPC, parity matrix. Tanner graph using defined sets of nodes. 1st variable nodes refer to a single bit of valid codeword x with the length of the bits. The second set represents the checking node. Constraint a flexible agreement trust extension decoder transmits the probability between checks nodes and variable nodes. This is data transfer local data using find solutions to a difficult overall complication with less complexity. However, for this type of application, it is necessary to save all the codewords that search for 2K codewords, which are increasing significantly [26]. Faith Promotion Decoder uses repeat messages to pass checks to search for codeword X and bit nodes.

5.2 performance analysis of LDPC
AWGN Channel is considered to perform in the best possible way only reason to reduce the power of the channel[27]. The performance of LDPC on an AWGN channel in 11. Performance of LDPC codes 10^3 on AWGN channel at SNR = 0 dB and BRR 10^{-1} at the same SNR is not for any coding is higher than the original.

Rayleigh fading is considered the worst-case scenario as there is no effective way. Due to the functionality of the LDPC codes of the relay channel 12, multiple received
signals are due to events such as reflection, scratching, and refractions[28]. For example, a comparison of curves in $\text{SNR} = 5 \text{ dB}$ implies that the code is $\text{BER} \ 10^3$ for coding and not $\text{BER} \ 10^{-1}$ for no coding.

11 and 12 shows the effectiveness of LDPC codes on AWGN, Rayleigh channel. Here the curves are displayed at the same $\text{SNR} = 2 \text{ dB BER}$, respectively $10^{-4}$, $10^{-1}$. The results show that the AWGN channel provides the best performance for the LDPC. It is almost impossible to encounter AWGN channels in real-life applications. In most cases, we have to consider the Rayleigh Fading system that should be built and keeping in mind the effects of the Rayleigh channel.

5.3 Bose Chaudhuri Hocquenghem(BCH) Codes

The BCH codes give a wide assortment of straight lengths and comparing code rates. They are vital not as it were since of their adaptability within the choice of their code parameters but moreover since, at block lengths of a couple of hundred or less, numerous of these codes are among the foremost utilized codes of the same lengths and code rates[29]. Another advantage is that there exist exceptionally exquisite and effective arithmetical translating calculations for the BCH codes. The significance of the BCH codes too stems from the reality that they are competent in redressing all arbitrary designs of dread by an interpreting calculation that’s both straightforward and effectively realized in a sensible sum of hardware. BCH codes possess an unmistakable put within the hypothesis and hone of multiple-error rectification.

5.3.1 BCH Encoder

Codewords are shaped by including leftover portion after divided the message polynomial with generator polynomial. They’re products of the generator polynomial. On the encoding side, the generator polynomials are not ordinarily part because they will request more equipment and control circuitry. The polynomial is utilized as such for encoding[30]. The generator polynomial for BCH is given by $1 + x^3 + x^4 + x^5 + x^9 + x^{12}$. BCH codes are executed as efficient cyclic codes. Consequently, can be effectively actualized and the rationale which actualizes encoder and decoder is controlled into move enroll circuits. The leftover portion can be calculated within the $(n-k)$ straight arrange move registers with the input association at the coefficient of the generator polynomial. LFSR is initialized with seed esteem 0.

5.3.2 BCH Decoder

The interpreting handle of the BCH codes comprises three steps. The disorder computation prepare creates $2t$ disorders from the gotten codeword which is the data information concatenated with the equality information. At that point, the blunder locator polynomial is computed from the disorders, of which the roots point out the blunder positions. Inevitably, by thoroughly finding out the roots of it utilizing the look calculation, the mistakes are adjusted. In the event it demonstrates to be no blunder within the square, we require not one or the other to assess the mistake locator polynomial nor conduct the Chien look handle. In this way, for decreasing the interpreting time, it is exceptionally important to recognize whether there’s
any blunder or not as early as conceivable. Here, we propose to check the mistake event with a disorder polynomial by reusing the encoder which as it were requires the GFD, whereas the routine blunder location strategy employments the disorder values which require a much longer time for conducting a few diverse CGFMs.

5.4 Performance analysis of BCH Code
13 and 14, shows the BER plots vs. threshold SNR ft. for BCH code for two values of average SNR 0, 10dB and 20dB, with different Doppler frequencies. From the figures, it is clear that an increase in the performance of the BCH code occurs and for large values, the errors tend to be more random as the transition probabilities \( b \) and \( g \) increase leading to good performance since the BCH code is capable to correct such random errors.

5.5 Convolutional Codes
In later a long time, the request for mixed media applications over remote portable communication frameworks has developed exceptionally quickly. Remote versatile communication systems show a few plan challenges coming about from the versatility of clients throughout the framework and the time-varying channel. One of the most targets when transmitting data over any communication channel is unwavering quality, which is measured by the likelihood of redress reception at the recipient. Convolutional codes on the other way are one of the preeminent broadly utilized channel codes in down to earth communication systems. These codes are essentially utilized for actual time botch correction. Convolutional codes alter the total data stream into one single code-word. The encoded bits depend not as they were on the current \( k \) input bits but in addition on past input bits. As a result of the wide affirmation of convolutional codes, there have been numerous signs of progress to extend and make strides in this basic coding plot. Convolutional coding may be a broadly utilized coding technique that isn’t based on pieces of bits but or perhaps the abdicate code bits are chosen by basis operations on the appear bit in a stream and a small number of past bits.

5.5.1 Convolutional Encoder
Insides the encoder, data bits are input to a move enlist of length \( K \), called the elemental length. As each bit enters at the cleared out of the select, the past bits are moved to the proper in show disdain toward of the truth that the primary orchestrated bit insides the select is evacuated. Two or more twofold summing operations, let’s say \( r \) make code bits that leave inside the center of one data stream period.

In this way figure 15, the code bit rate is \( 1/r \) times the data rate, and the encoder is called a rate \( 1/r \) convolutional encoder of confinement length \( K \). Also required to completely characterize the encoder are the affiliations from stages insides the move select to the \( r \) summing squares. These are generator vectors each of which may be on a very basic level communicated as a push of \( K \) parallel digits.

5.5.2 State Diagram
Convolutional encoder shows up an outline with \( K = 3, r = 2 \), and the generator vectors are chosen as \([111]\) and \([11]\). Discrete looking at times are labeled \( n \). The
data stream enters on the cleared out and the show bit at time $n$, the first afterward bit $n1$ and the taking after a most reliable bit at $n2$ have the move to enlist. Two balance bits are traded out inside the between times between $n$ and $n1$ from the upper snake and after that the lower one. When the taking after data bit arrives, the move select moves its substance to the proper. The $K1$ earlier bit, in this case, two, choose the state of the encoder. They have appeared up in gray in 15.

Convolutional encoder There are $2K1$ states. For each encoder state, there are two conceivable comes about of yield code bits, depending on whether the input bit is zero or one. The advancement of states in time, at that point, can be a work of the information stream. 15 statechart may be a state chart of our layout the development of states in time, at that point, may well be a work of the information stream. Fig. State chart may be a state chart of our diagram. Each state is appeared up insides of a circle and the alter from one state to another is showed up by a jar, recognized by the input bit, cut, yield code bits. You will be able to see that encoding can be done by and huge clear equipment.

5.5.3 Convolutional Decoder
Convolutional codes are frequently alluded to as trellis codes due to the reality that trellis charts can effortlessly portray them. The trellis chart of a code records the diverse states of the encoder and the ways they are connected to. The trellis structure for the state diagram of 16 state diagram. is appeared in 16. Trellis structure for a four-state encoder. There exist two unmistakable approaches to translate a transmitted arrangement of bits. The begin with approach finds the foremost likely bit when they got incorrect grouping is known and is accomplished by.

The Viterbi calculation can be utilized by utilizing two primary procedures. The primary approach employments the difficult choice on the received noisy data bits by thresholding the information to parallel digits and after that applying the calculation, whereas, the moment approach employments delicate choice to translate the information by finding the way among all the ways of the trellis which has the largest matrix. Here we are going as it discussed the delicate choice approach. This approach not as it included an execution advantage over the difficult choice approach but too will be accommodating within the taking after chapters.

5.6 performance analysis of Convolutional code
For the event, at an SNR regard of 5dB, a bit botch rate of $10^{-5}$. was getting. That’s, in this regard, 1 bit gotten in a blunder for 100000 bits sent. This was far off predominant to when the SNR was 2dB with a bit bumble rate of $10^{-1}$. That’s 1 bit gotten in botch when 10 bits were sent. For the theoretical BER, the SNR ranges of 2dB, 2.5dB, and 3dB had a bit botch rate of $10^{-1}$ whereas inside the mirrored BER the SNR was observed to be of the expand 2dB, 2.5dB and had the same regard of BER of $10^{-1}$ whereas the SNR of 3dB of the imitated BER had an advanced BER of $10^{-2}$. This was as a result of the convolution coding displayed. Another characteristic was gotten by considering the incline of the hypothetical and imitated regard gotten as in 17 and 18.
5.7 Shannon’s Theorem

The yield of a source is first handled by an encoder, which changes over the message from one arrange to another, ordinarily a double stream, for more proficient transmission or capacity of the data. The yield of the encoder is alluded to as a flag. There are two essential forms that an encoder can execute source and channel coding. On the other hand, the objective of channel coding is to include or present additional repetition in arrange to account for conceivable unsettling influences or commotion that will influence the data amid transmission or capacity [31].

5.7.1 Shannon’s Encoding

The included repetition increments the length of the flag but permits for more prominent location and adjustment of mistakes amid the translating prepare. Common causes of channel coding incorporate the utilize of equality check bits and redundancy codes. An equality check bit is essentially an additional bit that’s included in a twofold sequence such that there’s an indeed number of 1’s. If an arrangement with an odd number of 1’s is gotten, at that point, the decoder can identify that a blunder has happened amid transmission through the channel. A reiteration code basically rehashes the message a certain number of times in trusts that the clamor within the channel would degenerate as it were a little division of the flag.

5.7.2 Shannon’s Decoding

The yield of the channel is at that point gotten by a decoder, which attempts to change over the gotten flag back to the first message. At that point, at long last, the yield of the decoder is sent to the ultimate client or goal, which is alluded to as the data sink [31]. W speaks to a message. We’ll regularly consider that it is the yield of the compressor. The encoder gets W and encodes it to Xn. The encoder puts Xn into the channel and Yn is the yield the decoder gets. At long last, the decoder tries to appraise W through Yn. The decoders appraise is signified by Wc. Our objective is to get what kind of encodings are such that Wc is the same as W with tall likelihood and n is as little as conceivable.

5.8 Performance Evaluation of shannon’s theorem

In this figure 19 and figure 20, AWGN Channel and Rayleigh fading we have used Shannon Theorem. Higher theory a scale that can be loaded with a BER, with an enabled central signal, above the B Hz bandwidth affected by the channel. By the term “unfairly BER” means that it has provided conditions for the theorem is met, in any given BER, no matter how small, we can find the coding process that benefits this BER the smaller the BER given, the harder it will be processed. The least accessible bit rate is called channel capacity C. S / N is a square signal that means the sound ratio, and the logarithm is in base 2.

6 Results and Discussion

In analytical figure 21 and figure 22, we apply two types of noise Rayleigh Channel and AWGN channel for all algorithms. AWGN Channel is considered to perform in the best possible way only reason to reduce the power of the channel. Rayleigh fading
is considered the worst-case scenario as there is no effective way. Here we can see that LDPC, Turbo, Convolutional, BCH, and Shannon’s Theorem this algorithms are best performing for different types of data. Some algorithms are good for fewer data and some algorithms are better for more data. LDPC works better when signal noise is increasing. Convolutional code works best when signal noise is medium and bit error ratio $10^{-3}$. LDPC works better for the AGWN channel. We transmitted data continuously in machine learning techniques and which type of data is best for which algorithms and identify more error data and remove error data in less time.

7 Limitation and Future Work

LDPC adds to additional bits per conversation that have been transmitted through the satellite data transmission system. An LDPC cannot detect all types of bits error. Turbo code affects single bit error correction and also detects multiple bit errors. If multiple bit error detection in this code but turbo code can only solve single bits error correction. A BCH is not suitable for security purposes. The error correction BCH alone will be a useless thing. It is more complex than a checksum and takes more processing. A strong BCH might run slowly in software. But Reed Solomon codes are not efficient as BCH codes. It cannot provide satisfying performance without BCH codes in BPSK modulation schemes.

In the future, we will introduce an advanced error detection method based on satellite transmitted data. Depending on data size, type, and importance detection algorithms will be changed. It will reduce the time of the EDAC process and get reliable safe data in a faster way. We will train your system for real-time simulation. Predicted the less error mechanism in a different type of data. We will use the machine learning technique to find less error paths. Implementing the ASCI architecture in Spartan 6 FPGA. After all, we collaborating our system architecture with Bangabandhu Satellite-1.

8 Conclusion

In this paper, we focused on different EDAC techniques. At the same time with a code correlation to the study has been regulated. This application came up with the editor with a good concern of all regular EDAC techniques. This paper represents an analytical approach to EDAC algorithms for nanosatellite data transmission systems. The prototype can be expanded or EDAC of multiple bits defect by using other more complicated error detecting and error-correcting codes alter Turbo Code, LDPC, BCH, Shannon’s Theorem, Reed Solomon codes etc. The ground station of nanosatellites are continuously maturing and growing in an impressive way. This is scheduled for the law that gives a plan of action from which the perimeters of space and technology are regularly being forced. The automation progresses memory chip cell architecture is becoming more and more solid, principally with the evolution of nanotechnology. As organizes an increasing requirement for a more developed and dependable EDAC system that is efficient in preserving the memory attitudes of nanosatellites.

Abbreviations

EDAC: Error Detection and Correction; FPGA: Field Programmable Gate Array; AWGN: Additive White Gaussian Noise; EO: Earth Observation; LDPC: Low Density Parity Check; BCH: Bose Chaudhuri Hocquenghem; LEO: Low Earth Orbit;
Declarations
Availability of data and materials
The data set used and/or analysed during the current study are available from the corresponding author on reasonable request.

Competing interests
The authors declare that they have no competing interests.

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Authors’ contributions
All authors contributed to the study conception and design. Data collection was done by MH. Methodology design were done by MH and MI. Original draft preparation including review and editing was done by MH. The study was supervised by MI. Both authors read and approved the final manuscript.

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Not applicable.

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