Wide Range Detector of Plasma Induced Charging Effect for Advanced CMOS BEOL Processes

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Abstract－**This work proposed a modified plasma induced charging recorder to widen detection range, for monitoring the possible plasma damage across a wafer during advanced CMOS BEOL processes. New antenna designs for plasma induced damage patterns with extended capacitance are investigated. By adapting the novel PID recorders, maximum charging levels of the detectors have been enhanced.**

I. INTRODUCTION

In recent years, the evolution of semiconductor process technology continues to scale down the critical dimension in large-scale integrated circuits [1-3]. Advanced FinFET logic processes has become more complex for realizing more tightly packed transistors in multi-functional and more powerful Si chips. Reactive ion etching steps enhanced by plasma [4-5] become inevitable in advanced nano-scale processes for achieving high aspect ratio structures which are essential for high packing density circuits [6]. For CMOS technology nodes beyond 45nm, the transistor gates changed from the conventional poly-silicon gate with silicon dioxide to high-k metal gate stacks [7-8]. This change not only make the devices become more susceptible to the plasma induced damage, but also might lead to unforeseen latent damages to the high-k dielectric layers [9]. In state-of-art manufacturing processes of FinFETs, numerous RF plasma steps such as etching, deposition and cleaning processes are inevitable, which create higher frequencies of plasma induced charging events [10]. Both positive and negative charging on metal structures may occur. As these charges flow through the conductive paths made of pre-existing metal lines, via and contacts, the undesirable discharging through vulnerable parts of the circuits, particularly through the transistor gate dielectric may lead to significant reliability concerns. For instance, in the dry etching step, scattering impinging ions and sputtered materials at the reaction surface cause more defects in the bulk fins [11-12]. To avoid the plasma charging event leading to irreversible damage to circuits, design rules that limit the size of metal structures are given. Other example of alleviating PID includes the usage of protective diodes, which could shunt the plasma charging current away from sensitive circuits [13]. The introduction of In-Situ Steam Generation (ISSG) gate oxide reported to improve its tolerance for plasma damage [14]. Furthermore, trimming the chamber and modifying PECVD-Ti deposition process were also found to alleviated plasma induced damage [15]. Most of these methods however result in undesirable limitations on circuit design flexibility or processing tradeoffs.

Conventionally, on-wafer test patterns have been used to monitor the plasma induced damage (PID) levels [16]. The most common and widely used parameters for monitoring on-wafer PID is the time-to-breakdown (TDDB) characteristics of the transistor gates with large antenna structures. The latent damage on gate dielectrics can be revealed by measuring the degradation of the gate dielectric layer under voltage or current stress tests. Hence, these patterns are not able to provide real-time feedback of the plasma processes [17]. In our previous works, an on-wafer plasma induced charging effect detector is demonstrated in advanced FinFET technologies. The PID recorder uses capacitive coupling structure to induced a response on the floating gate [18-20]. Therefore, there is no damage to gate dielectric layer as it does in a conventional PID recorder. On these new detectors, one measures the shifting I-V curves to find out both the intensity, duration as well as the polarity of charges on the antenna gate. It is found that these recorders may subject to saturation effect as the plasma intensity at certain recording sites exceed critical levels. To extend the dynamic range of the PID detector, new antenna gate designs have been investigated in this work, where widening of the sensing ranges are successfully demonstrated.

II. OPERATION PRINCIPLE AND TEST PATTERN DESIGN

The 3D schematic of plasma induced damage (PID) recorder with a parasitic capacitor connected to antenna node is shown in Figure 1(a). Differing from PID monitoring structure, this recorder utilizes a long contact slot to couple the antenna voltage on the floating gate. The cross-sectional TEM photograph is shown in Figure 1(b). As shown in the figure, contact slots which collect charges are capacitively coupled to floating gate. Figure 2. compares the recorded threshold voltage distributions from these recorders across a 12-inches wafer. The negative threshold voltage shift indicates that negative charges was collected on the antenna, drawing positive charges into floating gate, resulting in negative threshold voltage shifts. It is found that as the antenna area increases, the rising total capacitance leads to lowering of the overall antenna voltages, hence, smaller the shift in V_t. Here, in Figure 3(a), the flow chart explaining the basic operation principles of the PID recorder is outlined. As the plasma charge (Q_{Ant}) are collected on the antenna, the potential of antenna gate, V_{Ant}, varies. V_{Ant} is then coupled to the floating gate (FG), promoting the tunneling of electrons either into or out of FG. After plasma processes, V_{th} of these recorders may become more negative or more positive based on the polarity of Q_{Ant}. V_t can be calculated by the FN tunneling current model with the parameter listed in the Figure 3(b). From Figure 4, it is found that as the antenna area increases, $\triangle V_t$ tends to saturate. As V_{Ant} reaches the maximum levels, Q_{Ant} starts to leak out when voltage level is too high. To avoid the plasma flux level exceeding the detector limitation, the antenna capacitance is deliberately increased by adding loading capacitors which could reduce the proportion of antenna capacitance in the total capacitance. Figure 5 (a) shows the 2D structure of previously reported in-situ PID recorder, and three structures of realizing additional capacitors are presented. They are MOM capacitors, which use the larger overlap area of metal layers to increase the total capacitance in Figure 5 (b), STI capacitors, which increase the capacitance by adjusting the length of Metal Gate in Figure 5 (c), and sidewall capacitors, which use the overlap area of Metal Gate and contact to form additional capacitor Figure 5 (d).

III. Experimental Results and Discussion

Figure. 6 compares the simulation of parasitic and total capacitance with different level of additional loading capacitors. More significant effect on the total antenna capacitance is found for detector with antenna ratio under 1K. Drain current characteristics for devices of AR=10 with different STI capacitors are compared in Figure 7. When a larger loading capacitor is added, the percentage of antenna capacitance in total capacitance is reduced. Under the same plasma charging flux, the total plasma charge after a period is proportional to the antenna area. Hence, when overall capacitance increases, V_{ant} is expected to be lowered, allowing for the detection of high plasma flux level. As shown in Figure 7, smaller shifts are found on the I-V curves for the samples with added loading capacitors. Figure. 8 shows the threshold voltage during plasma process versus the total antenna capacitance on the device. A strong positive correlation indicating that as the loading capacitance increases, the detectable threshold voltage ranges increases. Box charts of the threshold voltages measured from samples with AR=1K and different sizes of MOM, STI and sidewall capacitors are compared in Figure 9. When the loading capacitance is increased, less overall threshold voltage shifts are observed. Data also suggested that the three way of adding loading capacitors can also effectively raise the detection range. The addition of a loading capacitor can successfully expand the detection range of the PID detector to the plasma charging effect, while the sensitivity of the detectors is reduced. To mitigate the effect, PID detector without loading capacitance can be kept to reflect the low PID levels, so that the dynamic range of the detector can be extended.

IV. Conclusions

This study investigates a new antenna gate design to extend the sensing range of plasma induced charging levels on the PID monitoring recorders. By adding a loading capacitor, high antenna gate voltage subject to charge leak can be prevented, allowing for higher level of charging level to be registered on the PID recorders. This novel design effectively widens the detection range of plasma charging levels in advanced CMOS BEOL processes.

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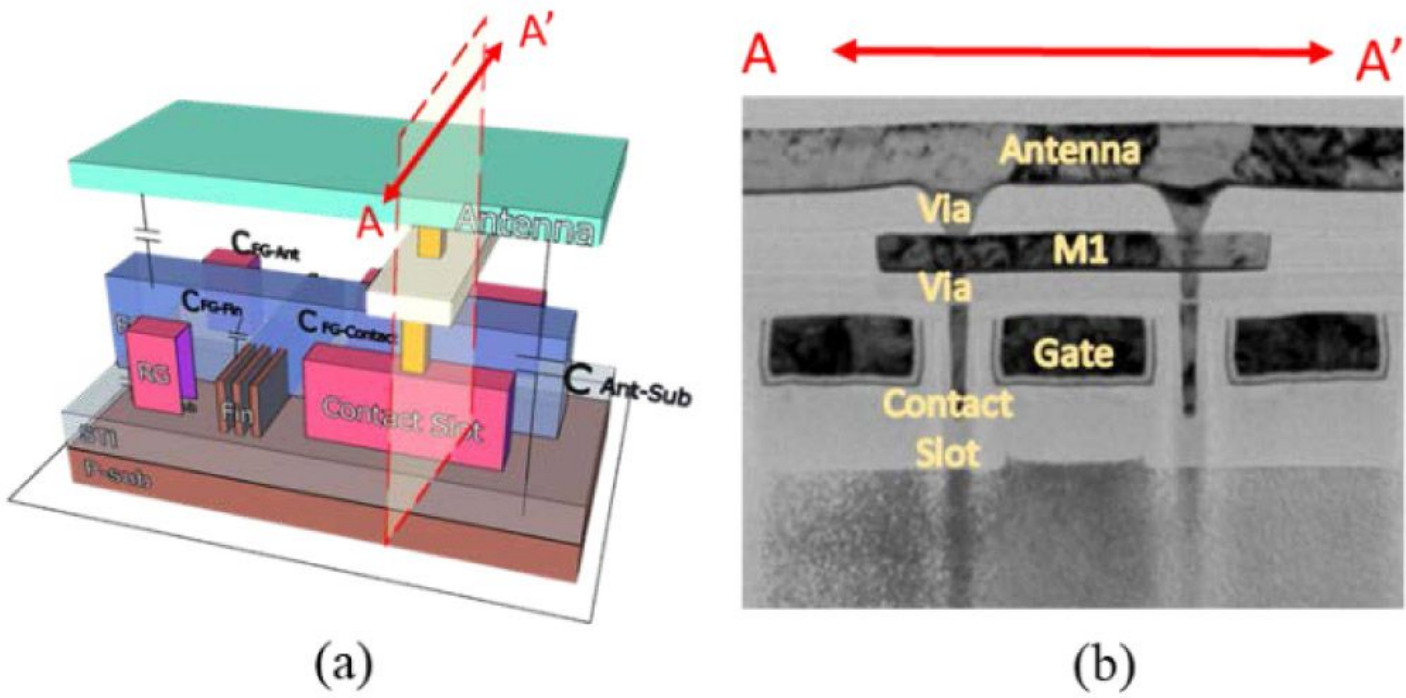
Figures

(a)

(b)

Figure 1

(a)The 3D illustrations of previously reported in-situ PID recorder and the antenna capacitor hiphliglitinp a M2 antenna in this structure.(b)The TEkf pholo of PID recorder.
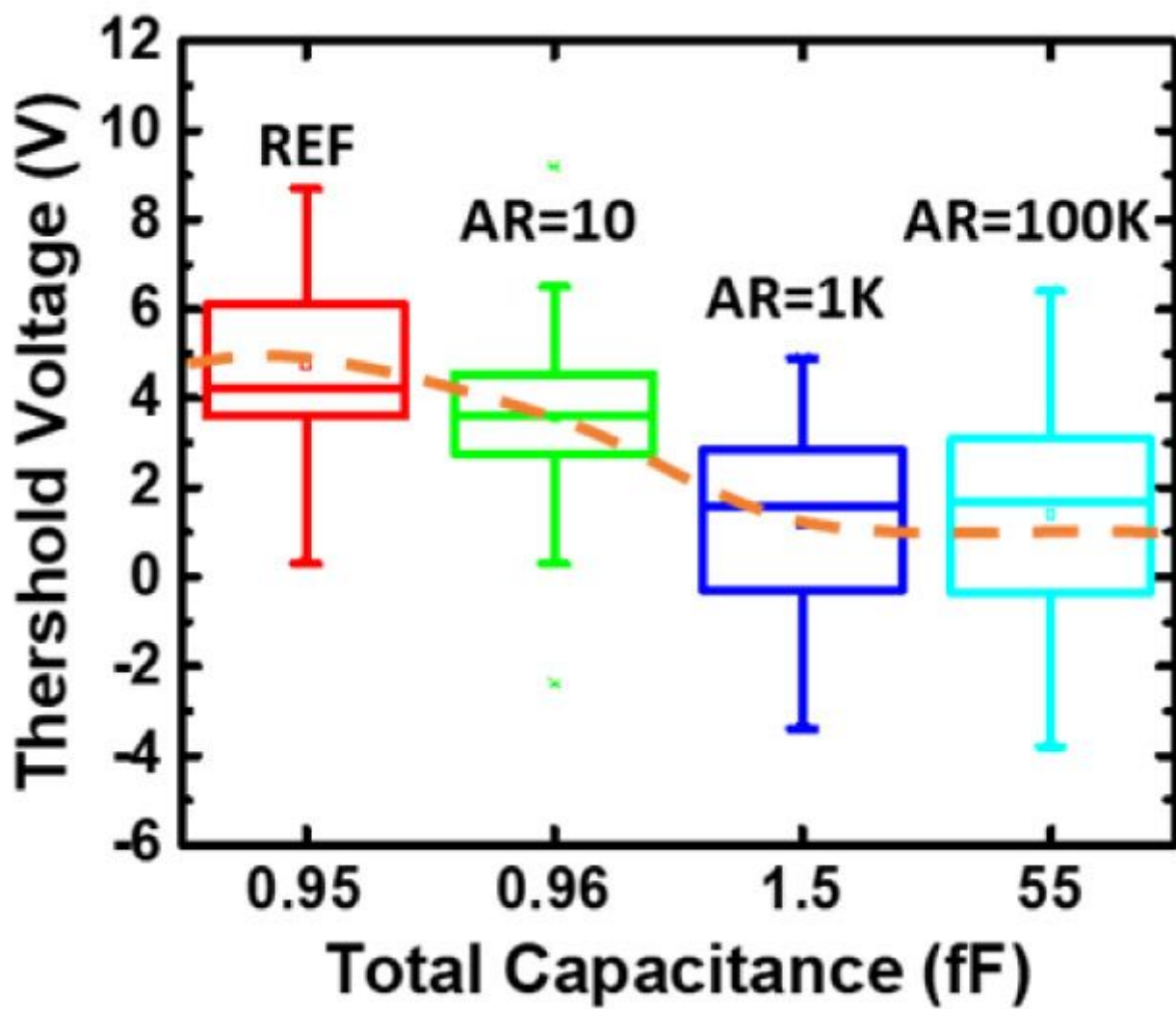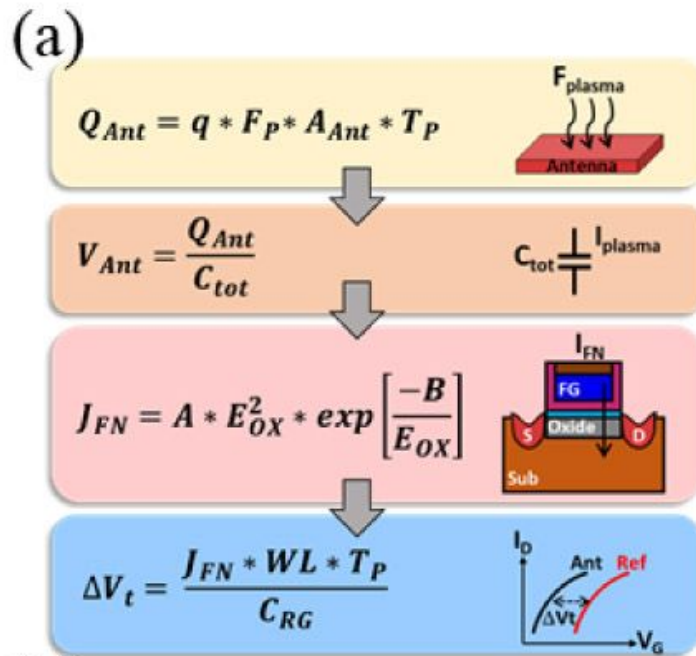
Figure 2

Threshold voltage range of samples with different size of antenna, and the corresponding total capacitance on the antenna.

(a)

$$Q_{Ant} = q * F_P * A_{Ant} * T_P$$

F_{plasma}

Antenna

$$V_{Ant} = \frac{Q_{Ant}}{C_{tot}}$$

C_{tot} ⊥ I_{plasma}

$$J_{FN} = A * E_{OX}^2 * exp\left[\frac{-B}{E_{OX}}\right]$$

I_{FN}

FG
S Oxide D
Sub

$$\Delta V_t = \frac{J_{FN} * WL * T_P}{C_{RG}}$$

I_D Ant Ref
ΔVt
V_G

(b)

Parm	Description	Unit	Parm	Description	Unit
Q_{Ant}	Charges on the antenna	Coul	E_{OX}	Electric field of oxide layer	V/cm
F_P	Plasma flux	A/cm²	V_{FB}	Flat Band voltage	V
A_{Ant}	Antenna area	cm²	T_{OX}	Oxide thinkness	cm
T_P	Plasma process time	sec	J_{FN}	FN tunneling flux	A/cm²
V_{Ant}	Antenna voltage	V	ΔVt	Threshold voltage variation	V
V_{FG}	Floating Gate voltage	V	WL	Oxide effective area	cm²
$\propto_{Ant}$	Coupling ratio of antenna		C_{RG}	Capacitance of Read Gate	

Figure 3

(a)The flow chart from plasma charges (Qp,) collected on the antenna to shift Ve Based on the FN fiinneling model, AVE can be calculated. (b)The list of parameters with its definitions.

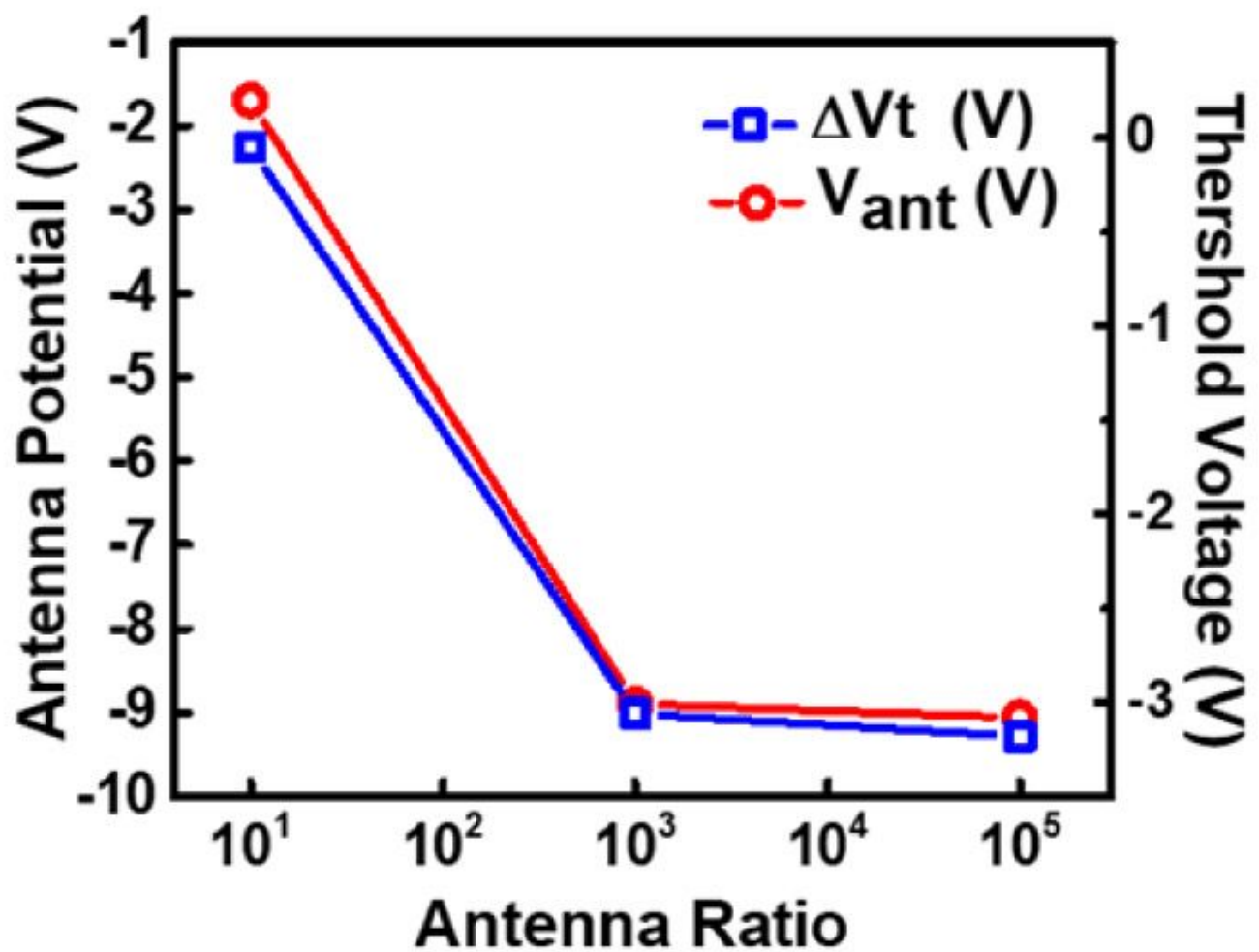**Figure 4**

Both the threshold voltage level as well as projected antenna voltage level saturates on patterns with increased antenna area.

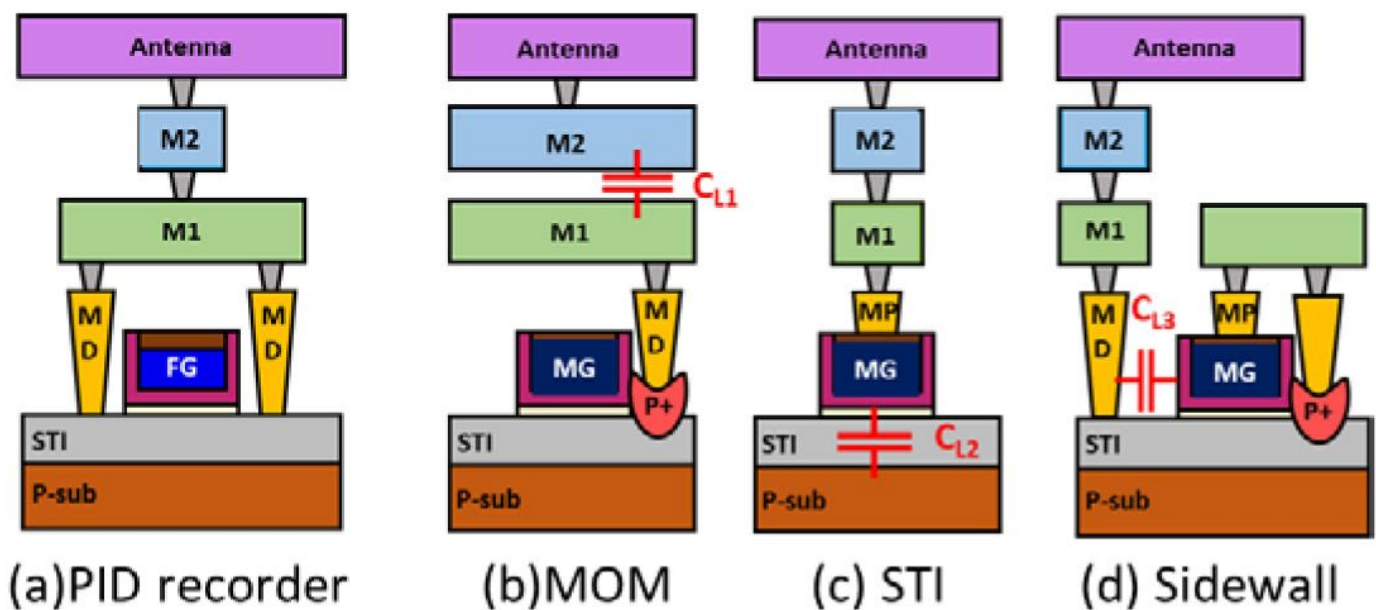(a) PID recorder   (b) MOM   (c) STI   (d) Sidewall

Figure 5

Cross sectional illustration of (a) the in-situ PID recorder, and those with an loading additional capacitor realized by (b) MOM, (c) STI, and (d) Sidewall, respectively
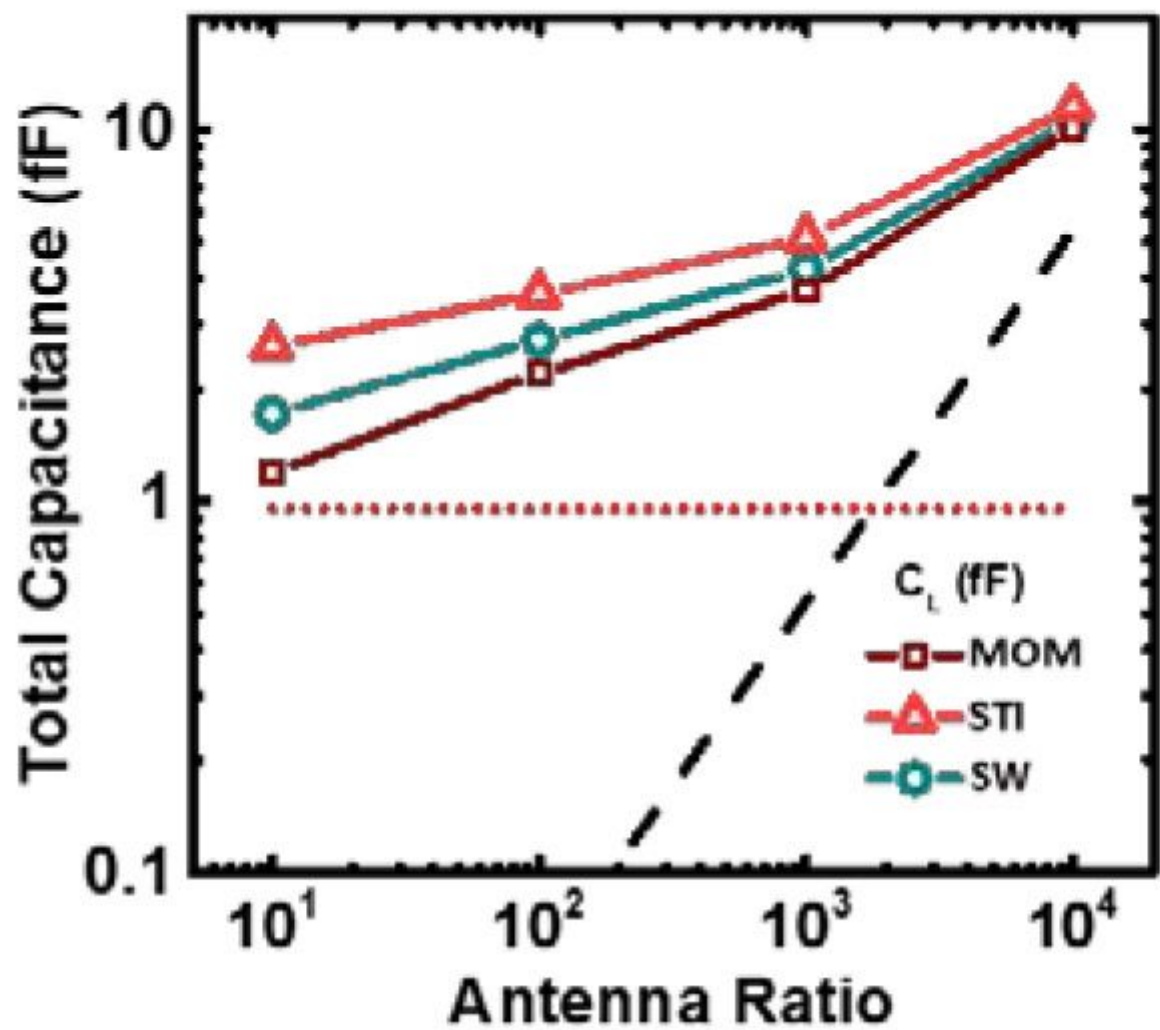

Figure 6

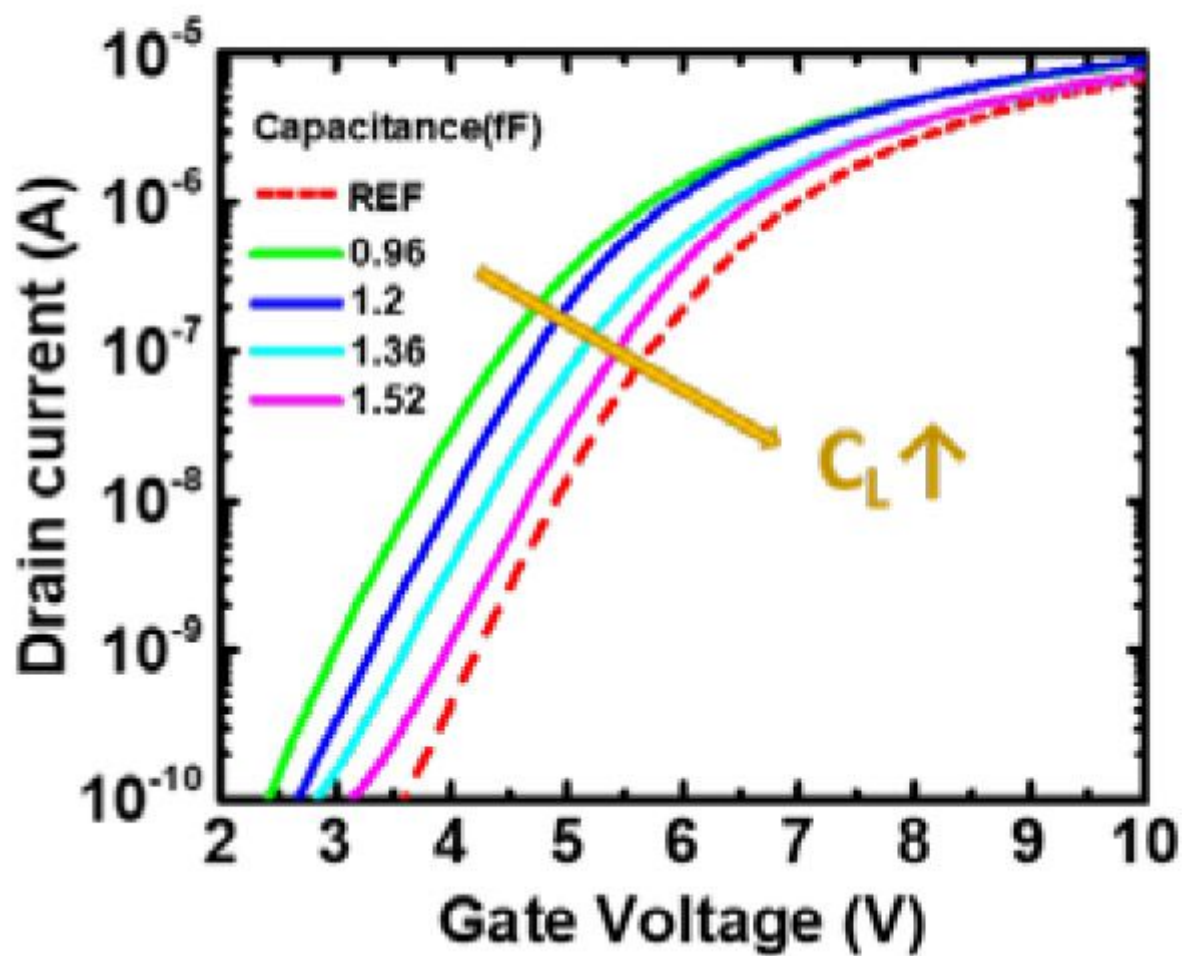Comparison of parasitic, Cp, antenna, Cant, total capacitance on the three type of samples.

Figure 7

I-V curve of different sizes of STI capacitor with AR=10. When the external capacitance is larger, the I-V curve is closer to the reference.
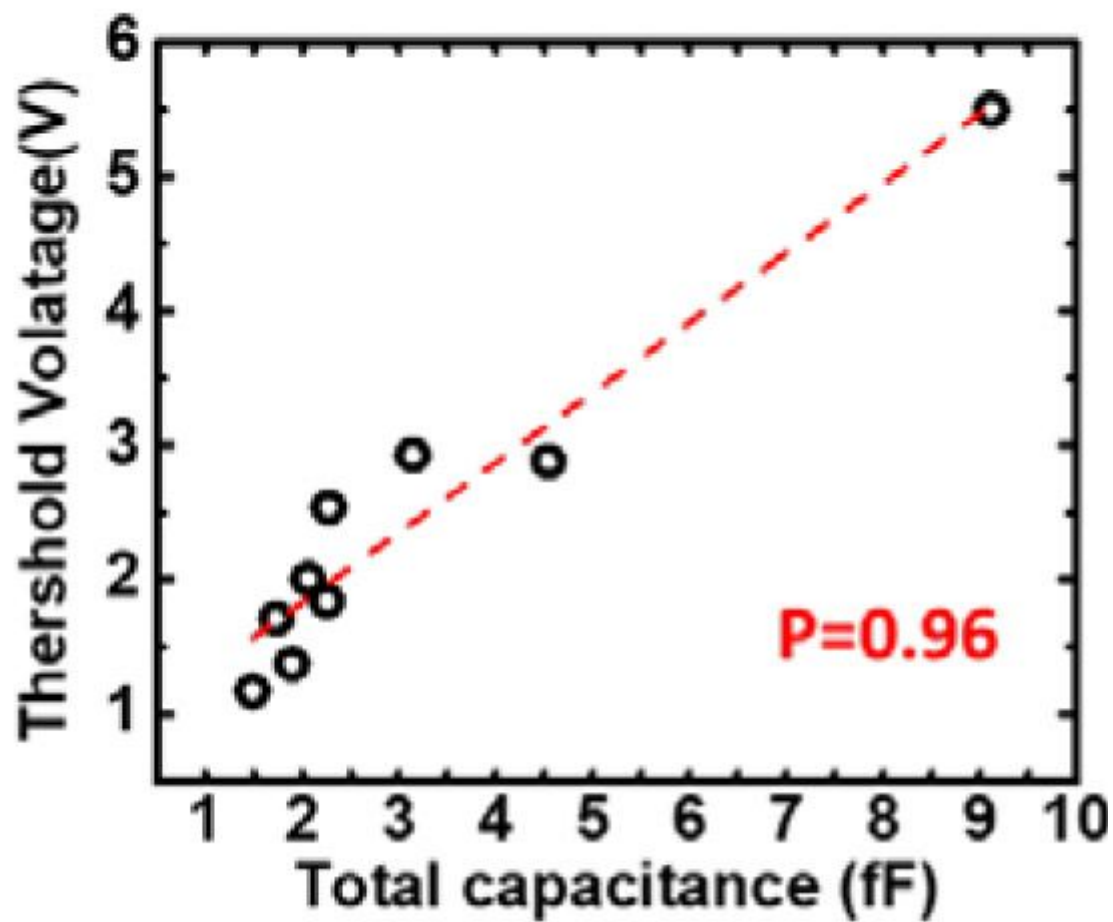
Figure 8

Correlation between the total capacitance on the antenna and average threshold voltage measured on the detections.
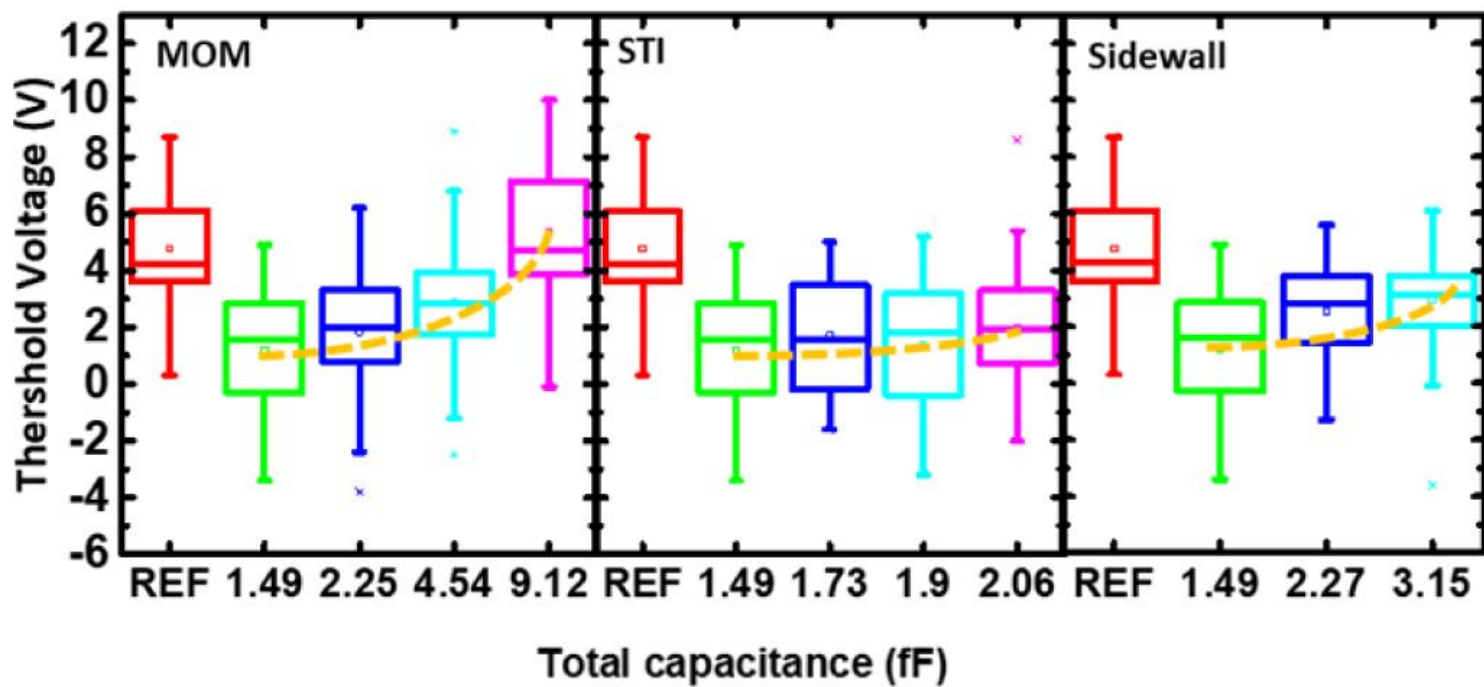
Figure 9

Threshold voltages measured on samples with different sizes of MOM, STI and Sidewall capacitors are compared. All devices have the same AR of 10.