Ultimate 0.34 nm Gate-length Side-Wall Transistors with Atomic Level Channel

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Abstract

Despite 55 years of efforts into short gate length transistors following the Moore's law, the gate length below 1 nm has not been realized. Here, we demonstrated a side-wall monolayer MoS_2 transistors with ultimate 0.34 nm gate length using the edge of graphene as gate electrode. Moreover, large area of chemical vapor deposition graphene and MoS_2 are used for 2-inch wafer production. These ultrashort devices show excellent ON/OFF current ratio of 2×10^5. Simulation results indicate that the MoS_2 side-wall effective channel length approaches 0.34 nm in the ON state. This graphene edge gate combined with MoS_2 vertical channel structure provides an efficient gate control ability and enables the physical gate length scaling down to atomic level, which shows great potential to build next generation electronics.

Main Manuscript

Since the first integrated circuit built in 1960s, silicon (Si) transistors have shrunk following the guide of Moore's law so that more devices can be built on one chip[1]. Until now, Si transistors are approaching the scaling limit when the gate length (L_g) scales down to sub-5 nm[2]. Theoretical analysis indicates that short channel effects (SCEs), including direct source-to-drain tunneling currents ($I_{SD-LEAK}$) and drain-induced barrier lowering (DIBL) effect, can influence and even terminate the scaling down process[3]. It is theoretical predicted that the minimum L_g for Si-based transistors is ~2.67 nm[4]. So, there is of great significance to explore new materials with further L_g scaling down potential.

In recent years, two-dimensional materials, dispersing wide range of electrical conductivity from semi-metal, semiconductor to insulator, have attracted great attention for next generation electronic devices[5-7]. Graphene, as a semi-metal material, shows high intrinsic electrical conductivity up to 10^8 S/m, which is very suitable as electrode[8-10]. MoS_2, as a representative for 2D transition metal dichalcogenides (TMDCs), has a larger bandgap (~1.8 eV for monolayer) than Si (~1.12 eV)[6]. Besides, its native n-doped behavior, larger electron effective mass (~0.50 versus ~0.19 for Si [100])[11], and lower dielectric constant (~3.3 versus ~11.7 for bulk Si)[12,13], leading to superior resistance to SCEs. In 2017, Xie et. al demonstrated a 3.8 nm channel length MoS_2 transistor[14]. Therefore, MoS_2 is expected to be an ideal candidate to replace Si as channel material in the future transistors[15,16].

Nowadays, for 2D material-based transistors, there are three typical device structures, as shown in Fig. 1a-c. Global back gate 2D material-based transistors are most widely studied due to the simple fabrication process[17]. But the relatively large effective oxide thickness (EOT) restrains the performance improvement. Another is the top gate 2D material-based transistors (6). EOT can be greatly scaling down to sub-1 nm through atomic layer depositing (ALD) high-k dielectric material. Therefore, subthreshold swing (SS) can be greatly reduced. However, whether for global gate or local gate, the L_g is typically determined by the resolution of lithography. Even using electron beam lithography (EBL), the L_g can be

hardly scaled down below 5 nm[18]. In 2016, Desai et. al promoted a prototype of junction-less 2D MoS$_2$ transistor using metallic single-wall carbon nanotube (SWCNT) as gate electrode, which demonstrates the L_g down to 1 nm[19]. Among the three typical transistor structures, it is hard to further scaling down L_g below 1 nm. To date, it is of great significance to explore the 2D TMDC transistors with the gate-length approaching the ultimate scaling limits.

In this work, we demonstrate a new concept of side-wall 2D transistors gated by the edge of graphene, which only have 0.34 nm L_g controlling the atomic MoS$_2$ channel (Fig. 1d). Large area CVD graphene and MoS$_2$ are used for wafer-scale production. The additional metal layer screens the electrical field from the upper surface of graphene, so that the electrical field comes from the edge of graphene, which can influence the vertical MoS$_2$ channel. The intrinsic CVD graphene has the high electrical conductivity, which can minimize the voltage drop along the gate layer. The 0.34 nm side-wall gated transistors show good switching characteristic with 2×10^5 ON/OFF current ratio. Sentaurus technology computer-aided design (TCAD) simulation results show that 2D planar characteristic of graphene gate provides efficient gate control ability, which can effectively deplete the MoS$_2$ side-wall channel close to the graphene plane. Our work promoted a production method for scaling down L_g beyond the resolution of lithography. And most importantly, it provides a great insight into the ultimate scaling, which can be regarded as the smallest node to date based on our best knowledge (Fig. 1e).

Results

Fabrication and Characterization

To fabricate the 0.34 nm gate-length side-wall transistor, monolayer chemical vapor deposition (CVD) graphene with 3 cm×3 cm size was first wet-transferred to a highly p-doped Si/ 300 nm SiO$_2$ substrate followed by patterning graphene as gate electrode. After that, EBL was performed and a 25 nm aluminum (Al) layer was deposited by electron-beam evaporation. Graphene transistors were first measured to verify their electrical conductivity (Fig. S1). The samples were naturally oxidized in the air for more than 3 days to form ~5 nm dense oxidization layer (AlO$_x$). The high quality dense AlO$_x$ was also confirmed by the breakdown measurement (Fig. S2). Al layer serves as not only screening layer, but also self-aligned layer for further SiO$_2$ inductively coupled plasma (ICP) etching. Extra 20 nm SiO$_2$ was etched to form side-wall structure and 13 nm high-k HfO$_2$ as gate dielectric was grown via ALD. Then, monolayer CVD MoS$_2$ film with 2 cm×2 cm size was wet-transferred and patterned on the substrate. Ti/Pd (2 nm/ 35 nm) as source and drain contacts were made on MoS$_2$ to complete the device. The final device has four electrical terminals named source (S), drain (D), 0.34 nm graphene edge gate (G), and the highly p-doped Si substrate back gate (B). By applying the edge of graphene gate a negative voltage to locally deplete the vertical MoS$_2$ channel, the device can be turned off. The device structure and the main fabrication flow of the 0.34 nm gate-length side-wall transistor are shown in Fig. 2a&b.

The devices after the fabrication were characterized, the SEM image with false-colored and TEM image from a representative sample are shown in Fig. 2c and Fig. 2d. For SEM image, purple region contains monolayer graphene/AlO_x/Al/AlO_x/HfO_2 stack. The yellow and blue regions represent the MoS_2 channel and Ti/Pd metal contacts. TEM image shows the profile of the device core region, the layered structure of atomic vertical side-wall MoS_2 channel gated by the edge of graphene can be recognized clearly. The topography MoS_2 film/HfO_2 (~13.8 nm) stack was smooth. To reduce the ungated channel resistance, source electrode was made very close to the edge of graphene (<50 nm, 14 nm in this device). The spatial distribution of aluminum, hafnium, carbon, molybdenum, sulfur and oxygen was observed in the energy dispersive spectrometer (EDS) mapping of the core region (Fig. 2e & Fig. S3), thus confirming the location of the monolayer graphene, HfO_2, Al, AlO_x and monolayer MoS_2 in this device. In the fabrication flow, the CVD graphene and MoS_2 were applied as gate and channel materials, which realizes wafer-scale production (Fig. 2f).

Electrical Measurement and TCAD Simulation

A back gate MoS_2 transistor was first measured (Fig. S4). It indicates that by applying positive back gate voltage (V_{BS}=50 V), the lower extension MoS_2 region on 275 nm SiO_2/ 13 nm HfO_2 can be tuned to relatively high electron carrier density (n^+-type). Therefore, the I_{DS}-V_{GS} transfer characteristic at V_{DS}=-50 mV, -1 V, -2 V and -3 V of this side-wall transistor in Fig. 3a is carried out at V_{BS}=50 V, which demonstrate the feasibility of the graphene edge as the gate of side-wall transistor to turn off the channel. The SS is ~210 mV/dec and ON/OFF current ratio can reach up to 2×10^5. Due to the present of SCEs, the value of DIBL is ~1 V/V. Leakage current from monolayer graphene side-wall gate (I_G) and highly p-doped Si substrate (I_B) are both close to the noise level (10^{-13} A).

The I_{DS}-V_{DS} output curves under different V_{GS} bias at V_{BS}=50 V is shown in Fig. 3b with a linear-like characteristic. By varying V_{BS} from 0 V to 50 V, which can affect the extension of MoS_2 region, the ON state current increases from 10^{-9} A to 10^{-7} A and in I_{DS}-V_{GS} transfer characteristic at V_{DS}=-1.0 V (Fig. 3c). Non-ideal ON state current ~10^{-7} A also proves the ultra-thin gate length due to the present of ungated region in the MoS_2 channel. Besides, the transfer curves slightly left shift under larger V_{BS} because the V_{GS} has to be more negative to deplete the vertical MoS_2 channel owing to the ultra-thin 0.34 nm gate length. Three I_{DS}-V_{GS} transfer curves at V_{DS}=-1.0 V and V_{BS}=50 V from different devices are shown in Fig. 3d, the SS and ON/OFF current ratios of the three devices in the same batch are shown in Fig. 3e. These results demonstrate good uniformity of this 0.34 nm L_g side-wall transistors.

To understand the electrical behaviors and device physics, Sentaurus TCAD was performed based on this experimental side-wall transistor (Fig. 4a). All the parameters in simulation are close to the actual devices. The lower plane of the extension MoS_2 region is 13 nm below the graphene gate plane in

simulation. The comparison of experimental and simulated I_{DS}-V_{GS} curves are shown in Fig. 4b, which have similar trends. The curves negative shifts as V_{DS} becomes more negative, which calls DIBL in small size transistors. The SS in simulation is slightly lower than that in experiment and the ON state current is slighter higher, which is due to the idealized materials and interfaces in the simulation. The electron density and band diagram of ON (V_{GS}-V_{TH}=1.5 V) and OFF (V_{GS}-V_{TH}=-0.5 V) state can demonstrate the ultra-thin 0.34 nm gate control ability. To have a better visibility, the circumstances of MoS_2 channel along the side-wall are shown in Fig. 4c-d and Fig. S6. In the OFF state (Fig. 4c), there is a region of low electron density. The location that graphene edge gate counterparts does not possess the lowest electron density because of the electric field contributing from the 2D planar surface (Fig. S5). Meanwhile, the reduced electron density (Fig. 4c) and E_F (Fig. S6a) shifts downward also verifies the efficient gate control. The extension region is still at high electron density due to the controlling of global back gate. The effective channel length (L_{eff}) is defined as the channel region with electron density $n<n_{threshold}$ ($n_{threshold}$=1.3×10^5 cm^{-2}) (19), therefore the ~13 nm side-wall MoS_2 channel close to the graphene plane can be regarded as effective channel. In the ON state (Fig. 4d & Fig. S6b), the whole MoS_2 channel is at relative high electron density. Therefore, the L_{eff} can be regarded as L_g, which is approaching physical limitation.

As the L_g reaching the physical limitation, the semiconductor thickness is also required to be scaling down to atomic level, in order to minimize the SCEs[20]. Therefore, MoS_2 layer dependent I_{DS}-V_{GS} characteristic of the 0.34 nm gate-length side-wall transistor has also been simulated (Fig. 4e). With the thickness of MoS_2 channel increases from 0.65 nm (1 layer) to 20.8 nm (32 layers), although the ON state current improves for thicker MoS_2, the channel can not be completely depleted at the same V_{GS}-V_{TH}, both the ON/OFF current ratio and SS become undesirable. Besides, atomic layer MoS_2 channel is suitable for scalable production, which is promising for next generation electronics.

Realization of small size transistors is a critical demand. The iterative progresses of gate length as a function of time line is shown in Fig. 4f[14,21-33]. From 2D planar device to 3D FinFET and further GAAFET, the structure of Si transistors gradually changes with better gate control ability. In the meantime, low dimensional materials come into sight, SWCNT gated MoS_2 transistor reached the smallest physical node 1 nm in 2016 and the gate length has been leveling off for 4 years. Our work promotes the side-wall structure and realizes atomic thickness material gating atomic channel. The side-wall structure utilized the naturally thickness direction, and 0.34 nm in this work is the ultimate gate length to date. Wafer-level 2D CVD monolayer materials can also be realized for future logic and circuit integration. This work shed the light of the Moore's law going down to 0.34 nm node.

2D materials provides us opportunities to scale down the electron device to atomic level. TMDCs show good resistance to SCEs and graphene has high electrical conductivity and ultra-thin thickness. In this work, MoS_2 and the edge of graphene act as channel and gate respectively, which realized ultimate 0.34 nm gate length side-wall transistors. The side-wall structure effectively utilizes the nature ultrathin

thickness of graphene and shows the wafer-scale production. The ON/OFF current ratio and SS value could reach 2×10^5 and 210 mV/dec. Further scaling down EOT, improving the MoS_2 film quality and developing ideal contacts to MoS_2 are essential for device performance enhancement. Nevertheless, this work promotes a new insight to scale down the transistors approaching physical limitation and shed light on next generation electronics.

Methods

(1) CVD growth of graphene and MoS_2:

i. Monolayer graphene growth on Cu:

The 3 cm×3 cm CVD monolayer graphene on Cu was bought from Hefei Vigon Material Technology Co., LTD. The monolayer graphene coverage is higher than 99%.

ii. Monolayer MoS_2 growth on Si/SiO_2:

MoO_3 powder (Alfa Aesar 99.95%) contained in a ceramic crucible and adequate sulfur powder (Alfa Aesar, 99.999%) was placed in Zone 2 and at the upstream of furnace in Zone 1, respectively. Cleaned Si/SiO_2 substrate was placed on the crucible. After purge 300 sccm Ar gas 20 min as carrier gas, the growth temperature for the sulfur and MoO_3 precursors was 180 °C and 650 °C, respectively. Continuous monolayer MoS_2 film was synthesized at room pressure with 10 min sulfidation time.

 (2) Wet transfer of graphene and MoS_2:

i. Graphene wet transfer: PMMA was first spin coated on Cu/graphene. Dilute hydrochloric acid (HCl) solution with 20% mass fraction was used to etch supported Cu layer. After Cu was completely etched, graphene/PMMA was transferred to the target sample. Further 85 °C, 60 min annealing can enhance the adhesion between graphene and substrate. PMMA was removed by acetone for more than 30 min soaking.

ii. MoS_2 wet transfer: PMMA was first spin coated on $Si/SiO_2/MoS_2$. Potassium hydroxide (KOH) solution with 3% mass fraction was used to lift off MoS_2/PMMA from the Si/SiO_2 Then, MoS_2/PMMA was transferred to the target sample. Further 85 °C, 60 min annealing can enhance the adhesion between MoS_2 and substrate. PMMA was removed by acetone for more than 30 min soaking.

(3) SEM (scanning electron microscopy) imaging was performed by Quanta FEG 450 field emission scanning electron microscope (FESEM). A 10 kV accelerating voltage was used for imaging the MoS_2 channel and contacted metal.

(4) TEM (transmission electron microscopy) and EDS (energy dispersive spectroscopy) imaging was performed by Themis Z (Thermo Scientific) with a Super-X (Thermo Scientific) EDS system. The system operated at 200 kV accelerating voltage. TEM was carried out with a 23.8 mrad convergence angle electron beam and the collection angle was set to 90-370 mrad. The sample was first deposited carbon by electron-beam and Pt by ion-beam to protect the surface from the damage of the ion-beam.

(5) Electrical measurements were performed under vacuum ($\sim 10^{-5}$ mbar) in Lakeshore vacuum probe station with Agilent Technologies B1500A Semiconductor Device Analyzer.

Declarations

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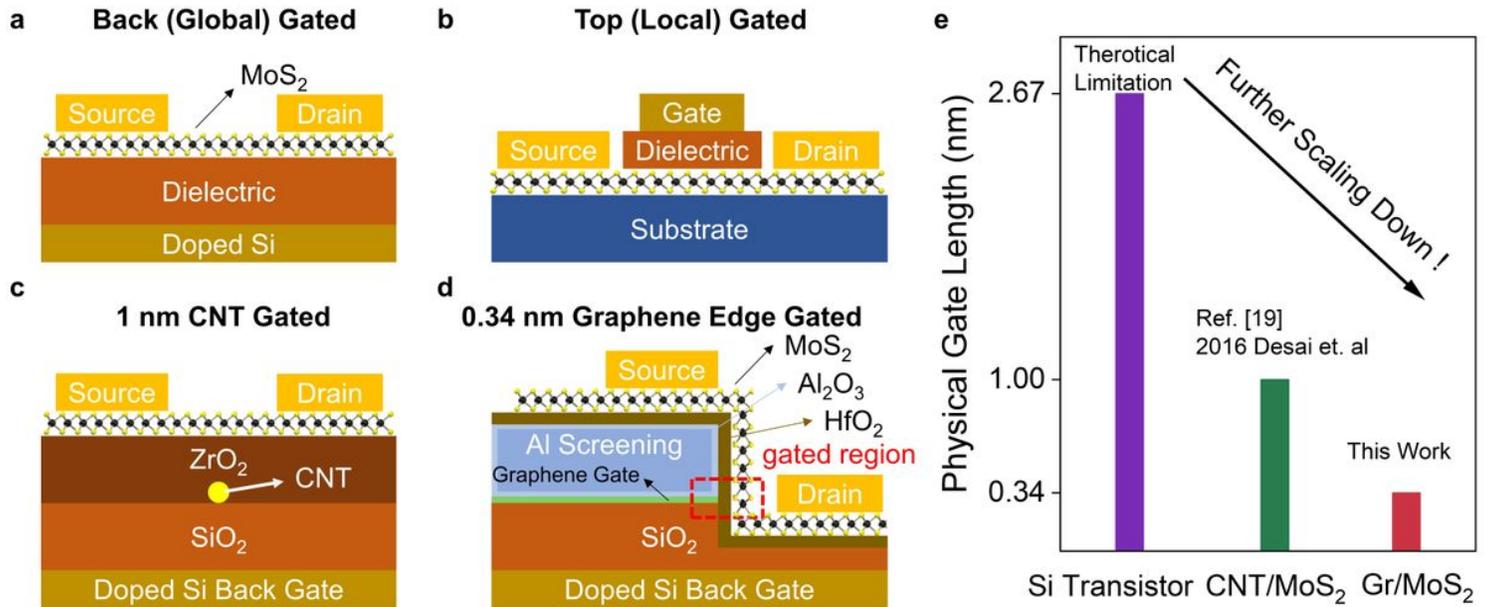
Figures

Figure 1

Comparison of the 0.34 nm Lg side-wall transistor with other typical structure transistors. (a) Back (global) gate structure. (b) Top gate structure. (c) 1 nm SWCNT buried gate structure19. (d) Our side-wall transistor with the edge of graphene as gate electrode. (e) The physical limitation of gate length under different gate and channel conditions.
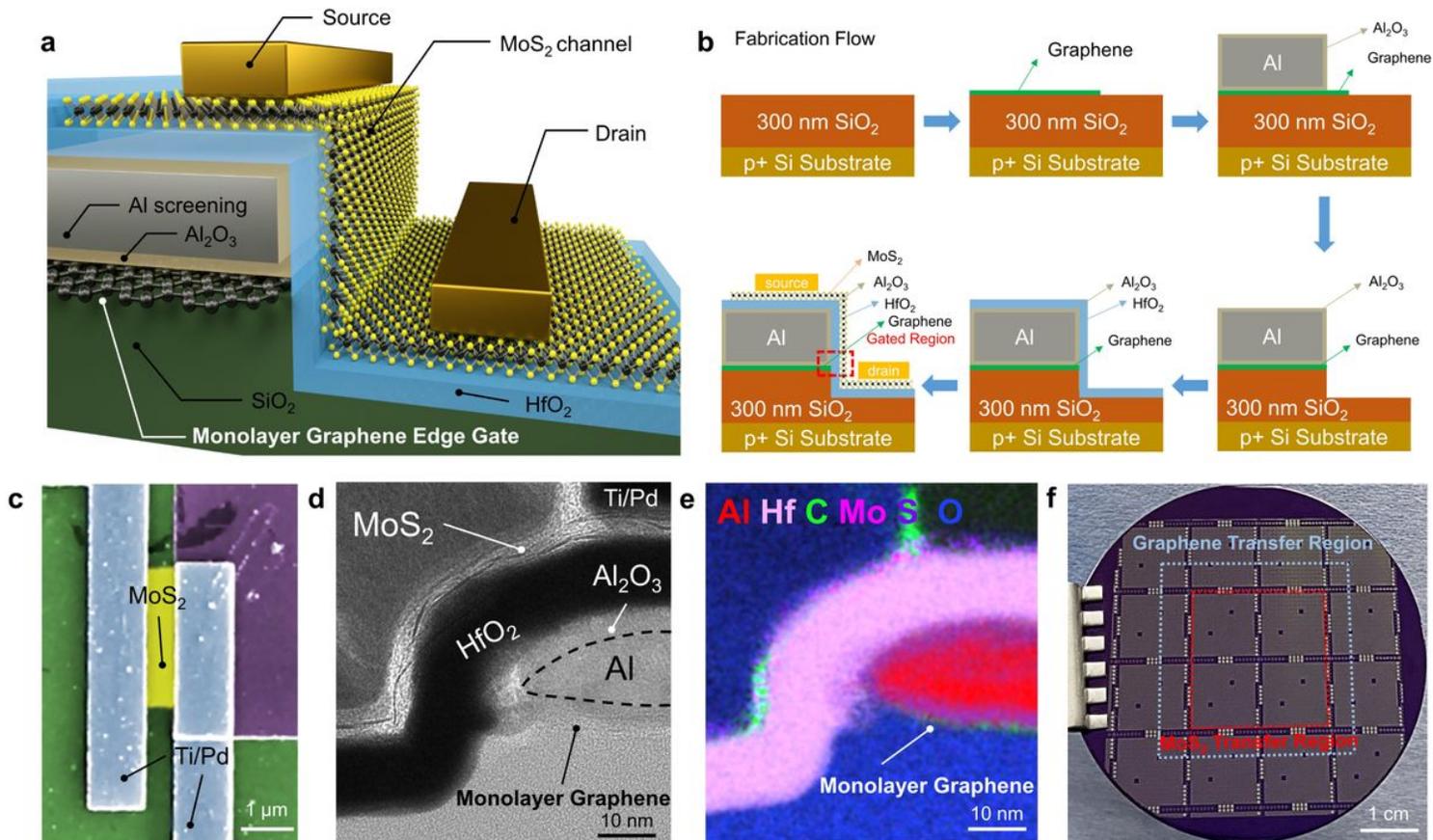
Figure 2

0.34 nm gate-length side-wall monolayer MoS2 transistor device structure and characterization. (a) Schematic of side-wall gate structure with a monolayer MoS2 channel and 0.34 nm monolayer graphene edge gate. (b) Process flow for the device fabrication. (c) False-colored SEM image of the device showing the HfO2 gate dielectric (green), Al screening layer (purple), monolayer MoS2 channel (yellow), and the Ti/Pd source and drain electrodes (blue). (d) Cross-sectional TEM image of a representative sample showing the monolayer graphene edge gate, HfO2 gate dielectric, Al screening layer and monolayer MoS2 channel. (e) EDS mapping showing the spatial distribution of aluminum, hafnium, carbon, molybdenum, sulfur and oxygen in the device region, confirming the location of the Al screening layer, HfO2 dielectric, monolayer graphene, and MoS2 film. (f) Optical image of a 2-inch wafer 0.34 nm Lg side-wall transistor array.
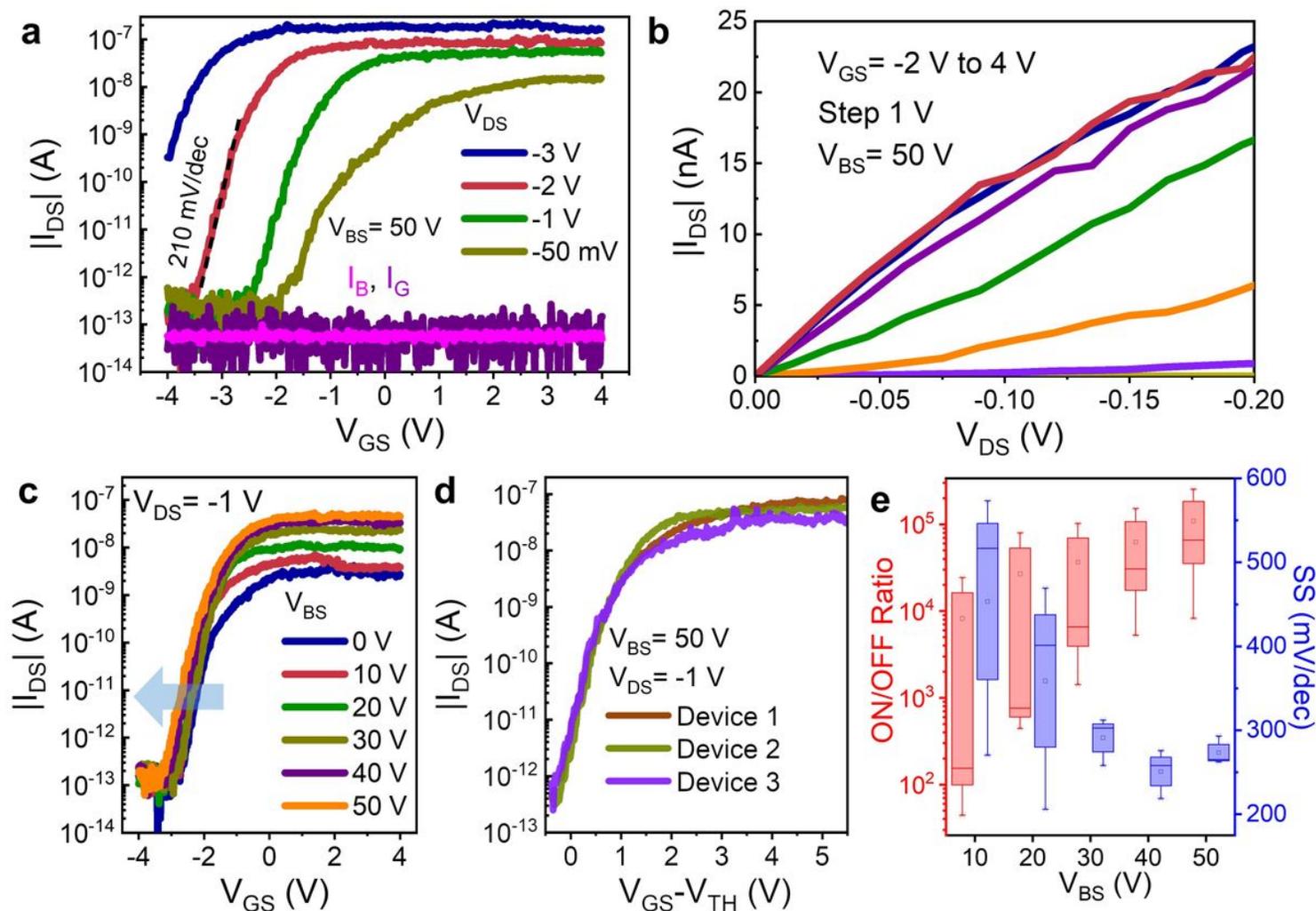
Figure 3

Electrical characterization. (a) IDS-VGS characteristics at VBS = 50 V and VDS = -50 mV, -1 V, -2 V, -3 V. The leakage current from back gate and graphene edge gate are also shown. (b) IDS-VDS characteristics at VBS= 50 V and VGS varies from -2 V to 4 V at small VDS value. (c) IDS-VGS characteristics at VDS = -1 V and varying VBS illustrating the effect of back-gate bias on the extension region resistance, on-state current, and device characteristics. (d) IDS-VGS characteristics of three devices at VBS= 50 V and VDS=-1 V. (e) The variation of devices in one batch. The data are extracted from IDS-VGS curve at VDS=-1 V.
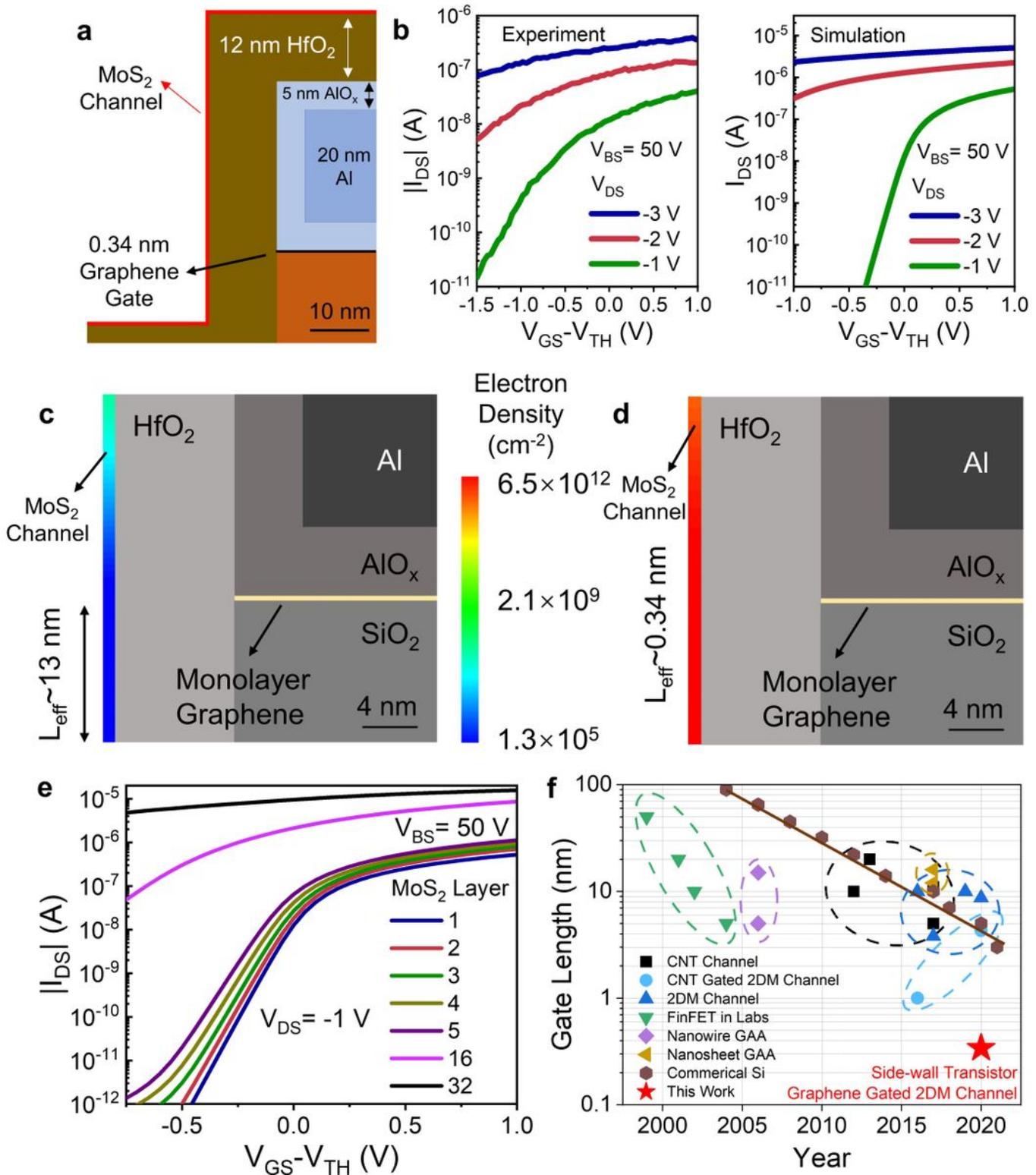
Figure 4

TCAD simulation results and benchmark. (a) Simulated structure. (b) The comparison between experimental and simulated IDS-VGS curve. The VTH values are extracted at VDS=-1 V. The electron density of MoS2 channel along side-wall at the OFF state (c) and ON state (d). The graphene edge gate can effectively turn off the device due to the 2D planar characteristic. The effective channel length (Leff) is ~13 nm in OFF state and 0.34 nm (≈Lg) in ON state. (e) The MoS2 layer dependent IDS-VGS curve in

this simulated side-wall transistor. Monolayer MoS2 channel has the lower SS value comparing to that of thicker MoS2 and suitable ON/OFF current ratio. (f) A time scale evolution of Lg. This work is marked by the red star, which promotes the Lg scales down to atomic limit.

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