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Research Article

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A Hybrid Design Technique to Improve the Structure and Performance of Microstrip Components

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Abstract: A hybrid approach to improving the structures of microstrip devices is presented in this study. The proposed technique includes a combination of simple series inductor (L) and capacitor (C) circuits with microstrip-based structures and transmission lines. In this method, the LC circuits are replaced with those parts of the microstrip components that need to act like a bandpass filter. Not only does this simple modification lead to a 100% size reduction, an infinite number of harmonics suppression and high frequency selectivity theoretically, but it will also result in a noticeable performance practically compared to the conventional arrangements of microstrip lines. To show the capability of the proposed method, two quarter-wavelength branches of a Wilkinson Power Divider (WPD) have been rectified and implemented using the LC circuit, which is called LC branches in this paper. Extreme size reduction and harmonic suppression in this implementation of the Filtering Power Divider (FPD) can be considered two important outcomes of this design technique. Furthermore, by tuning the LC circuit, the arbitrary numbers of unwanted harmonics can be blocked, and the operating frequency, the stopband bandwidth and the operating bandwidth could be opted optionally. The experimental result has verified the theoretical and simulated results of the proposed technique. The results clearly demonstrate the considerable potential of this technique to improve the design process of the microstrip devices with desirable specifications.
Keywords: Filtering power divider (FPD), Harmonic suppression, Microstrip components, Size reduction.

1. Introduction

As modern communication systems grow rapidly, the demands for components with low energy loss, compact size and filtering response have been increased. Furthermore, wireless components should be integrated for multiple function ability in embedded systems. For example, integrating filter with power divider can be result in compact size and low energy loss in the microwave components. Besides, the microstrip passive devices, such as power dividers and couplers are widely used in power amplifier applications. Therefore, harmonic suppression and high performance power divider lead to higher efficiency resulting in more energy saving in wireless devices. [1, 2]

Power dividers play an important role in modern wireless communication systems [3]. Wilkinson power divider (WPD) is one of the most popular types in dividers. WPD is first proposed by Ernest J. Wilkinson in 1960 [4]. The WPD is widely used in modern communication circuit devices, such as Doherty power amplifiers [5], balanced power amplifiers [6, 7], push-pull power amplifiers [8], antenna feed networks [9], phase shifters [10] and RF/microwave frontend systems [11].

One of the disadvantages of the typical WPD is that the spurious harmonic suppression can pass through the power divider paths and decrease the performance of the circuit. The other disadvantage of WPD is the large size of about approximately 0.0156 λ^2 surface area. Recently, several approaches have been performed to overcome these problems. For example, coupled lines [12], open stubs [13], T-shaped and Π-shaped resonators [14], and embedded filters [15].

Open subs are usually used in the main quarter wavelength branches of the divider as studied in [13, 16] to reduce the size and suppress a few harmonics. Open stubs can also be used at the input port to improve the input return loss parameter [17-19]. Applying open stubs technique causes to provide desirable transmission zeros at the frequency response, which can suppress the desired harmonics and also reduces the size [20]. However, the disadvantage of this method is that each open stub provides a single transmission zero, so for obtaining a wide stopband several open stubs should be applied. Therefore, high numbers of open subs may increase the overall size and also make the design complicated.

Another technique, which has been used in several approaches, is using coupled lines [21, 22]. Applying coupled lines in the divider structure can produce several transmission zeros and also can widen the operating bandwidth of the amplifier. In [21], coupled lines are used in a WPD to obtained wideband and harmonic suppression. However, this WPD has a rather large size compared to the conventional divider. Parallel coupled lines are used in [22] to present an FPD with filtering response. The frequency response of this divider is wideband with filtering shape, but the size reduction has not been achieved in this work.
Stepped impedance resonators are also used for improving the performances of the dividers [23, 24]. A dual-band filtering divider is presented in [23]. The Stepped impedance resonators are used in this divider to provide filtering response in both operating frequencies, but the overall size of the divider is quietly large. Stepped impedance resonators are applied in [24] for harmonic suppression in WPD. However, the obtained suppressing bandwidth is narrow and the designed WPD has a large size.
Microstrip filters can suppress the desired frequency band; therefore, they can be embedded in the divider to make filtering divider [25]. Substrate integrated waveguide (SIW) with embedded filters are used to present a filtering power divider in [15]. Multiple isolation resistors technique is presented in this work to improve the divider isolation. However, the overall size of the divider is very larger than the conventional divider.
Lumped elements have also been used in divider structures to improve the performances of the divider [26, 27]. In [26] parallel inductor and capacitor are used between output ports to achieve FPD. Finally, equivalent transmission lines are used instead of the lumped elements, in this work. A filtering response has been achieved in this work, but the suppression bandwidth is not wide enough. Two capacitors are exploited in parallel with the main branches to design a broadband WPD in [27].
In many approaches, the mentioned techniques are combined, for instance, in [28] the stepped impedance and open stubs are combined. In [29] stepped impedance and open stubs and coupled lines are used to design filtering divider. In addition, in [30], lumped elements, coupled lines, and open stubs techniques are gathered to design a harmonic suppressed divider with a wide operating band. Good suppression band and the wide operating band is obtained in this work, however, the overall size of the divider is rather large.
All of the mentioned techniques result in limited improvement in harmonic suppression and size reduction of the amplifiers. Because, the circuit will be very complicated and the divider performances will be decreased when high size reduction and harmonic suppression are desired. In this paper, a very simple and novel structure is proposed using LC branches in both main paths of the divider. By using this new structure theoretically, 100% size reduction and an infinite number of harmonics suppression can be achieved in the divider. In practice, it is impossible to have 100% size reduction and the infinite number of harmonics suppression; but, the extreme values of size reduction and excellent numbers of harmonic suppression will be obtained which has not been achieved in any divider so far.

The paper organization is described as follows. In Section II (Typical Structure in Microstrip Components) typical WPD is described. In Section III (Proposed Structure) it is explained that how the proposed LC branches structure is applied in a typical WPD. The describing equations of the proposed divider are extracted in Section IV (Analyses of the Proposed FPD). In Sections V (Design Examples at 2.4 GHz) and VI (Design Examples at 0.8 GHz), two design examples at 2.4 GHz and two design examples at 0.8 GHz are presented to verify the performance of the proposed structure in different frequencies and different dimensions. In section VII (Results) the analytical and simulation results of the proposed structure are verified by experimental results. Finally, in the last section VIII (Conclusions) summary of the results and conclusions are described.

2. Typical Structure in Microstrip Components

To describe the structure of a conventional microstrip device, a typical WPD is investigated in this section. In such devices, quarter-wavelength branches are responsible for suppressing the unwanted harmonics and passing the main one. Fig. 1 illustrates a classic WPD with two quarter-wavelength branches and a resistor between output ports. One of the most challenging drawbacks with such structures is the large size of the device due to utilizing the large quarter-wavelength branches being not desirable in modern wireless components. Another disadvantage, which can be mentioned for this type of design, is to suffer from the existence of spurious harmonics, because the typical quarter-wavelength branches cannot provide suppression band for the divider. Although the overall size of WPDs are totally determined based on WPD layout structure, the layout of dividers can be selected arbitrarily. Generally, two common forms of the WPD have been utilized in the design of WPDs, namely squared shape and circular shape, depicted in Fig. 2 (a) and Fig.2 (b), respectively. As you can see in Fig. 2 (a), the overall area of the square shape WPD, is $0.125\ \lambda \times 0.125\ \lambda$, which is equal to $0.0156\ \lambda^2$ while the overall size for circular one is $0.0198\ \lambda^2$ indicating this point that circular type of WPD is typically larger than the squared shape one. Regardless of this difference, the magnitude of WPD and many microstrip components significantly depend on their quarter-wavelength branches, such as branch-line couplers, rat-race couplers and several types of discrete power amplifiers. In addition, the proposed method can be applied to the

transmission lines with any electrical length, which can be significantly effective in performance improvement of the microwave components.

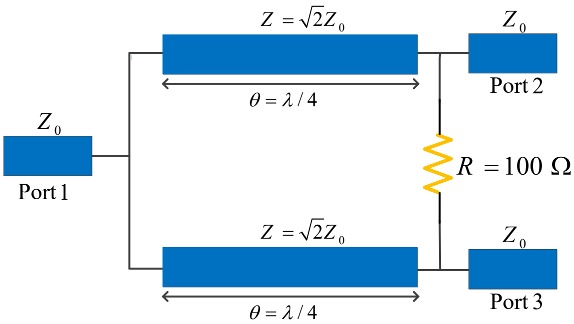


Figure 1. Arrangement of microstrip transmission lines to design a typical WPD

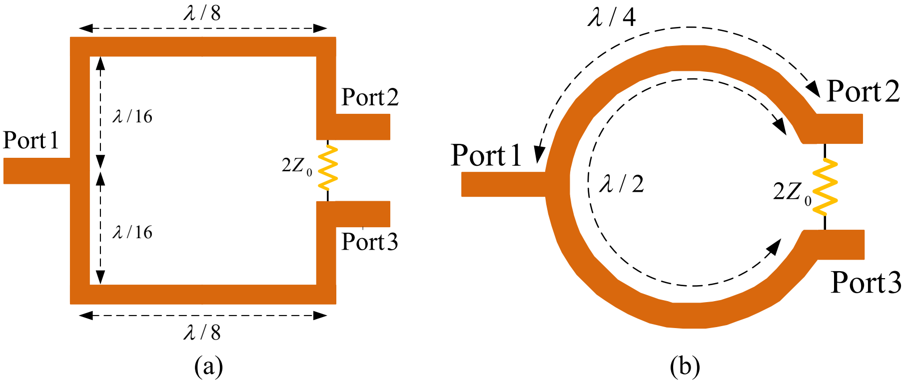


Figure 2. Arrangements of microstrip transmission lines in classic WPD layout; (a) squared-shaped WPD layout; (b) circular-shaped WPD layout.

3. Proposed Structure

As is mentioned, the typical FPD suffers from large size and harmonics existence. Therefore, by modifying those parts of the microstrip devices that are more responsible in increasing the magnitude, not only will the size of components made by this technology be far more compact, but it can also lead to increasing the efficiency. Overall, to reach this objective, some important parameters like selectivity and stopping the unwanted harmonics should be considered. A novel solution to reshape and redesign the classic structures has been presented following.

3.1. Proposed LC Branch Lines

With a modification based on replacement of LC branches with those parts of the components, which play the role of bandpasss filters, considerable improvements are obtained in designing of the new generation of microwave devices. Fig. 3 demonstrates the proposed hybrid approach using microstrip lines and LC branches in a integrated device. 3. As is observed in Fig. 3, microstrip branch lines of the conventional WPD are replaced with the proposed LC branch lines. The LC branch lines include a resonance capacitor (C_0), a resonance inductor (L_0), and a miniaturizing inductor (L_m). The resonance capacitor and inductor, which form a series LC circuit, should be tuned at the desired operating frequency (f_0). The series LC circuit will be shorted at f_0 while it will be opened at other frequencies, which results in the bandpass response of the divider. Therefore, the LC branch structure can be used to reduce the desired harmonics.

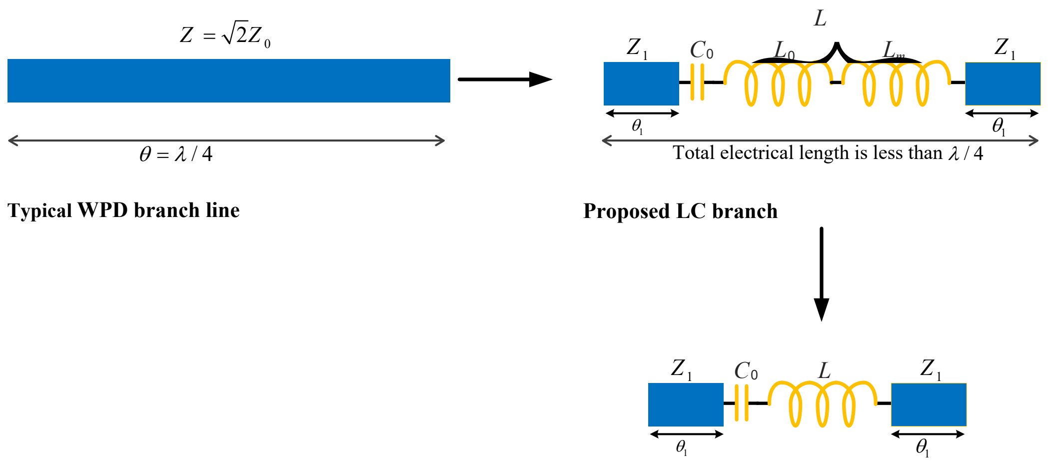


Figure 3. The main idea of replacing the microstrip lines with the proposed LC branches

Furthermore, the size of each microstrip branch line is significantly decreased from a considerable area to the small transmission line, as will be discussed in the next sections. The miniaturizing inductor results in reducing the LC branch length. The inductances of L_0 and L_m are in series and can be considered as inductance of L in practice. After applying the proposed LC branches, a new structure will be obtained for the FPD. The proposed structure of FPD with the presented LC branches is depicted in Fig. 4.

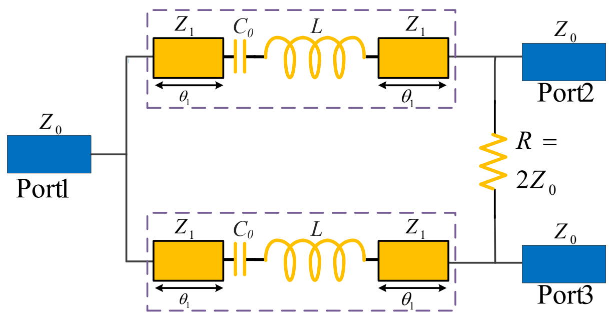


Figure 4. The proposed structure of FPD with the presented LC branches

4. Analyses of the proposed FPD

The structure of the proposed FPD is analyzed using the ABCD matrix. The ABCD matrix of the proposed LC branch has to be equaled to the ABCD matrix of a conventional quarter wavelength branch. Therefore, the obtained equation is written in (1)

$$\mathrm{M}_1 \times \mathrm{M}_{\mathrm{LCB}} \times \mathrm{M}_1 = \mathrm{M}_{\mathrm{QWL}} \qquad (1)$$

where, in M_1, M_{LCB}, and M_{QWL} are ABCD matrices of the transmission line (Z_1, θ_1), LC branch, and quarter wavelength line ($\sqrt{2}Z_0$, $\lambda/4$), respectively. In addition, the values of M_1, M_{LCB}, and M_{QWL} matrices are defined in (2).

$$\mathrm{M}_1 = \begin{bmatrix} \cos(\theta_1) & jZ_1\sin(\theta_1) \\ jY_1\sin(\theta_1) & \cos(\theta_1) \end{bmatrix},$$

$$\mathrm{M}_{\mathrm{LCB}} = \begin{bmatrix} 1 & jL_m\omega + jL_0\omega - j/(C_0\omega) \\ 0 & 1 \end{bmatrix}, \qquad (2)$$

$$\mathrm{M}_{\mathrm{QWL}} = \begin{bmatrix} 0 & j\sqrt{2}Z_0 \\ j/\sqrt{2}Z_0 & 0 \end{bmatrix}$$

As mentioned before, the series L_0C_0 is tuned at the main frequency (f_0), which is shorted at the main frequency. Hence, if it is assumed to perform the analysis in the main frequency, the LC branch matrix can be simplified as written in (3).

$$\mathrm{M_{LCB}} = \begin{bmatrix} 1 & jL_m\omega \\ 0 & 1 \end{bmatrix} \quad (3)$$

By solving equation (1), three independent equations are obtained as follows

$$2Z_1 = L_m\omega_0 \tan\left(2\theta_1\right) \quad (4)$$

$$\sqrt{2} = \frac{Z_1}{Z_0}\sin\left(2\theta_1\right) + \frac{L_m\omega_0}{2Z_0} + \frac{L_m\omega_0}{2Z_0}\cos\left(2\theta_1\right) \quad (5)$$

$$\frac{1}{\sqrt{2}} = \frac{Z_0}{Z_1}\sin\left(2\theta_1\right) - \frac{Z_0L_m\omega_0}{2Z_1^2} + \frac{Z_0L_m\omega_0}{2Z_1^2}\cos\left(2\theta_1\right) \quad (6)$$

By comparing equations (5) and (6), the following equation is achieved.

$$2 - \frac{Z_1^2}{Z_0^2} = \frac{\sqrt{2}L_m\omega_0}{Z_0} \quad (7)$$

By solving equation (7), which is a second-order equation, the normalized value of Z_1 can be calculated as written in (8).

$$\frac{Z_1}{Z_0} = \frac{-\sqrt{2} + \sqrt{2 + \tan\left(2\theta_1\right)^2}}{\tan\left(2\theta\right)} \quad (8)$$

Fig. 5 demonstrates the proposed approach, including the prototype of the microstrip device- a conventional WPD here- and the suggested method to solve the equations in order to obtain circuit parameters. As it can be seen in this figure, in the first stage, the prototype of the understudied component to be compacted is indicated. In the second stage, the values of the key parameters for the device, such as the amount of size reduction (SR%), operating frequency (f) and operating Band Width (BW) are arbitrarily determined. Next, θ_1 is computed based on the selected SR% in the previous stage. In the third stage, $Z_1$is reached using equation (8), which the calculated circuit values in the third stage are listed in Table 1at the operating frequency of 2.4 GHz and 0.8 GHz. As is observed in equation (8), the value of Z1 is independent of the operating frequency. Although in the second and third stages, the operating frequency is utilized in no computations, in forth one, it is used with Z_1 and $\theta_1$to determine the value of L_m. In other words, the L_m depends on the operating frequency. By adding $L_0$to and L_m, the total value of L is achievable in the fifth stage. The values of L_0 and C_0 are achieved based on values of Q being available in Table 2 and Table 3 at the operating frequency of 2.4 GHz and 0.8 GHz. Also the value of Q is obtained through BW, which will be more discussed at the next Sections. Finally, the new proposed divider with desirable parameters based on (θ1, Z1, C0, and L) can be achieved.

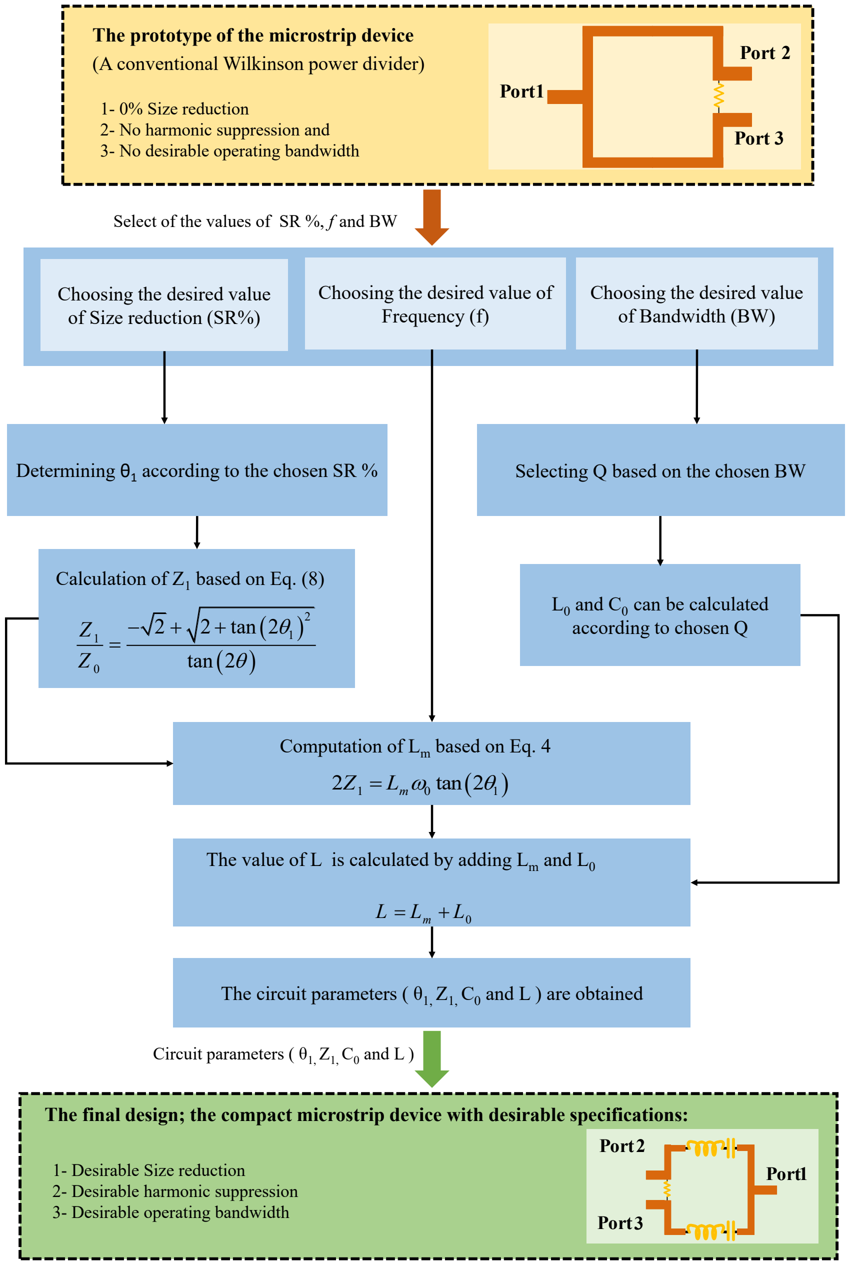


Figure 5. The process of redesign, solving the equations and improvement of a WPD based on the proposed technique. First, the conventional WPD with 0% size reduction, no harmonic suppression and no bandwidth tuning ability is considered. The desire value of SR%, frequency and bandwidth are then assumed arbitrarily. Next, with the use of the proposed analyze flowchart the equations are solved and the desired circuit parameters (θ1, Z1, C0, and L) are achieved. By applying these circuit parameters and the proposed structure to the typical WPD, the new reshaped compact divider with desirable SR%, great harmonic suppression, and desirable operating bandwidth is obtained.

Table 1. The calculated circuit values of the divider for desired values of the size reduction

Total Branch Electrical Length $2\theta_1$ (˚)	θ_1 (˚)	Z_1 (Ω)	L_m (nH) @2.4 GHz	L_m (nH) @0.8 GHz	Maximum Size (λ_g^2) Reduction of Divider (%)
90	45	70.7	0	0	0
80	40	59.3	1.4	4.2	21
70	35	49.5	2.4	7.2	39.5
60	30	40.8	3.1	9.4	55.5
50	25	33.0	3.7	11	69.1
40	20	25.7	4.0	12.2	80.2
30	15	18.9	4.3	13	88.9
20	10	12.4	4.5	13.6	95
10	5	6.2	4.6	14	98.7

The calculated values of divider maximum size reduction versus total branch electrical length and also versus the value of Z_1 (Ω) are shown in Fig. 6(a) and Fig. 6 (b).Moreover, the calculated values of Z_1 (Ω) and L_m (nH) versus total branch electrical length are illustrated in Figs. 6(c) and (d). The plots in Fig. 6are calculated at 2.4 GHz frequency. As seen in this Figure, any value of size reduction can be achieved theoretically using the proposed LC branches.

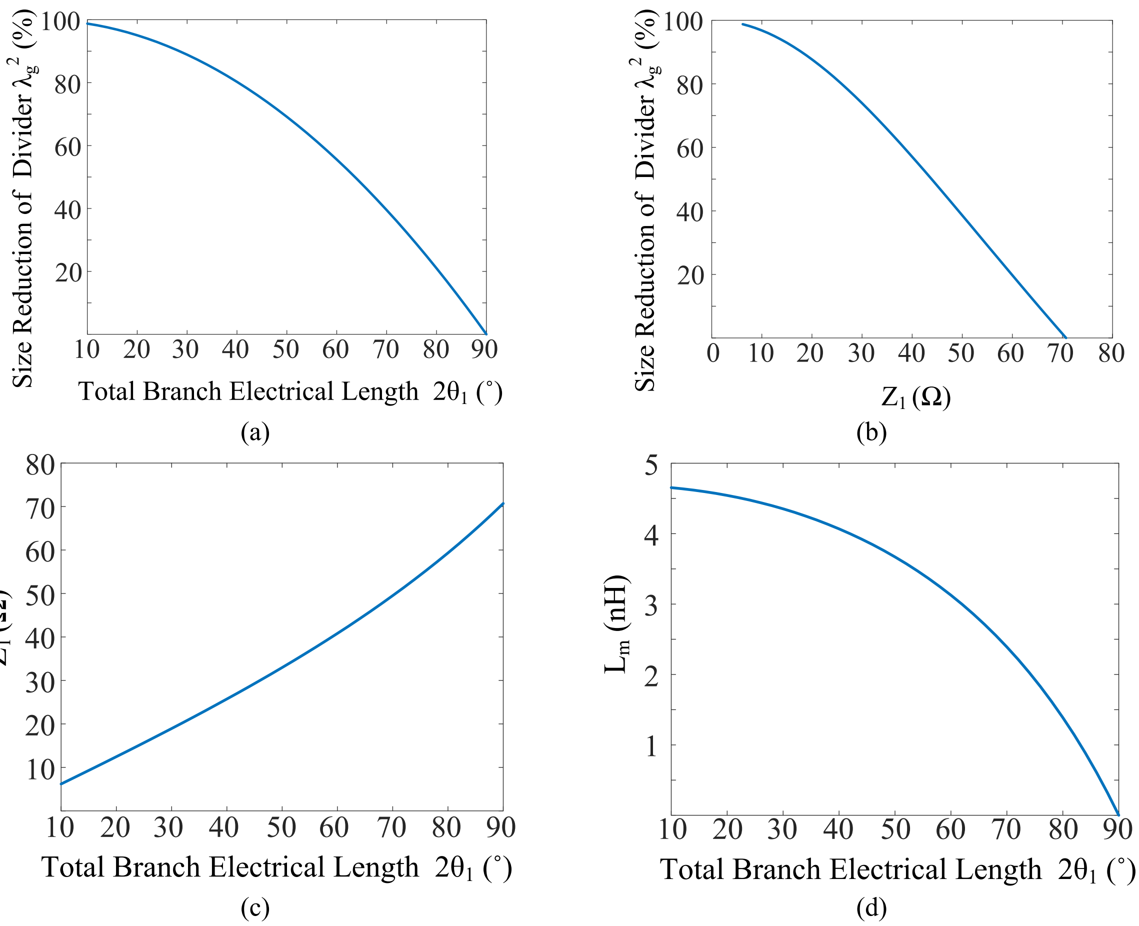


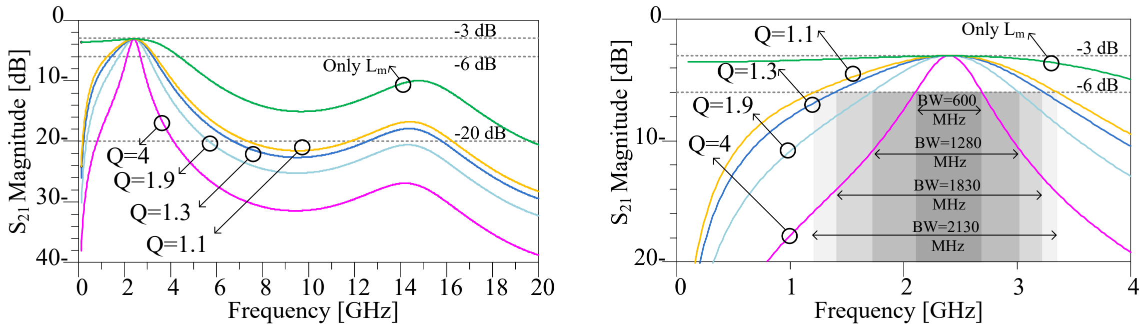
Figure 6. The calculated values of (a) divider maximum size reduction versus total branch electrical length and (b) value of Z_1 (Ω). (c) The calculated values of Z_1 (Ω) and (d) L_m (nH) versus total branch electrical length.

In the final design, in addition to L_m, resonant inductor (L_0) and capacitor (C_0) will be applied to form the LC branch. The series LC circuit should be tuned at the desired operating frequency. For a better explanation of the design procedures, four design examples are introduced, which two of them are at 2.4 GHz and two of them are at 0.8 GHz. These design examples are fully described at the next section.

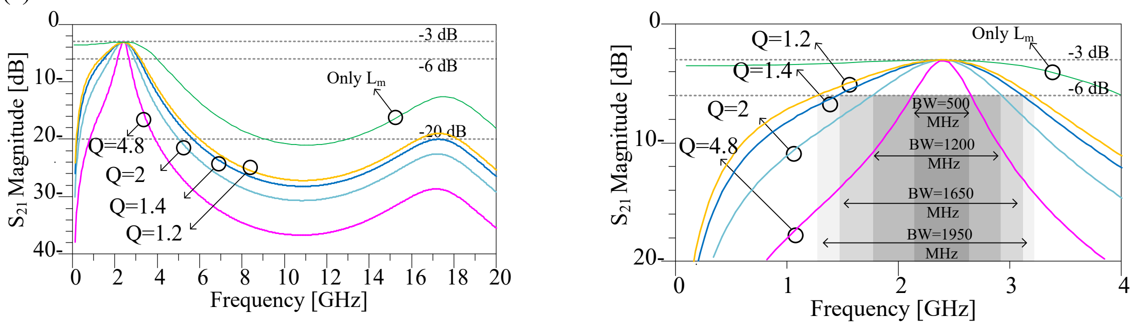
5. Design Examples at 2.4 GHz

To verify the analytical results, two design examples at the operating frequency of 2.4 GHz are introduced in this section. According to Table1, the size reduction values of 55.5% and 69.1% are chosen for the first and second design examples at 2.4 GHz. From Table 1, the width (Z_1) and length (θ_1) dimensions of LC branches

transmission line are 40.8 Ω and 30˚ for 55.5% size reduction, while they are 33 Ω and 25˚ for 69.1% size reduction, respectively. The values of L_m are calculated equal to 3.1 nH and 3.7 nH for55.5% and 69.1% size reduction values, respectively. In the next step, the series L_0C_0 circuit should be tuned at the operating frequency. However, the quality factor (Q) of the series L_0C_0circuit can be tuned by changing the L_0 and C_0 values. The effects of the series L_0C_0 circuit different quality factors on the simulated frequency responses of the presented design examples are shown in Fig. 7. As can be seen, by increasing the quality factor, the bandwidth will be decreased and the stopband will be increased. In other words by increasing the quality factor more harmonic suppression can be achieved. Therefore, the arbitrary bandwidth can be achieved by tuning the quality factor in LC branches. In the case, indicated with "only L_m" in Fig. 7, the L_m is only considered in the LC branch, while the resonant inductor (L_0) and capacitor (C_0) are not applied. This situation can also be assumed as a series resonant circuit with a small quality factor.



(a)



(b)

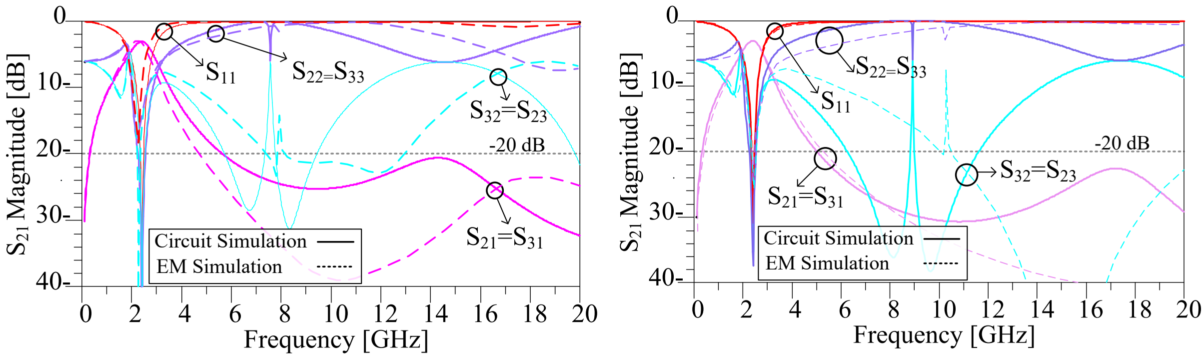
Figure 7. Effects of the series LC circuit different quality factors on the simulated frequency responses of the presented design example. (a) First design example with theoretical 55.5% size reduction and (b) second design example with theoretical 69.1% size reduction, both at 2.4 GHz operating frequency.

Different values of L_0 and C_0 combinations are considered at 2.4 GHz operating frequency in Table 2. Then, the corresponding values of quality factors and operating bandwidths are extracted in Table. 2.

Table 2. Values of L_0, C_0, quality factor and operating bandwidth at 2.4 GHz operation

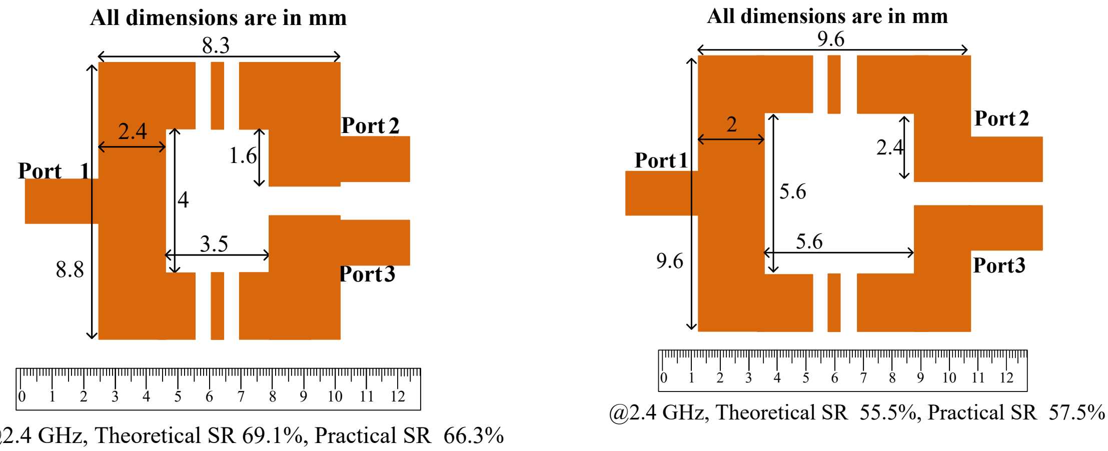
C_0 (pF) 55.5% SR	**L_0 (nH) 55.5% SR**	**L_m (nH) 55.5% SR**	**L (nH) 55.5% SR**	**BW (MHz) 55.5% SR**	**Q 55.5% SR**
0.2	22	3.1	25.1	600	4
0.5	8.8	3.1	11.9	1280	1.9
0.8	5.5	3.1	8.6	1830	1.3
1	4.4	3.1	7.5	2130	1.1
C_0 (pF) 69.1% SR	**L_0 (nH) 69.1% SR**	**L_m (nH) 69.1% SR**	**L (nH) 69.1% SR**	**BW (MHz) 69.1% SR**	**Q 69.1% SR**
0.2	22	3.7	25.7	500	4.8
0.5	8.8	3.7	12.5	1200	2
0.8	5.5	3.7	9.2	1650	1.4
1	4.4	3.7	8.1	1950	1.2

The frequency responses of the prototype dividers at 2.4 GHz for the first and second design examples are depicted in Fig 8. The circuit simulation and electromagnetic (EM) simulation are compared in this Figure. The Layouts of the prototype dividers at 2.4 GHz for the first and second design examples are depicted in Fig. 9. According to this Figure, the total area size of the first and second design examples are 9.6 mm × 9.6 mm (0.1 λ_g × 0.1 λ_g) and 8.3 mm × 8.8 mm (0.091 λ_g × 0.09 6λ_g), respectively. To calculate the practical size reduction of the designed examples, a layout of the conventional squared shaped WPD at 2.4 GHz is designed, which the overall size of the conventional divider is obtained as 15.6 mm × 13.9 mm (0.17 λ_g × 0.15 λ_g). Therefore, the practical size reduction of57.5% and66.3% are achieved for the first and second design examples. The cause of difference between theoretical and practical size reduction is that some areas should be considered for lumped elements in practice. Also folding and bending the microstrip lines change the theoretical values.



(a) (b)

Figure 8. Frequency responses of the prototype dividers at 2.4 GHz for the (a) first design example with theoretical55.5% size reduction and (b) second design example with theoretical 69.1% size reduction.

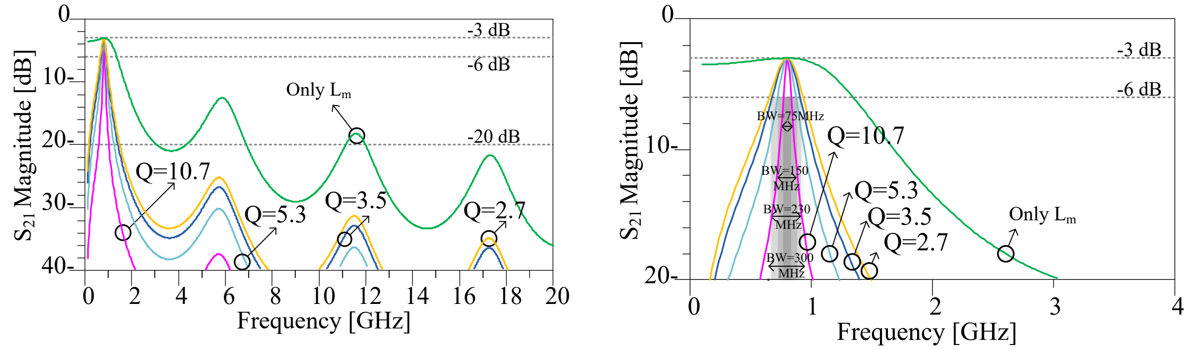


(a) (b)

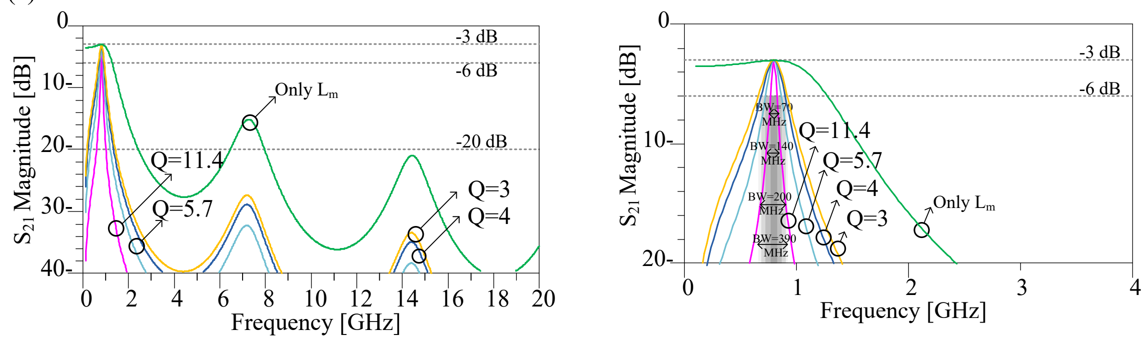
Figure 9. Layouts of the prototype dividers at 2.4 GHz for the (a) first design example with theoretical 55.5% size reduction and (b) second design example with theoretical 69.1% size reduction (All dimensions are in mm).

6. Design Examples at 0.8 GHz

Two design examples at the operating frequency of 0.8 GHz (third and fourth design examples) are introduced in this section to verify the analytical results at different frequencies. According to Table1, the size reduction values of 69.1% and 80.2% are chosen for the third and fourth design examples at 0.8 GHz. The values of L_m should be considered equal to 8.8 nH and 9.8 nH for 69.1% and 80.2% size reduction values, respectively. The next steps of the design procedures are done similarly to the first and second design examples. The effects of the series L_0C_0 circuit different quality factors on the simulated frequency responses of the presented design examples are shown in Fig. 10. As can be seen, by increasing the quality factor, the bandwidth will be decreased and the stopband will be increased.



(a)



(b)

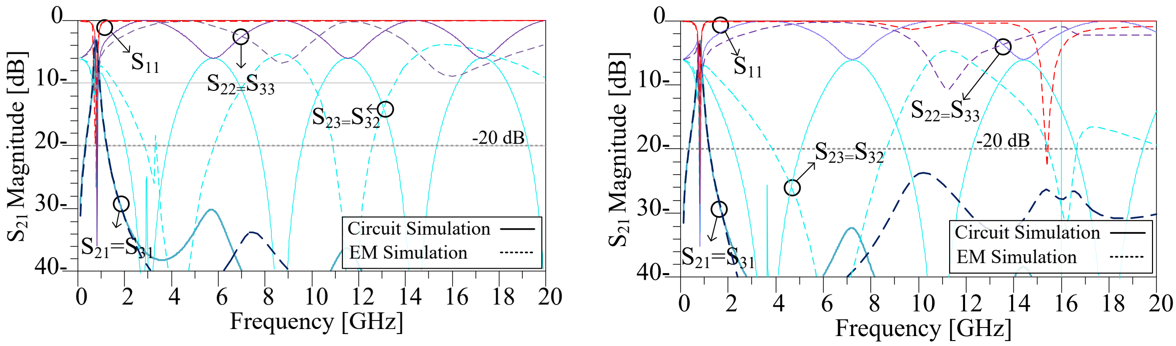
Figure 10. Effects of the series LC circuit different quality factors on the simulated frequency responses of the presented design example. (a) Third design example with theoretical 69.1% size reduction and (b) fourth design example with theoretical 80.2% size reduction, both at 0.8 GHz operating frequency.

Different values of L_0 and C_0 combinations are considered for 0.8 GHz operating frequency in Table 3. Then, the corresponding values of quality factors and operating bandwidths are extracted in Table. 3.

Table 3. Values of L_0, C_0, quality factor and operating bandwidth at 0.8 GHz operation

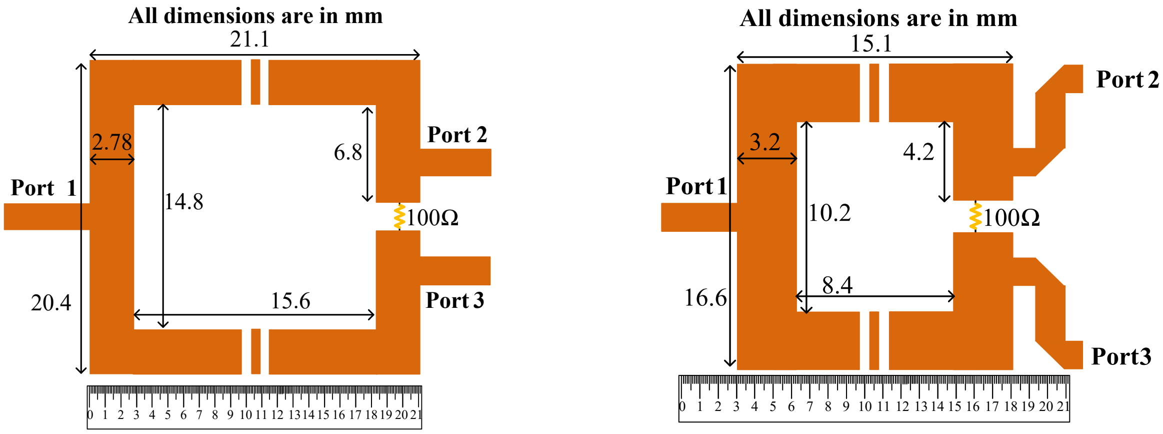
C_0 (pF) 69.1% SR	**L_0 (nH) 69.1% SR**	**L_m (nH) 69.1% SR**	**L (nH) 69.1% SR**	**BW (MHz) 69.1% SR**	**Q 69.1% SR**
0.2	198	11	209	75	10.7
0.5	79.2	11	90.2	150	5.3
0.8	49.5	11	60.5	230	3.5
1	39.6	11	50.6	300	2.7
C_0 (pF) 80.2% SR	**L_0 (nH) 80.2% SR**	**L_m (nH) 80.2% SR**	**L (nH) 80.2% SR**	**BW (MHz) 80.2% SR**	**Q 80.2% SR**
0.2	198	12.2	210.2	70	11.4
0.5	79.2	12.2	91.4	140	5.7
0.8	49.5	12.2	61.7	200	4
1	39.6	12.2	51.8	260	3

The frequency responses of the prototype dividers at 0.8 GHz for the third and fourth design examples are depicted in Fig 11. The circuit simulation and electromagnetic (EM) simulation are compared in this Figure. The Layouts of the prototype dividers at 0.8 GHz for the first and second design examples are depicted in Fig. 12. According to this Figure, the total area size of the third and fourth design examples are 20.4 mm × 21.1 mm ($0.075\ \lambda_g \times 0.077\ \lambda_g$) and 16.6 mm × 15.1 mm ($0.060\ \lambda_g \times 0.055\ \lambda_g$), respectively. To calculate the practical size reduction of the designed examples, a layout of the conventional squared shaped WPD at 0.8 GHz is designed, which the overall size of the conventional divider is obtained as 38.2 mm × 38.2 mm ($0.14\ \lambda_g \times 0.14\ \lambda_g$). Therefore, the practical size reduction of 70.5% and 82.8% are achieved for the third and fourth design examples.



(a) (b)

Figure 11. Layouts of the prototype FPDs at 0.8 GHz for the (a) third design example with theoretical 69.1 % size reduction and (b) fourth design example with theoretical 80.2% size reduction



@0.8 GHz, Theoretical SR 69.1%, Practical SR70.5%

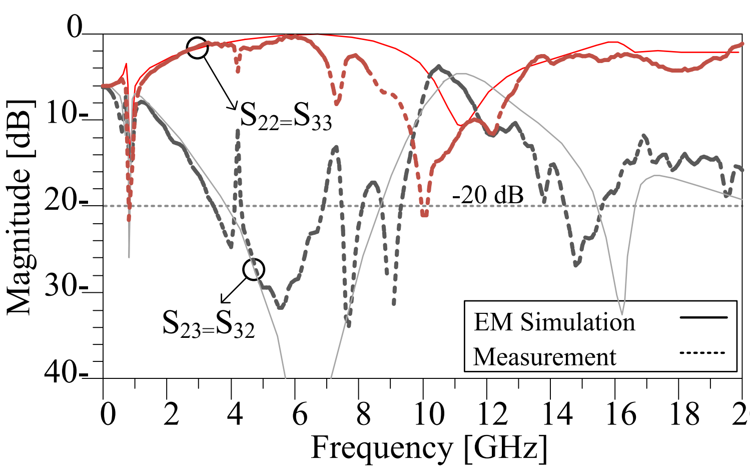
@0.8 GHz, Theoretical SR 80.2%, Practical SR 82.8%

(a) (b)

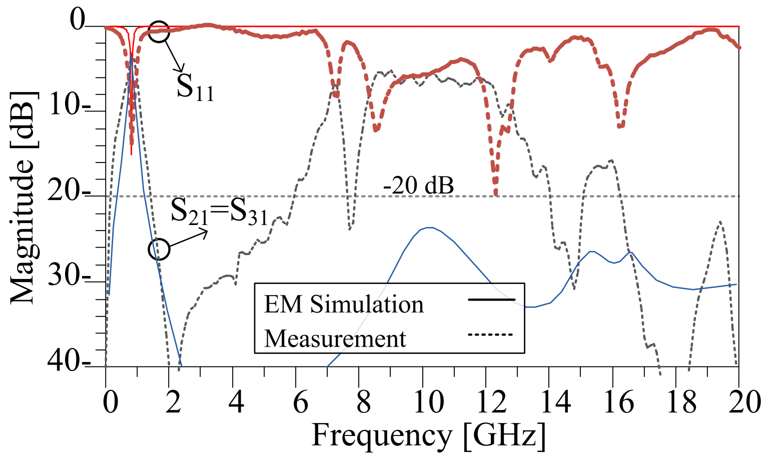
Figure 12. Layouts of the prototype dividers at 0.8 GHz for the (a) third design example with theoretical 69.1% size reduction and (b) fourth design example with theoretical 80.2% size reduction (All dimensions are in mm).

7. Results

To verify the simulation and analyses results, the fourth design example with a theoretical 80.2% size reduction is implemented on the high-frequency substrate with the specifications of RT Duroid 5880 with a thickness of 0.508 mm (20 mil) and Er = 2.2. The proposed divider is fabricated and the measurement results are compared with the EM simulation results as shown in Fig. 13.



(a)



(b)

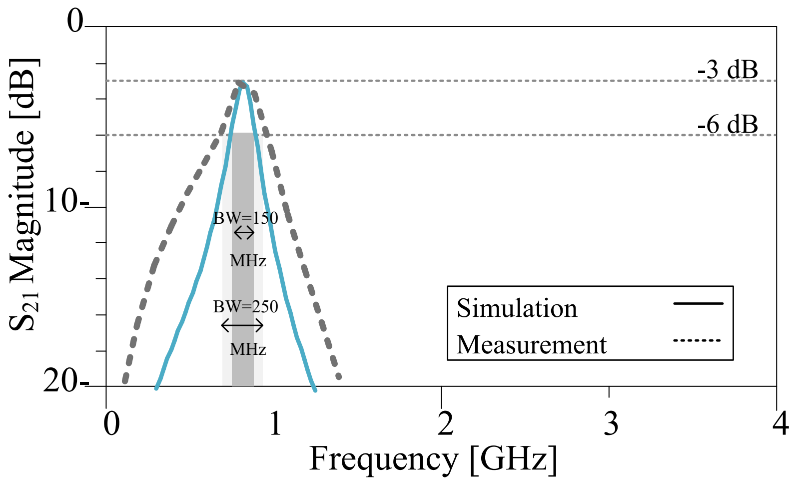


Figure 13. Frequency responses of fourth design example at 0.8 GHz. (a) The S21 and S11 Parameters. (b) The S32 and S22 Parameters. (C) The S21 parameter near operating bandwidth.

The measured results show that the proposed divider can practically operate at 0.7 GHz up to 0.95 GHz which shows 250 MHz operating bandwidth. The minimum insertion loss is 0.3 dB at this bandwidth. As seen the proposed divider can works properly at 0.8 GHz frequency with desirable specifications. Moreover, according to the measured results, the isolation between the output ports, input return loss, and output return loss are 15 dB, 14 dB and 22 dB, respectively. Good suppression band is obtained for the proposed divider with suppression level of more than 20 dB. The 2nd, 3rd, 4th, 5th, 6th, 7th, 8th, 10th, 17th, 18th, 19th, 20th, 21th, 22th, 23th, 24th, and 25th harmonics are suppressed with suppression levels of more than 15 dB, according to the measured results. The fabricated proposed power divider is shown in Fig. 14

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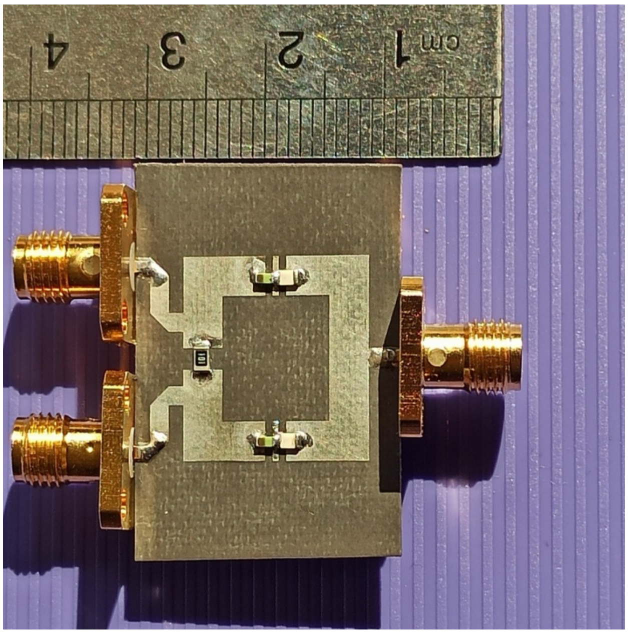

Figure 14. The fabricated proposed power divider.

A comparison table is presented in Table 4, to compare the proposed divider results versus the previous filtering dividers. Design Flexibility (DF) in this Table means that the main parameters of the divider, such as size reduction, harmonic suppression, and bandwidth can be changed to the desired values. According to Table 4, the proposed divider with high design flexibility, low design complexity (DC), compact size and high levels of harmonic suppression can be useful in modern communication systems applications.

Table 4. A comparison between the proposed divider results versus the previous approaches. Operating Frequency: f_0; Harmonic Suppression: HS; Size Reduction percent: SR; Insertion Loss: IL; Design Complexity: DC; Design Flexibility: DF; DEX: Design Example, Sim.: Simulation, Mes.: Measurement.

References		f_0 (GHz)	HR	SR (%)	IL (dB)	Isolation (dB)	Methods	DC	DF
[15]		2.3 3.5	2nd	Very larger than conventional	1.2 1.6	20	SIW	High	Low
[16]		1	2nd 3rd	Larger than conventional	1.1	20	Open Stubs	Low	No
[26]		1	2nd	32 %	0.85	20	Lumped Elements	Low	Low
[29]		1.99	2nd	Larger than conventional	0.74	20	Open Stubs Coupled Lines	Medium	No
[30]		2.0 2.52 3.06	2nd up to 6th	Larger than conventional	0.28	14.4	Lumped Elements	High	No
The Proposed Technique	DEX1; Sim.	2.4	2nd up to 8th	55.5%	0.1	40	LC branches	Low	High
	DEX2; Sim.	2.4	2nd up to 8th	69.1%	0.1	35	LC branches	Low	High
	DEX3; Sim.	0.8	2ndup to25th	69.1%	0.1	40	LC branches	Low	High
	DEX4; Sim.	0.8	2nd up to 25th	80.2%	0.1	38	LC branches	Low	High
	DEX4; Mes.	0.8	2nd up to 25th*	82.8%	0.3	15	LC branches	Low	High

* The 2nd, 3rd, 4th, 5th, 6th, 7th, 8th, 10th, 17th, 18th, 19th, 20th, 21th, 22th, 23th, 24th, and 25th harmonics are suppressed with suppression levels of more than 15 dB according to the measured results in the fabricated divider.

8. Conclusions

A technique based on an innovative hybrid modified structures for microstrip components to enhance their efficiency has been conducted and demonstrated in this paper. In this method, some parts of microstrip lines in a microwave device, are replaced with the proposed LC branches. This replacement leads to extreme size reduction, filtering response and improving the performance of such devices. To assess the effectiveness of the proposed approach, a Filtering Power Divider (FPD) has been redesigned and developed by amending its branch

lines in four different forms. This alteration in branches breeds an enormous size reduction and harmonic suppression in the divider. It is to be noted that with the use of this new structure, 100% size reduction and an infinite number of harmonics suppression are reached theoretically. However, due to lumped element lengths, the theoretical size reduction can be mildly affected in practice, especially in high frequencies. In addition, folding and bending the microstrip lines may have slight effects on the theoretical values. Nevertheless, the proposed technique dramatically improve the efficiency and size of such devices and provides new fields in development of many microstrip components, such as microstrip resonators, filters, diplexers, matching networks, couplers, power amplifiers, and the other types of the dividers.
The following results can be concluded from the proposed divider.

1- Arbitrary size reduction up to theoretically 100% could be achieved although the maximum size reduction percentage would be limited to a number between 90%-100%practically. The practicable size reduction percentage also depends on the operating frequency and the lumped elements dimensions.

2- Infinite numbers of harmonic suppression can be observed in theory. However, the maximum number of size reduction would practically be limited up to about 20-30 harmonics. The practical numbers of harmonic suppression is also changed by operating frequency.

3- The operating bandwidth and sharpness of the divider response can be tuned by setting the LC circuit values and different values of quality factor.

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Author Contributions

S.R. contributed to the conception of the idea and wrote the manuscript. S.R. performed the simulations. M.B.J., J.T. and Z.P. performed the device fabrication, measurements, wrote relevant texts and provided the constructive comments on this work.

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Additional Information

Competing Interests

The authors declare that they have no competing interests.

Figures

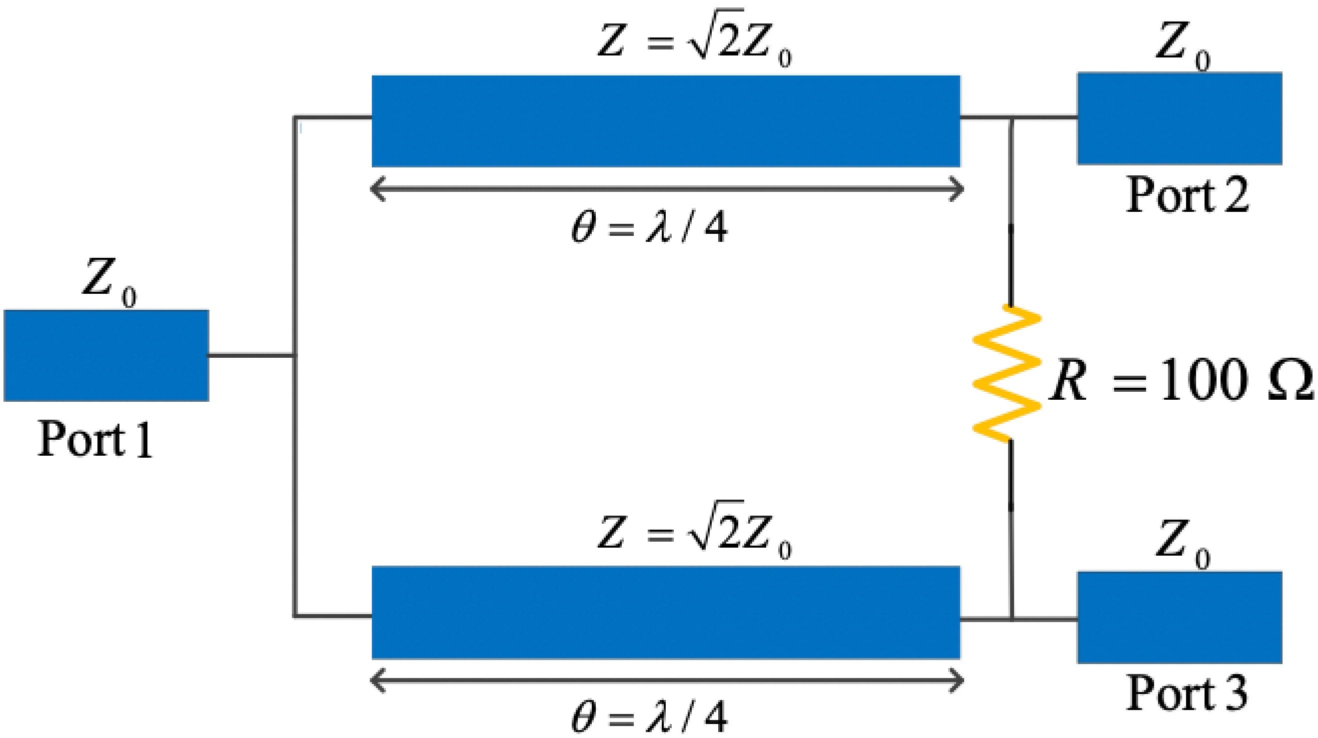

Figure 1

Arrangement of microstrip transmission lines to design a typical WPD

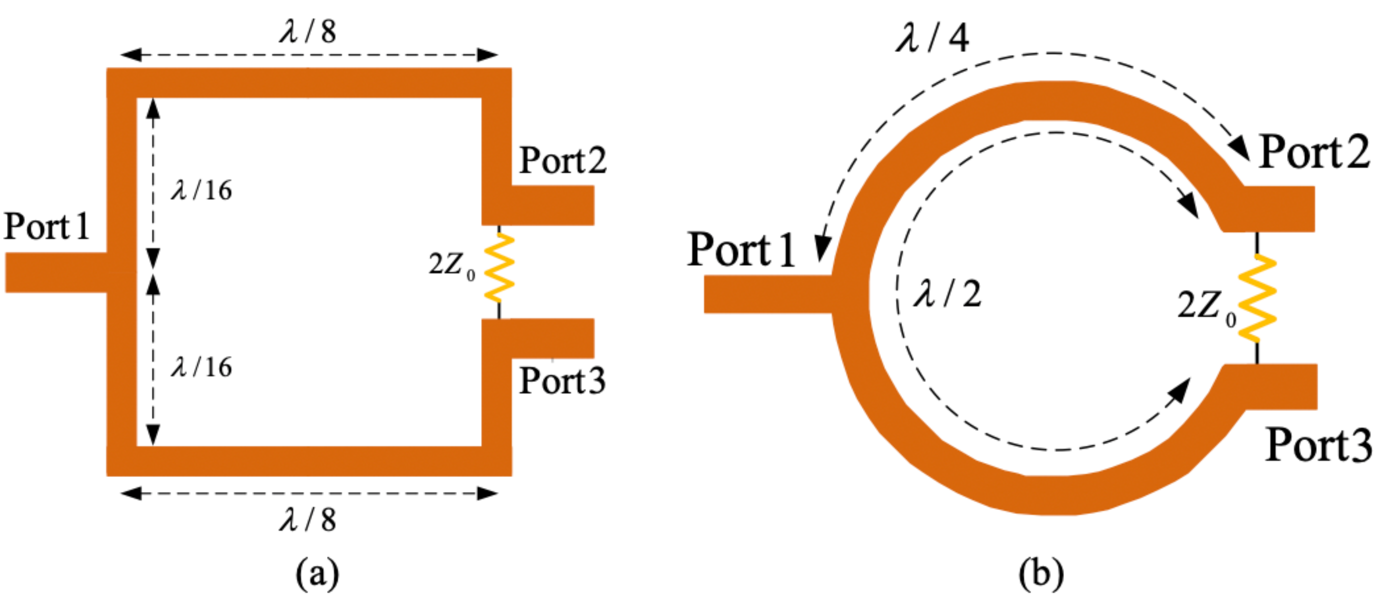

Figure 2

Arrangements of microstrip transmission lines in classic WPD layout; (a) squared-shaped WPD layout; (b) circular-shaped WPD layout.

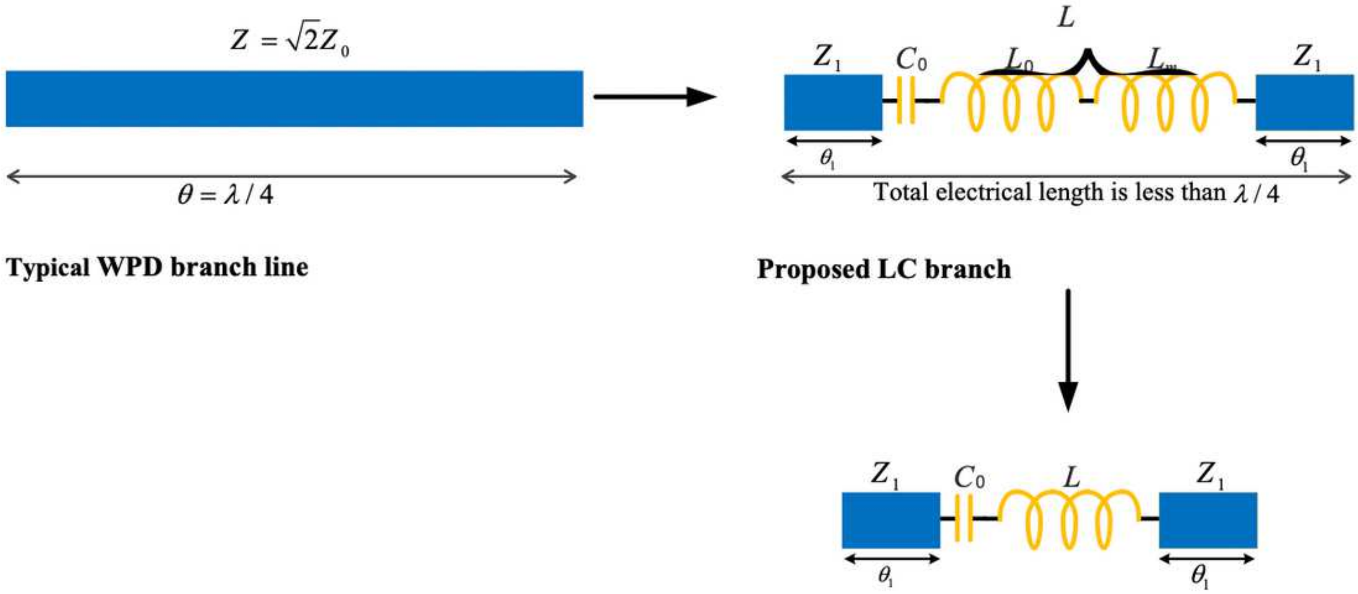

Figure 3

The main idea of replacing the microstrip lines with the proposed LC branches

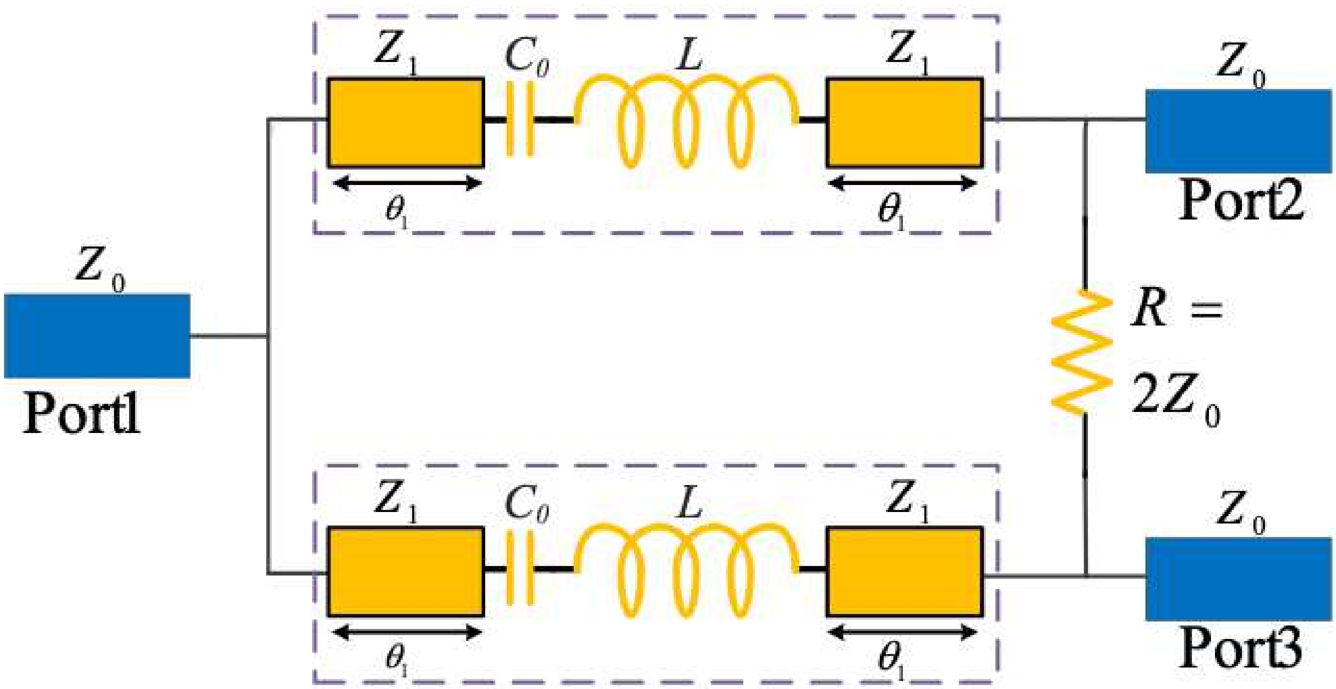

Figure 4

The proposed structure of FPD with the presented LC branches

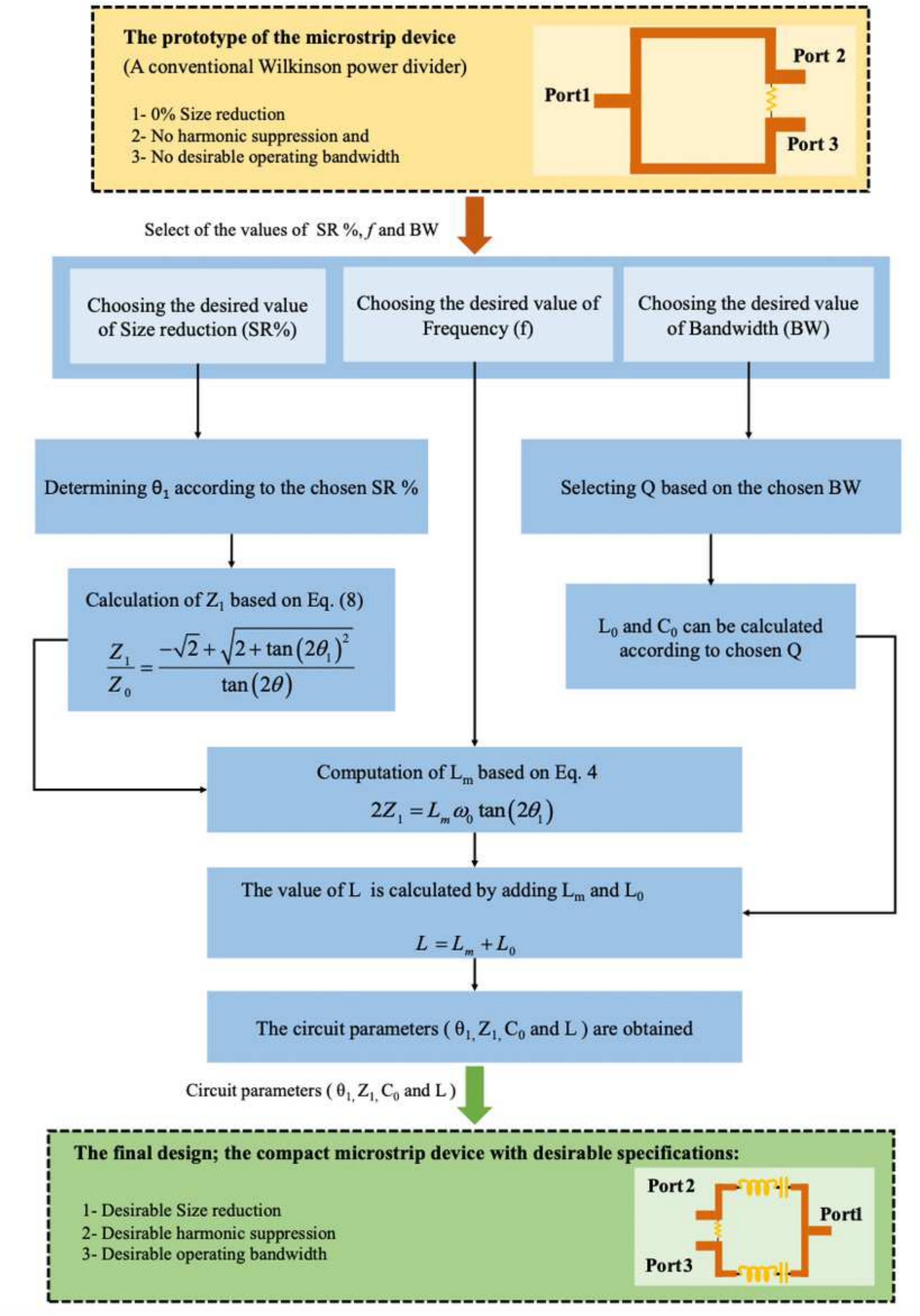

Figure 5

The process of redesign, solving the equations and improvement of a WPD based on the proposed technique. First, the conventional WPD with 0% size reduction, no harmonic suppression and no bandwidth tuning ability is considered. The desire value of SR%, frequency and bandwidth are then assumed arbitrarily. Next, with the use of the proposed analyze flowchart the equations are solved and the desired circuit parameters (θ1, Z1, C0, and L) are achieved. By applying these circuit parameters and

the proposed structure to the typical WPD, the new reshaped compact divider with desirable SR%, great harmonic suppression, and desirable operating bandwidth is obtained.

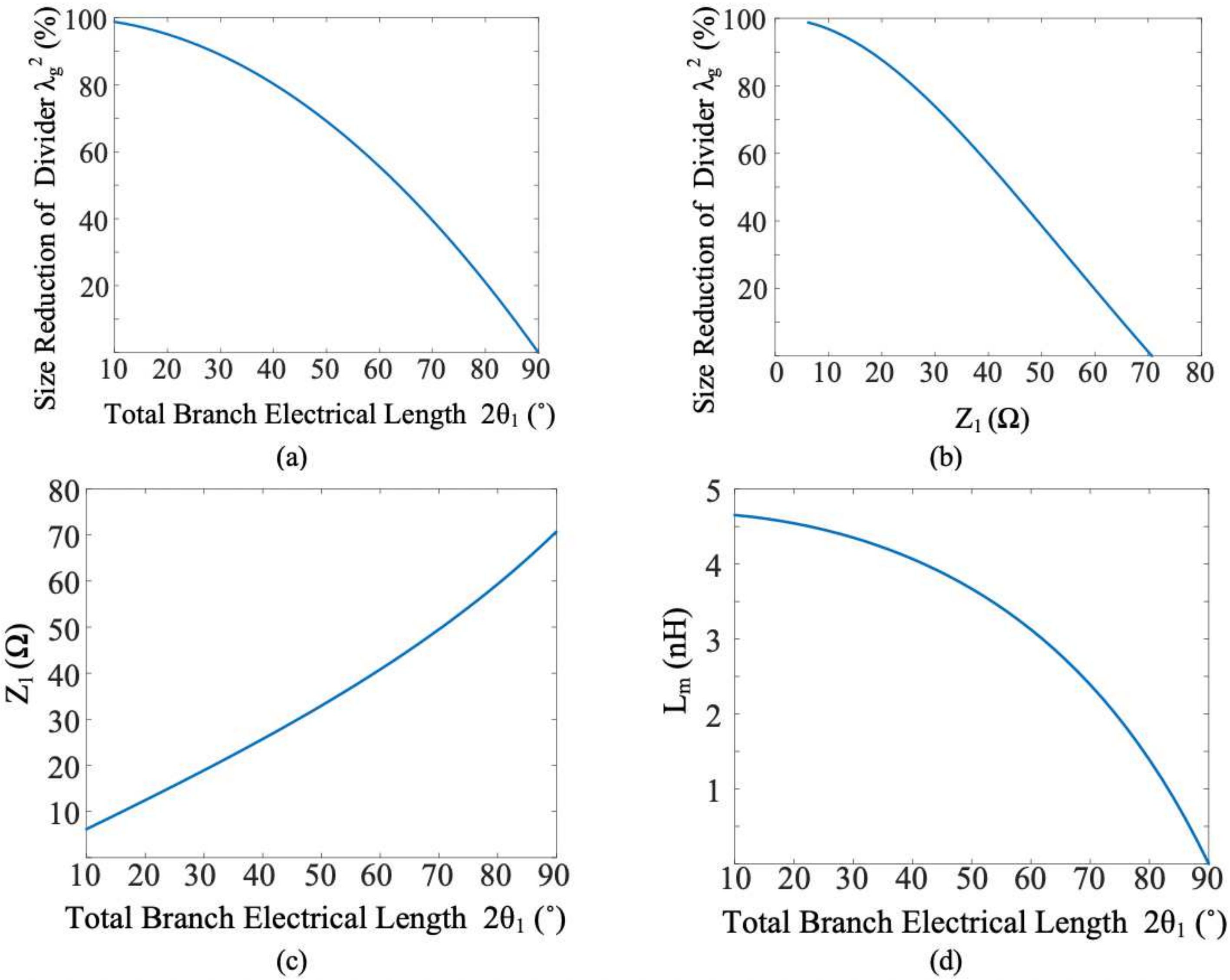

Figure 6

The calculated values of (a) divider maximum size reduction versus total branch electrical length and (b) value of Z1 (Ω). (c) The calculated values of Z1 (Ω) and (d) Lm (nH) versus total branch electrical length.

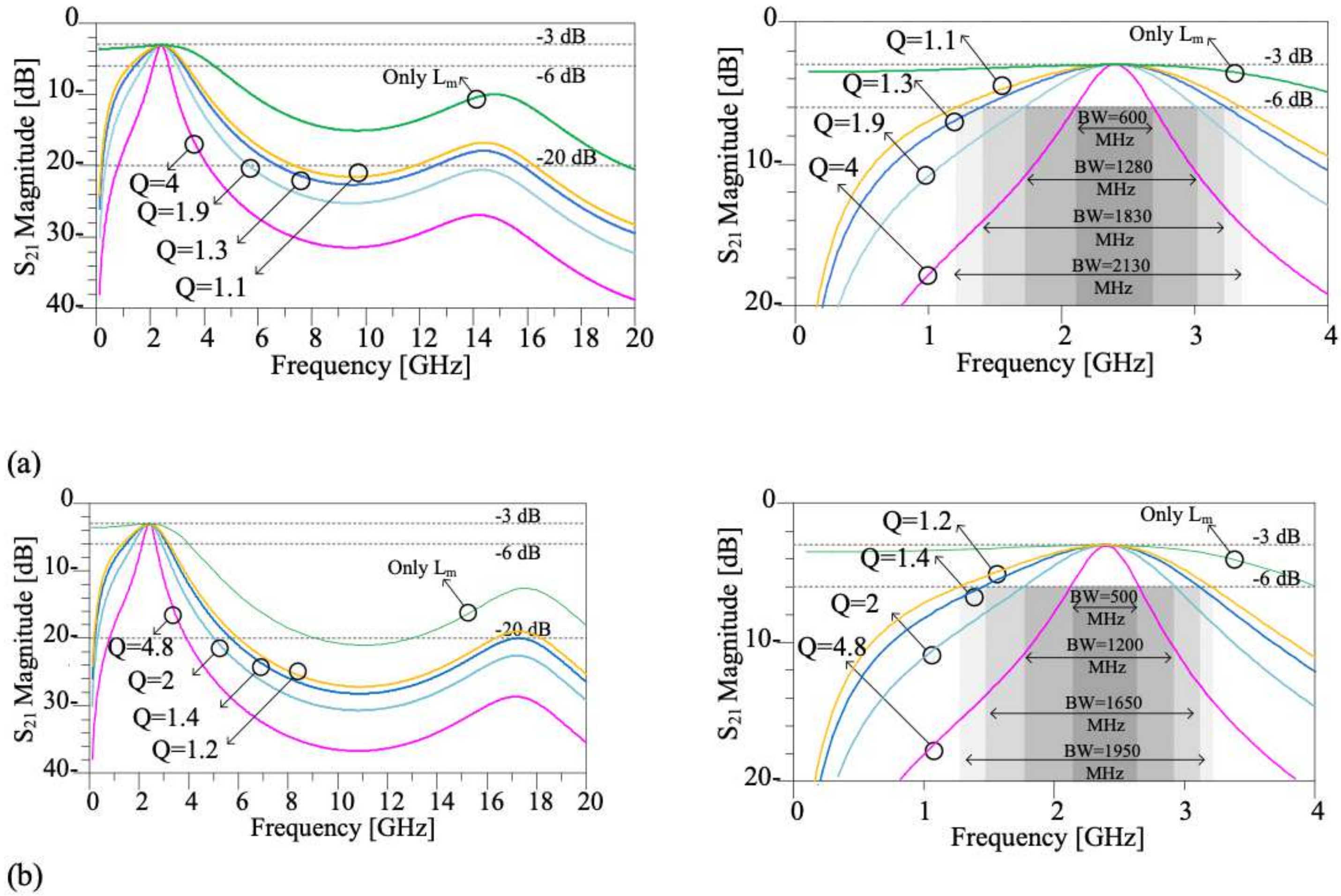

Figure 7

Effects of the series LC circuit different quality factors on the simulated frequency responses of the presented design example. (a) First design example with theoretical 55.5% size reduction and (b) second design example with theoretical 69.1% size reduction, both at 2.4 GHz operating frequency.

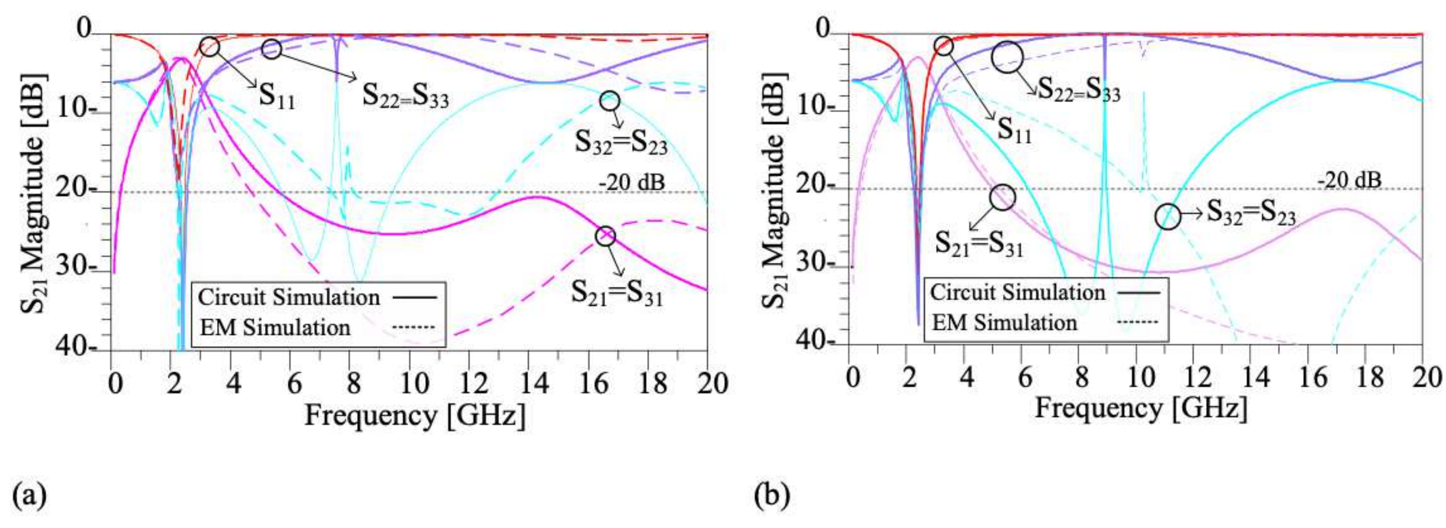

Figure 8

Frequency responses of the prototype dividers at 2.4 GHz for the (a) first design example with theoretical55.5% size reduction and (b) second design example with theoretical 69.1% size reduction.

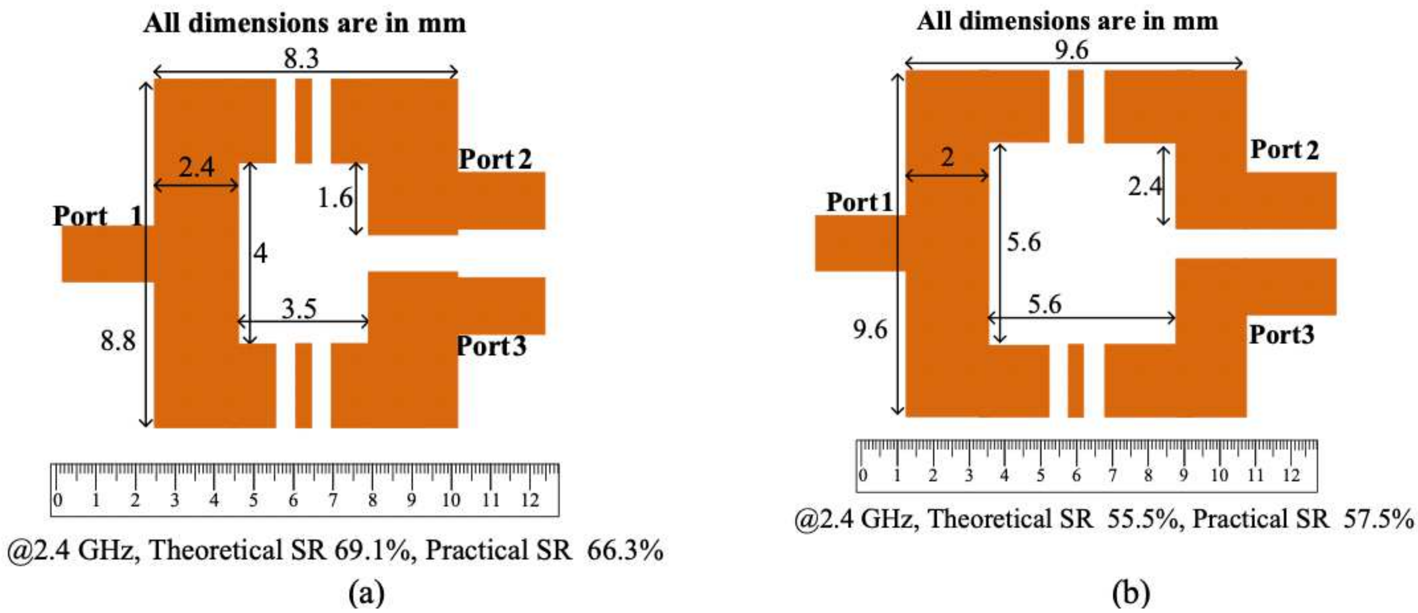

Figure 9

Layouts of the prototype dividers at 2.4 GHz for the (a) first design example with theoretical 55.5% size reduction and (b) second design example with theoretical 69.1% size reduction (All dimensions are in mm).

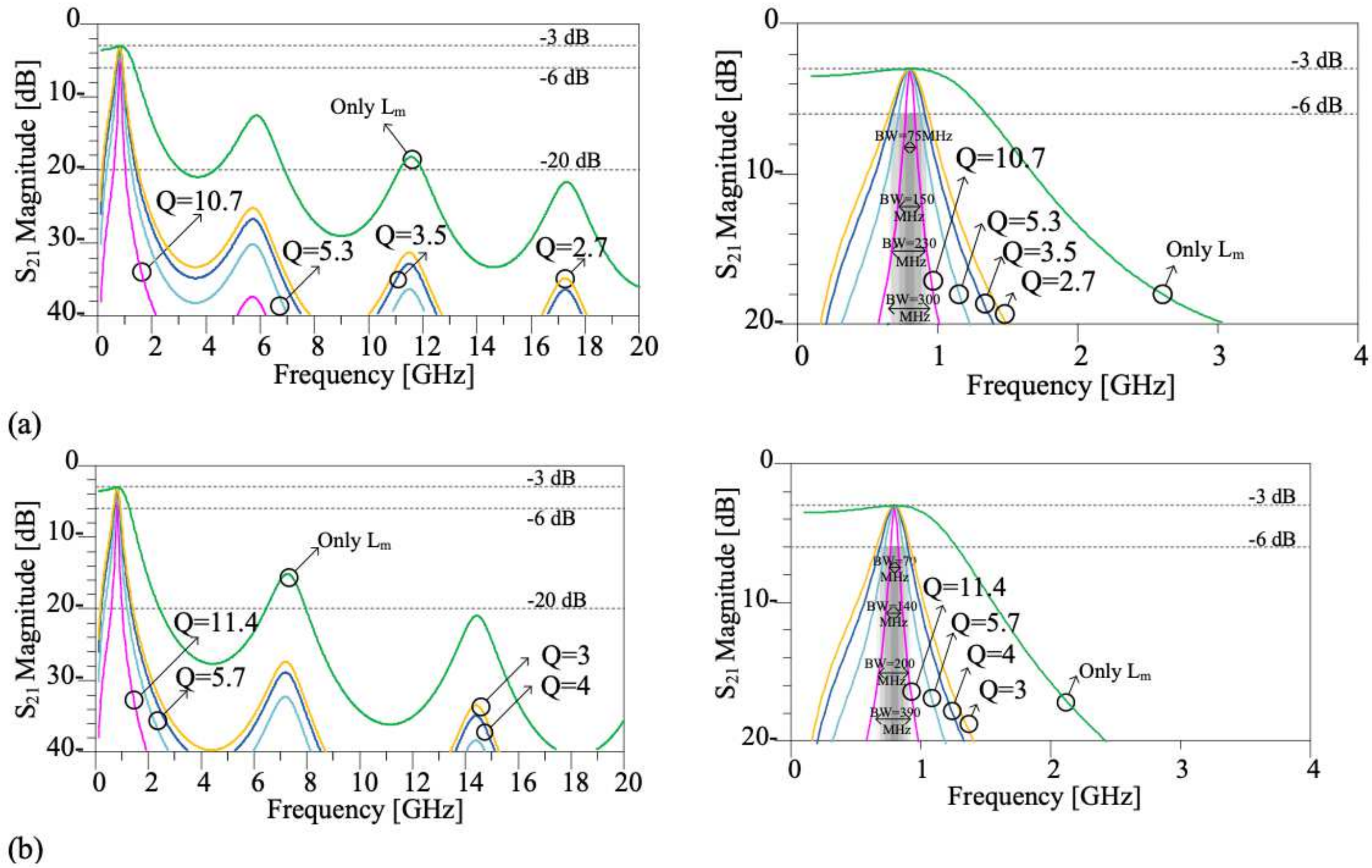

Figure 10

Effects of the series LC circuit different quality factors on the simulated frequency responses of the presented design example. (a) Third design example with theoretical 69.1% size reduction and (b) fourth design example with theoretical 80.2% size reduction, both at 0.8 GHz operating frequency.

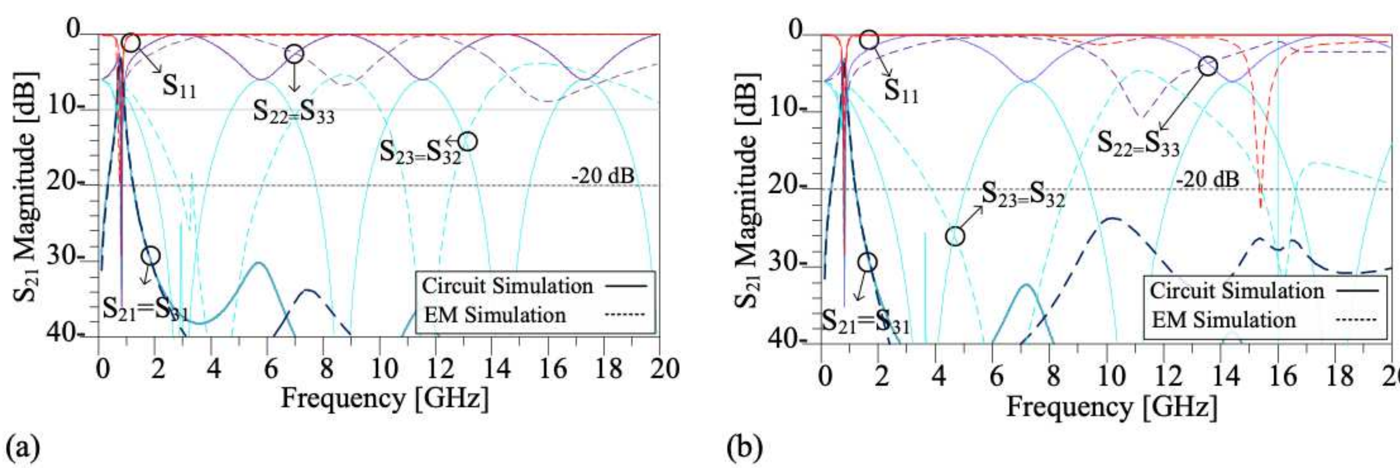

Figure 11

Layouts of the prototype FPDs at 0.8 GHz for the (a) third design example with theoretical 69.1 % size reduction and (b) fourth design example with theoretical 80.2% size reduction

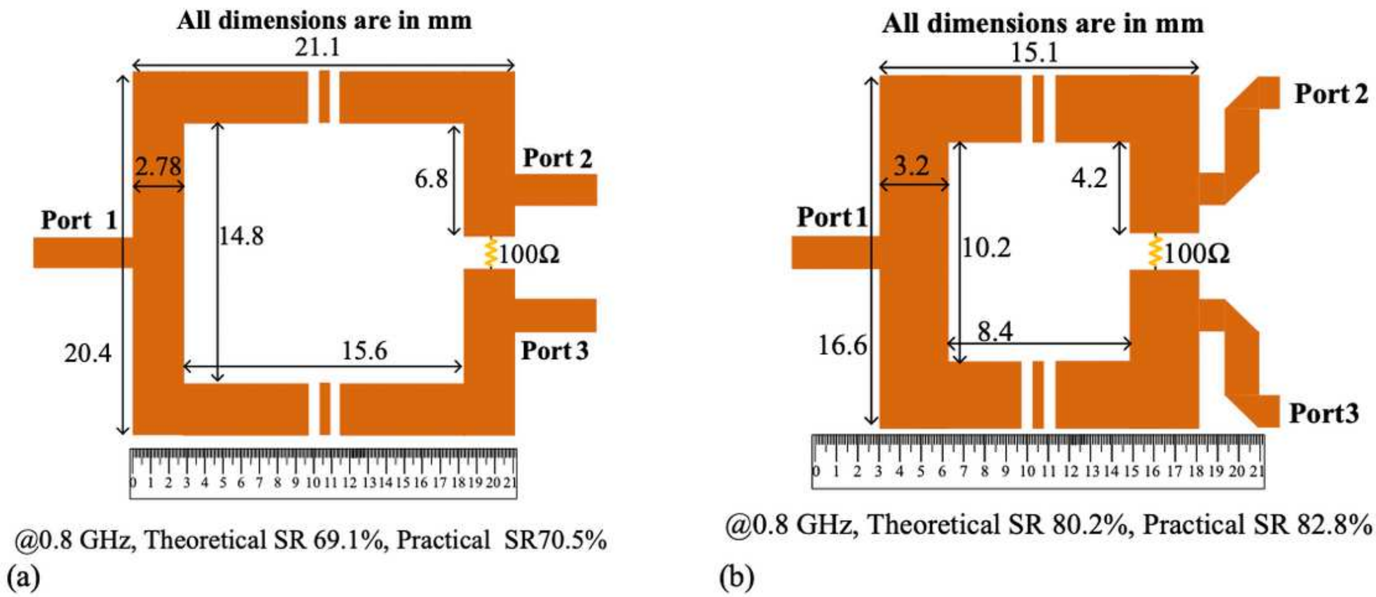

Figure 12

Layouts of the prototype dividers at 0.8 GHz for the (a) third design example with theoretical 69.1% size reduction and (b) fourth design example with theoretical 80.2% size reduction (All dimensions are in mm).

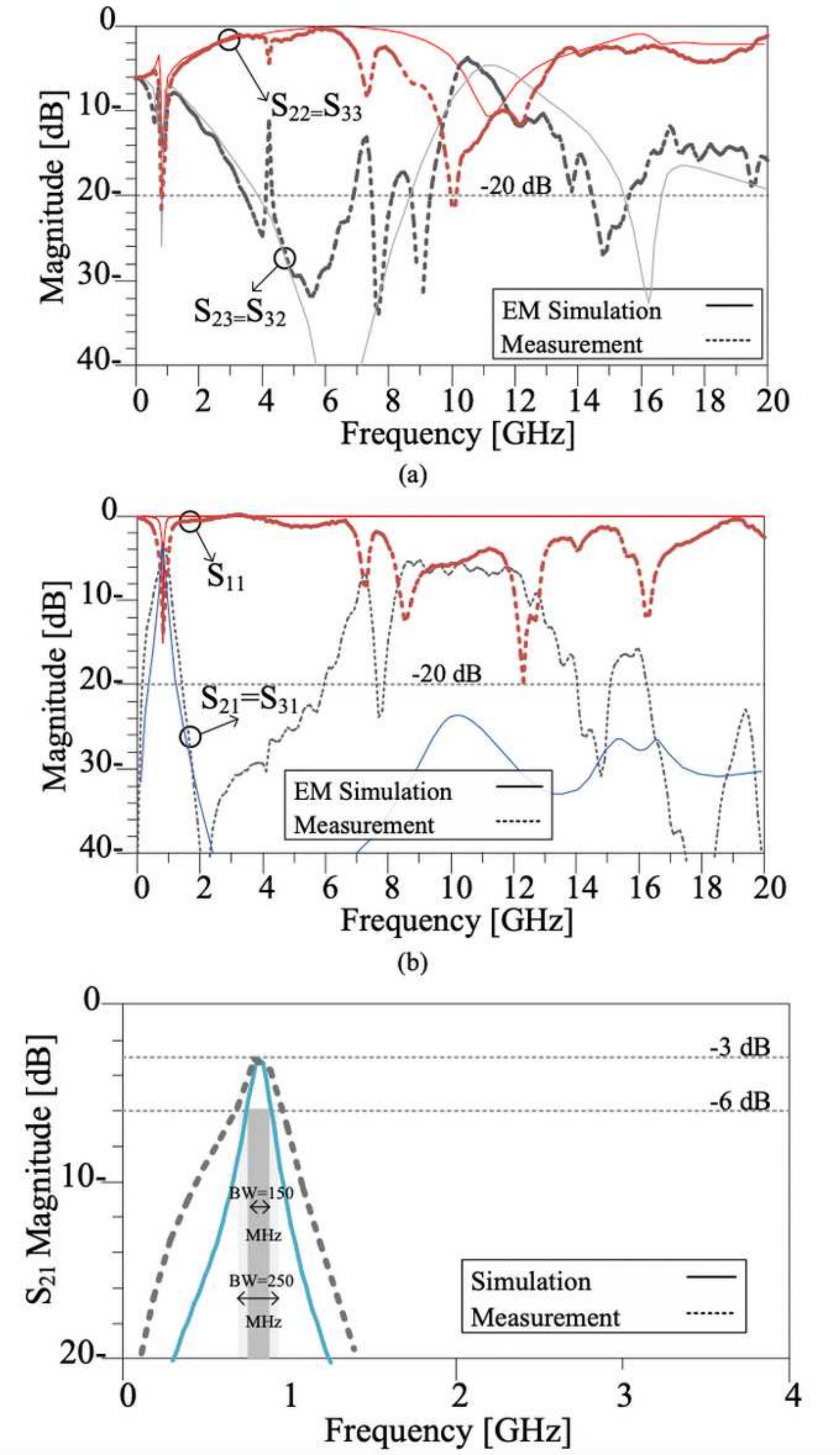

Figure 13

Frequency responses of fourth design example at 0.8 GHz. (a) The S21 and S11 Parameters. (b) The S32 and S22 Parameters. (C) The S21 parameter near operating bandwidth.

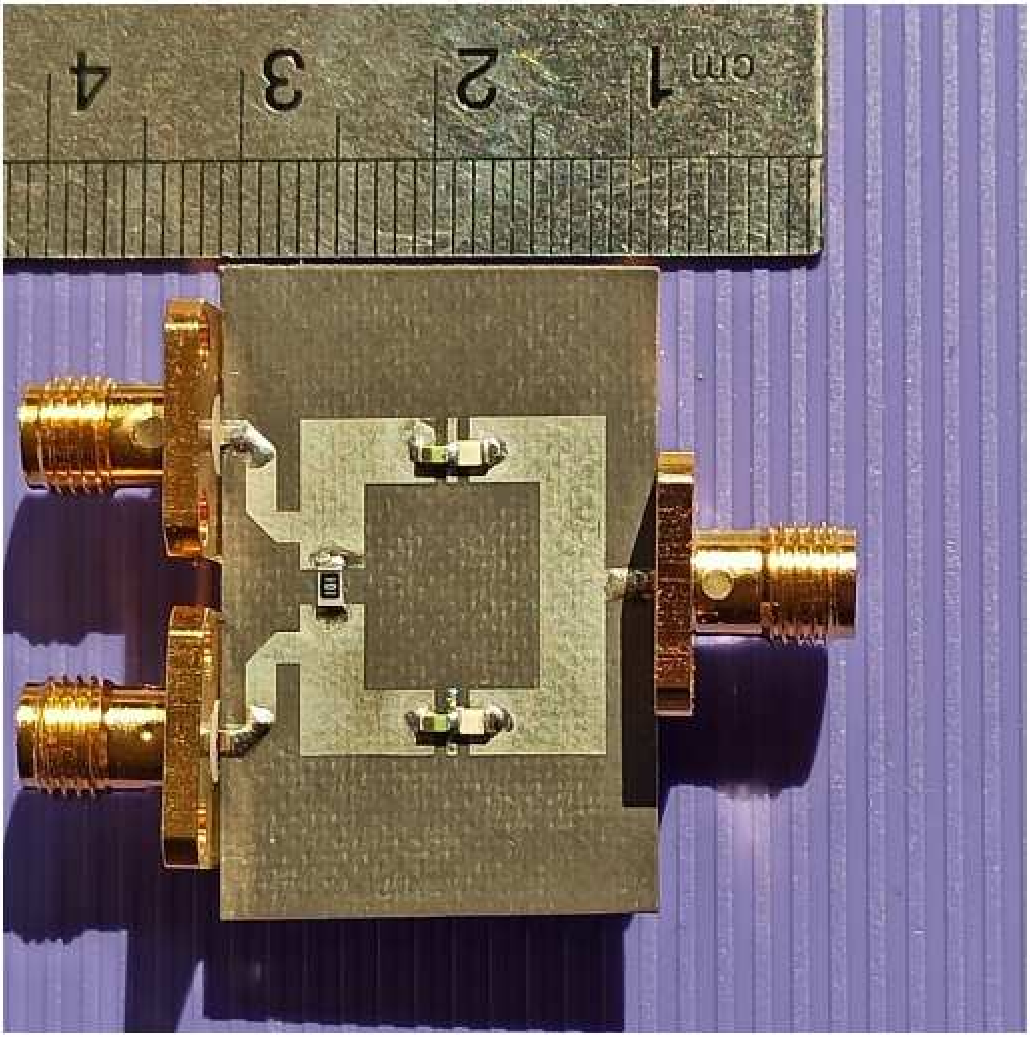

Figure 14

The fabricated proposed power divider.

Supplementary Files

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