A memristive Hopfield network for associative memory

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Method Article

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Abstract

This protocol presents an approach to realize associative memory in a memristive Hopfield network \(MHN). In the MHN, neurons and synapse are constructed with operational amplifiers and memristors, respectively; and control signals are provided by field programming gate array \(FPGA). Different patterns can be stored into the MHN by appropriately setting the synaptic weight matrix and threshold matrix. In the process to recall the pre-stored pattern, the states of the neurons in the MHN are asynchronously updated in sequence under the control of FPGA.

Introduction

An artificial neural network \(ANN) is a bio-inspired information processing paradigm, which has been proved useful in many applications, such as pattern recognition, speech production, real time control, and etc.[1] The Hopfield neural network is one of the most studied ANN[2-5], and its structure can be implemented by an electronic circuit[6]. Although many attempts have been made to simulate or construct ANNs with the ultimate goal to emulate the human brain[7], there are still many challenges. In biological systems, learning involves adjustments of the synaptic weights \(connections) between two adjacent neurons, and the ANNs process information in a similar way. An ideal synapse in the ANN should be reconfigurable, nonvolatile, scalable and low-power. Some types of devices \(such as resistor, capacitor and current source[8]) proposed in the early stage cannot completely satisfy the rigorous requirements of synapses. Recently, memristor[9], which takes advantages of reconfigurability, high-scalability, and low-power consumption[9], has been demonstrated to be an promising candidate for constructing synapses[10-14]. However, constructing ANN with memristors is still of great challenge[15-20]. In this protocol, we present an approach to demonstrate associative memory in a memristive Hopfield network \(MHN). Through an appropriate design of synaptic weight matrix and threshold matrix, pattern\(s) can be stored into the MHN, and the pre-stored pattern\(s) can be successfully retrieved.

Equipment

In the experiment of the Hopfield MHN, the following equipment and components are used: Keithley-4200 semiconductor characterization system, transmission-gate chips \(Texas Instruments CD4066), operational amplifiers \(Texas Instruments LM324N), comparator chip \(Texas Instruments LM339), field programming gate array \(FPGA, model no. ALTERA EP2C8Q208C8), RIGOL oscilloscope \(model no. DS4024), memristors in standard 28-pin dual in-line package \(DIP), capacitors, resistors, ribbon wires, and printed circuit board \(PCB). In the design and simulation of a more complicated MHN consisting of 6561 synapses, IC design software and database \(Cadence 5141 and standard 0.18 μm CMOS process library) are used.

Procedure

Fabrication of the MHN The MHN was fabricated on a printed circuit board \(PCB). The synapse consists of a memristor, a resistor, an inverter and a transmission gate. Positive or negative synaptic weight can be obtained by electronic switches. In the 3-bit MHN, a neuron consists of three synapses. A neuron was constructed with an operational amplifier to obtain the sum of the three inputs. The state of the neuron was stored on a capacitor. The fabrication procedure of the MHN is as follows: design of the schematic circuit of the

MHN; design of the PCB layout of the MHN \(see "Figure 1":http://www.nature.com/protocolexchange/system/uploads/3655/original/Figure_1.jpg?1432391113); assembly of the commercial chips, resistors and capacitors, onto the PCB; wire connection of the memristors with the PCB; and programming of the FPGA to control the MHN. **TIP**: There are two possible circuit configurations for the synaptic connection, as shown in "Figure 2":http://www.nature.com/protocolexchange/system/uploads/3657/original/Figure_2.jpg?1432391117. In the first configuration \(Figure 2\(a)), the synaptic weight of the synapse corresponding to input N_i \(i=1, 2, 3) is w_i=± R /\(M_i + R), where M_i is the resistance of the corresponding memristor. In this design, R should be of a high resistance at the level of 10^6 ohms in order to limit the current and avoid wrongly-switching of the memristor during circuit operation. M_i can only be adjusted in the range from several tens of ohms to several hundreds of kΩ due to the memristor inherent property. As R is much larger than M_i, w_i would be insensitive to M_i and may always stay at ±1. Thus the variable range of the synaptic weight is very small. It is difficult for the MHN to detect such a small change in w_i. In contrast, in the second configuration \(Figure 2\(b)), w_i=± M_i/\(M_i + R), thus the synaptic weight w_i is much more sensitive to the change of M_i and can be varied in a larger range. Therefore, the circuit configuration shown in Figure 2\(b) is used to implement the synapses. **Implementation of associative memory in the MHN** With a given pattern, the synaptic weight matrix elements in equation \(1) \(all equations in this protocol are placed in the "Supplementary document 1":http://www.nature.com/protocolexchange/system/uploads/3659/original/Supplementary_equation_file.pdf?1432386669) are set to w_{11}= w_{22}= w_{33}=0, w_{12}= w_{21}, w_{13}= w_{31}, and w_{23}= w_{32}. The threshold vector **T**=\(θ_1 θ_2 θ_3) is set as θ_1= θ_2= θ_3= θ. Here, w_{ij} \(i, j=1, 2, 3) is in the form of equation \(2). During the recalling process, the MHN is updated according to equation \(3). In equation \(3), t denotes the number of updating cycles; t=0 denotes no updating taking place and the corresponding state vector is the initial vector **X**\(0); and the sign function is defined in equation \(4). In one updating cycle, new states of the neurons are asynchronously updated from x_1, x_2 to x_3 in three stages, which are defined as stages a, b and c, respectively. **Single associative memory** It is required that if the input is the target pattern itself, the final output must also stabilize at the target pattern. Thus, when “110” is stored into the MHN, according to equation \(3) and Hopfield network rule for updating, equation \(5) should be satisfied. With w_{11}= w_{22}= w_{33}=0, w_{12}= w_{21}, w_{13}= w_{31}, and w_{23}= w_{32} and θ_1= θ_2= θ_3= θ, equation \(5) is simplified as shown in equation \(6). Equation \(6) can be satisfied with the following setting: θ=-2/60, w_{12}=4/60, w_{13}=1/60, and w_{23}=-4/60. Thus the synaptic weight matrix is given by equation \(7), and the threshold vector is given by equation \(8). The following initial states **X**\(0) along with equations \(7) and \(8) are put into equation \(3) to verify the convergence: “000”, “001”, “010”, “011”, “100”, “101”, “110”, and “111”. It is found that the MHN can eventually converge to the final state “110” from the above initial states. Here, **X**\(0)= \(x\(0)$_1$ x\(0)$_2$ x\(0)$_3$)=\(0 0 0) is taken as an example to demonstrate the recalling process. In stage a of the first updating cycle, we obtain equation \(9) according to equation \(3). And only x_1 is updated in stage a of the first updating cycle, and thus we eventually obtain equation \(10) in this stage; In stage b of the first updating cycle, equation \(11) can be obtained according to equation \(3). And only x_2 is updated in stage b, so we eventually obtain equation \(12) in this stage; In stage c of the first updating cycle, equation \(13) can be obtained according to equation \(3). And only x_3 is updated in stage c, and thus we eventually obtain equation \(14). From equations \(9)-\(14), we can see that “000” eventually converges to “110”. In a similar way, the MHN converges to “110” from any other initial states. With the synaptic weight matrix shown in

equation \(7), the resistance matrix of the memristors determined from equation \(2) can be set to the form of equation \(15). Note that it is not necessary to adjust the resistances of the memristors exactly to the above values because the MHN has a tolerance to the resistance variation. An offline training scheme for setting the resistance of the memristors to a pre-determined value is implemented with a C Language program embedded in the Keithley 4200 semiconductor characterization system. With the actual resistance matrix **M** in equation \(16), the actual synaptic weight matrix **W** was set to equation \(17). With the above synaptic weight matrixe **W** and the threshold vector in equation \(8), “110” can be correctly retrieved using the MHN fabricated on the PCB. **Multi-associative memory** Similar to the requirement for single associative memory, when the two patterns “000” and “101”, are stored in the MHN, equations \(18) and \(19) should be satisfied. With $\_w_{\_11} = \_w_{\_22} = \_w_{\_33} = 0$, $\_w_{\_12} = \_w_{\_21}$, $\_w_{\_13} = \_w_{\_31}$, and $\_w_{\_23} = \_w_{\_32}$ and $\_\theta_{\_1} = \_\theta_{\_2} = \_\theta_{\_3} = \_\theta\_$, equations \(18) and \(19) are respectively simplified as equations \(20) and \(21). Equations \(20) and \(21) can be satisfied with the following setting: $\_\theta\_ = 6/60$, $\_w_{\_12} = 1/60$, $\_w_{\_13} = 8/60$, and $\_w_{\_23} = 4/60$. Thus the synaptic weight matrix is given by equation \(22), and the threshold vector is given by equation \(23). Putting equations \(22) and \(23) and **X**\(0) \(**X**\(0) can be varied from “000” to “111”) into equation \(3), “000” and “101” can be stored into and retrieved from the MHN theoretically. For the synaptic weight matrix given in equation \(22), the resistance matrix obtained from equation \(2) can be set to the form of equation \(24). The actual resistance matrix and the actual synaptic weight matrix of the fabricated MHN are given by equations \(25) and \(26), respectively:

Timing

The time cost to retrieve the pre-stored pattern in the 3-bit MHN depends on the initial state and the operational frequency. At 5 kHz operating frequency, the time required to retrieve the pre-stored pattern ranges from 33.3 μs to 300 μs depending on the initial states.

Troubleshooting

Failure to set the resistance matrix to the pre-determined one with appropriate precision may lead to the failure of associative memory. In this work, we set the memristors to a low resistance state first with a compliance current \(_e.g._, 0.1 mA, 1 mA, _etc._), and then the memristors are programmed with an offline training scheme which is implemented with a C Language program embedded in the Keithley 4200 semiconductor characterization system. In this way, the resistance matrix with appropriate precision can be obtained.

Anticipated Results

In the associated article, we demonstrated single associative memory and multi-associative memories in a 3-bit MHN. In the 3-bit MHN, the pre-stored pattern\(s) can be successfully retrieved at an operating frequency of 5 kHz. On the other hand, the simulation for a more complicated MHN consisting of 6561 synapses shows that more complicated patterns can be stored and retrieved but convergence errors may occur, as described in the associated article.

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Figures

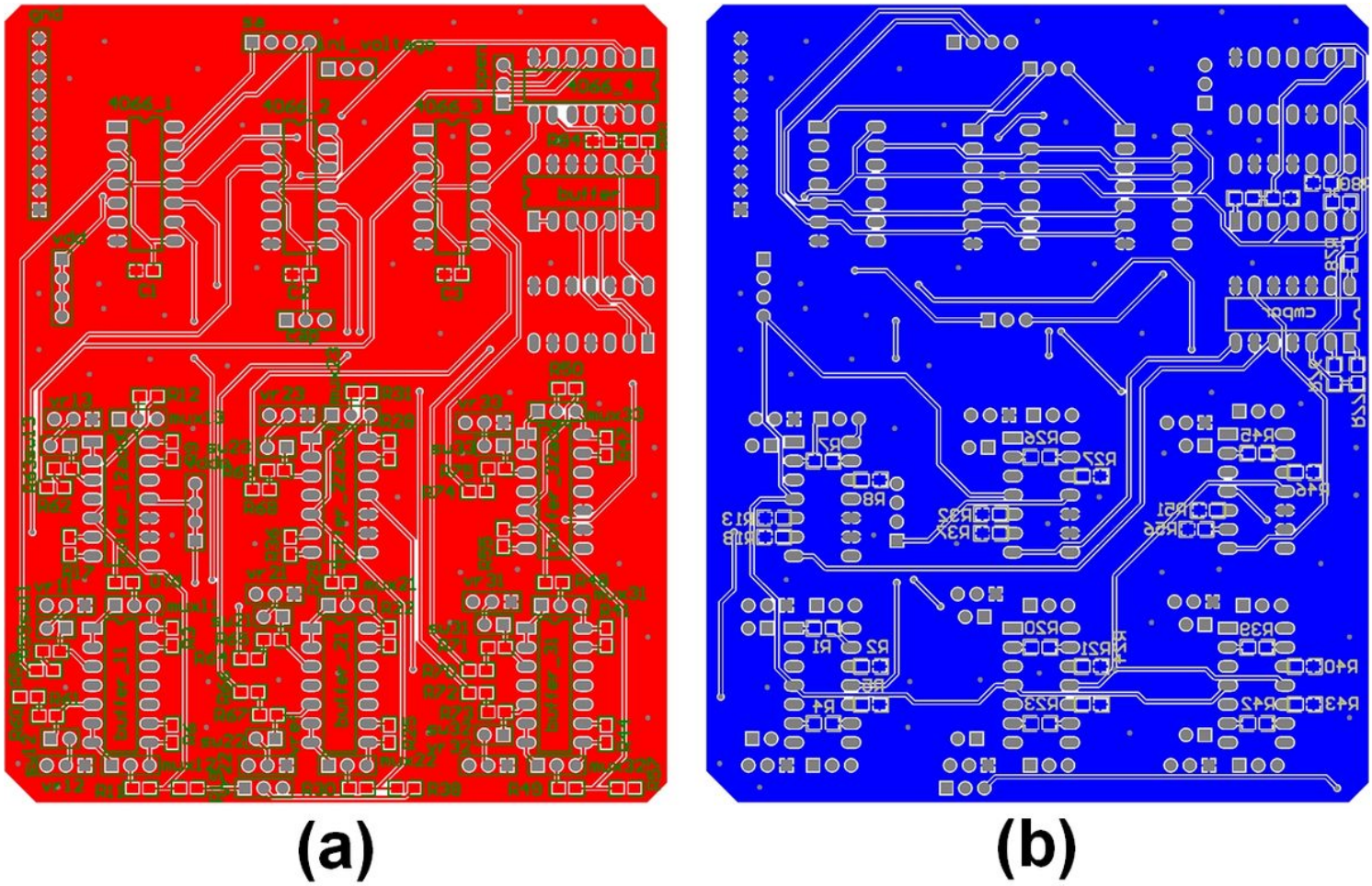

Figure 1

PCB layout of the MHN (a) the front view; and (b) the back view.

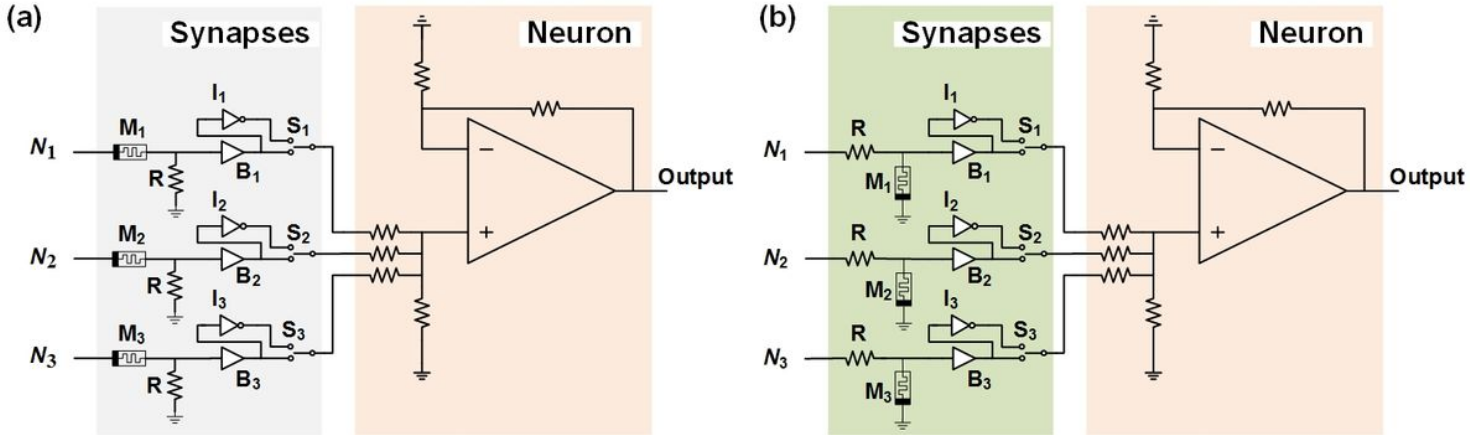

Figure 2

Two possible circuit configurations for the connection between one neuron and three synapses (a) synaptic weight _w~i~_= ± _R_/(_M~i~_ + _R_); and (b) _w~i~_= ± _M~i~_/(_M~i~_ + _R_).

Supplementary Files

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- supplement0.pdf